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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x8/12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f656ewqn-g-sne1

(Continued)

<table>
<tr><th>Part number
Parameter</th><th>MB95F652E</th><th>MB95F653E</th><th>MB95F654E</th><th>MB95F656E</th><th>MB95F652L</th><th>MB95F653L</th><th>MB95F654L</th><th>MB95F656L</th></tr>
<tr><td rowspan="2">UART/SIO</td><td colspan="8">1 channel (The channel can be used either as a UART/SIO channel or as an I²C bus interface channel.)</td></tr>
<tr><td colspan="8">• Data transfer with UART/SIO is enabled.
• It has a full duplex double buffer, variable data length (5/6/7/8 bits), an internal baud rate generator and an error detection function.
• It uses the NRZ type transfer format.
• LSB-first data transfer and MSB-first data transfer are available to use.
• Both clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer are enabled.</td></tr>
<tr><td rowspan="2">I²C bus interface</td><td colspan="8">2 channels (One of the two channels can be used either as an I²C bus interface channel or as a UART/SIO channel.)</td></tr>
<tr><td colspan="8">• Master/slave transmission and reception
• It has the following functions: bus error function, arbitration function, transmission direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.</td></tr>
<tr><td>Watch prescaler</td><td colspan="8">Eight different time intervals can be selected.</td></tr>
<tr><td>Flash memory</td><td colspan="8">• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.
• It has a flag indicating the completion of the operation of Embedded Algorithm.
• Flash security feature for protecting the content of the Flash memory
<table>
<tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr>
<tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr>
</table></td></tr>
<tr><td>Standby mode</td><td colspan="8">There are four standby modes as follows:
• Stop mode
• Sleep mode
• Watch mode
• Time-base timer mode</td></tr>
<tr><td>Package</td><td colspan="8">FPT-24P-M10
FPT-24P-M34
LCC-32P-M19</td></tr>
</table>

3. Differences among Products and Notes on Product Selection

Current consumption

When using the on-chip debug function, take account of the current consumption of Flash memory program/erase.

For details of current consumption, see “18. Electrical Characteristics”.

Package

For details of information on each package, see “2. Packages and Corresponding Products” and “22. Package Dimension”.

Operating voltage

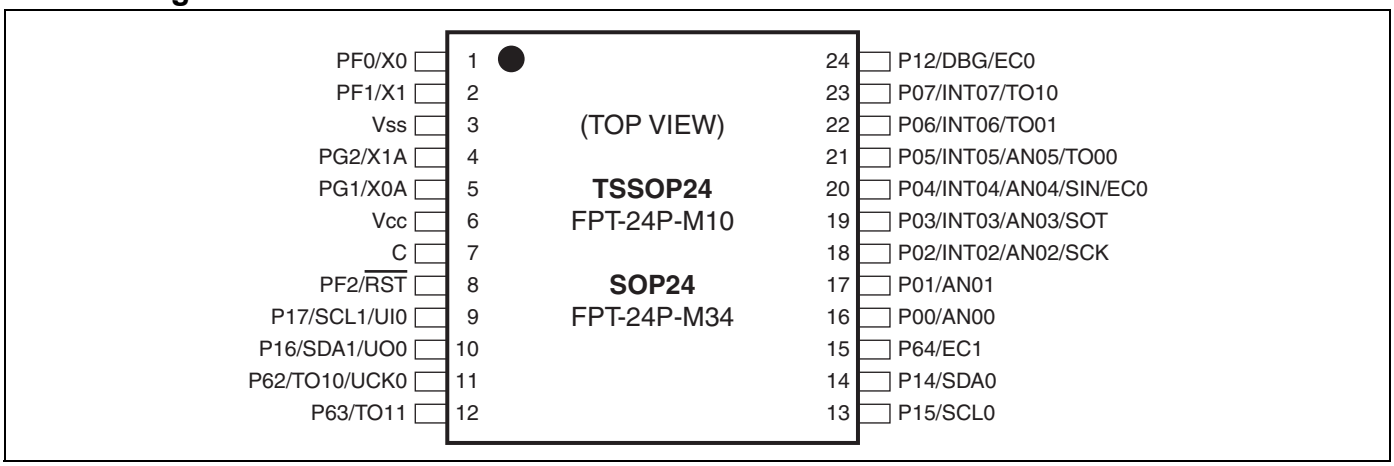
The operating voltage varies, depending on whether the on-chip debug function is used or not.

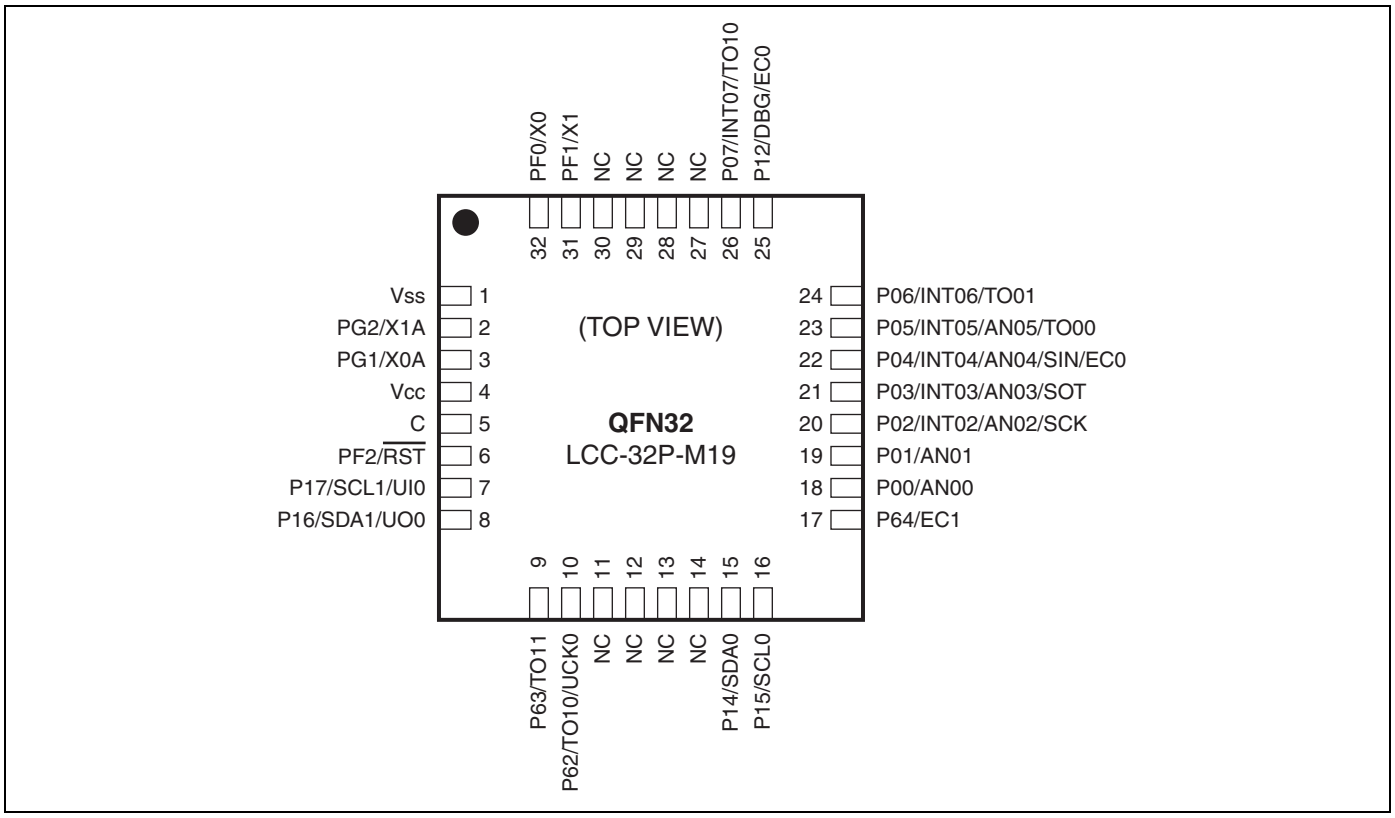
For details of operating voltage, see “18. Electrical Characteristics”.

On-chip debug function

The on-chip debug function requires that V_{CC}, V_{SS} and one serial wire be connected to an evaluation tool. For details of the connection method, refer to “Chapter 20 Example Of Serial Programming Connection” in “New 8FX MB95650L Series Hardware Manual”.

4. Pin Assignment





5. Pin Functions

Pin no.		Pin name	I/O circuit type*4	Function	I/O type			
SOP24*1, TSSOP24*2	QFN32*3				Input	Output	OD*5	PU*6
1	32	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
		X0		Main clock input oscillation pin				
2	31	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
		X1		Main clock I/O oscillation pin				
3	1	V_{SS}	—	Power supply pin (GND)	—	—	—	—
4	2	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
		X1A		Subclock I/O oscillation pin				
5	3	PG1	C	General-purpose I/O port	Hysteresis	CMOS	—	O
		X0A		Subclock input oscillation pin				
6	4	V_{CC}	—	Power supply pin	—	—	—	—
7	5	C	—	Decoupling capacitor connection pin	—	—	—	—
8	6	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
		$\overline{RST}$		Reset pin Dedicated reset pin on MB95F652L/F653L/F654L/F656L				
9	7	P17	J	General-purpose I/O port	CMOS	CMOS	—/O*7	—
		SCL1		I^2C bus interface ch. 1 clock I/O pin				
		UI0		UART/SIO ch. 0 data input pin				
10	8	P16	J	General-purpose I/O port	CMOS	CMOS	—/O*7	—
		SDA1		I^2C bus interface ch. 1 data I/O pin				
		UO0		UART/SIO ch. 0 data output pin				
11	10	P62	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		TO10		8/16-bit composite timer ch. 1 output pin				
		UCK0		UART/SIO ch. 0 clock I/O pin				
12	9	P63	D	General-purpose I/O port High-current output	Hysteresis	CMOS	—	O
		TO11		8/16-bit composite timer ch. 1 output pin				
13	16	P15	I	General-purpose I/O port	CMOS	CMOS	O	—
		SCL0		I^2C bus interface ch. 0 clock I/O pin				
14	15	P14	I	General-purpose I/O port	CMOS	CMOS	O	—
		SDA0		I^2C bus interface ch. 0 data I/O pin				
15	17	P64	D	General-purpose I/O port	Hysteresis	CMOS	—	O
		EC1		8/16-bit composite timer ch. 1 clock input pin				

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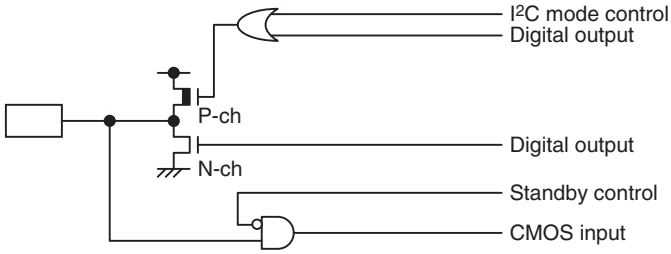
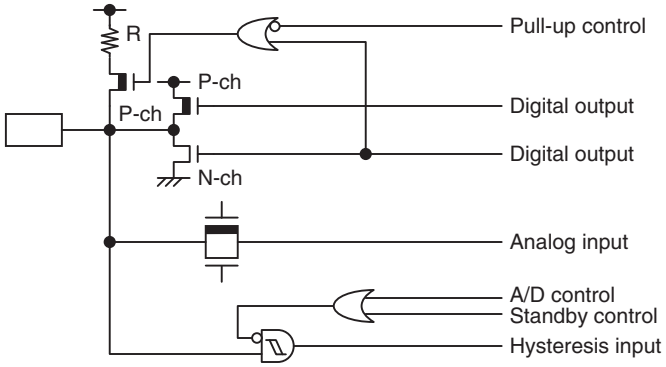
Type	Circuit	Remarks
J		• CMOS output • CMOS input • N-ch open drain output in I2C mode
K		• CMOS output • Hysteresis input • Pull-up control • Analog input • High current output

Address	Register abbreviation	Register name	R/W	Initial value
0x0049	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0b00000000
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C to 0x004E	—	(Disabled)	—	—
0x004F	LVDC	LVD control register	R/W	0b00000100
0x0050	SCR	LIN-UART serial control register	R/W	0b00000000
0x0051	SMR	LIN-UART serial mode register	R/W	0b00000000
0x0052	SSR	LIN-UART serial status register	R/W	0b00001000
0x0053	RDR	LIN-UART receive data register	R/W	0b00000000
	TDR	LIN-UART transmit data register		
0x0054	ESCR	LIN-UART extended status control register	R/W	0b00000100
0x0055	ECCR	LIN-UART extended communication control register	R/W	0b000000XX
0x0056	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register ch. 0	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register ch. 0	R/W	0b00000000
0x005A	RDR0	UART/SIO serial input data register ch. 0	R	0b00000000
0x005B to 0x005F	—	(Disabled)	—	—
0x0060	IBCR00	I^2C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I^2C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I^2C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I^2C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I^2C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I^2C clock control register ch. 0	R/W	0b00000000
0x0066	IBCR01	I^2C bus control register 0 ch. 1	R/W	0b00000000
0x0067	IBCR11	I^2C bus control register 1 ch. 1	R/W	0b00000000
0x0068	IBSR1	I^2C bus status register ch. 1	R/W	0b00000000
0x0069	IDDR1	I^2C data register ch. 1	R/W	0b00000000
0x006A	IAAR1	I^2C address register ch. 1	R/W	0b00000000
0x006B	ICCR1	I^2C clock control register ch. 1	R/W	0b00000000
0x006C	ADC1	8/12-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/12-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/12-bit A/D converter data register (upper)	R/W	0b00000000
0x006F	ADDL	8/12-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	ADC3	8/12-bit A/D converter control register 3	R/W	0b01111100

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000
0x0073	SWRE0	Flash memory sector write control register 0	R/W	0b00000000
0x0074	FSR3	Flash memory status register 3	R	0b000XXXXX
0x0075	FSR4	Flash memory status register 4	R/W	0b00000000
0x0076	WREN	Wild register address compare enable register	R/W	0b00000000
0x0077	WROR	Wild register data test setting register	R/W	0b00000000
0x0078	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0x0079	ILR0	Interrupt level setting register 0	R/W	0b11111111
0x007A	ILR1	Interrupt level setting register 1	R/W	0b11111111
0x007B	ILR2	Interrupt level setting register 2	R/W	0b11111111
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	—	(Disabled)	—	—
0x0F80	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0b00000000
0x0F81	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0b00000000
0x0F82	WRDR0	Wild register data setting register ch. 0	R/W	0b00000000
0x0F83	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0b00000000
0x0F84	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0b00000000
0x0F85	WRDR1	Wild register data setting register ch. 1	R/W	0b00000000
0x0F86	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0b00000000
0x0F87	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0b00000000
0x0F88	WRDR2	Wild register data setting register ch. 2	R/W	0b00000000
0x0F89 to 0x0F91	—	(Disabled)	—	—
0x0F92	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0b00000000
0x0F93	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0b00000000
0x0F94	T01DR	8/16-bit composite timer 01 data register	R/W	0b00000000
0x0F95	T00DR	8/16-bit composite timer 00 data register	R/W	0b00000000
0x0F96	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0b00000000
0x0F97	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	0b00000000
0x0F98	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	0b00000000
0x0F99	T11DR	8/16-bit composite timer 11 data register	R/W	0b00000000
0x0F9A	T10DR	8/16-bit composite timer 10 data register	R/W	0b00000000
0x0F9B	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	0b00000000

(Continued)

P02/INT02/AN02/SCK pin

This pin has the following peripheral functions:

- External interrupt input pin (INT02)
- 8/12-bit A/D converter analog input pin (AN02)
- LIN-UART clock I/O pin (SCK)

P03/INT03/AN03/SOT pin

This pin has the following peripheral functions:

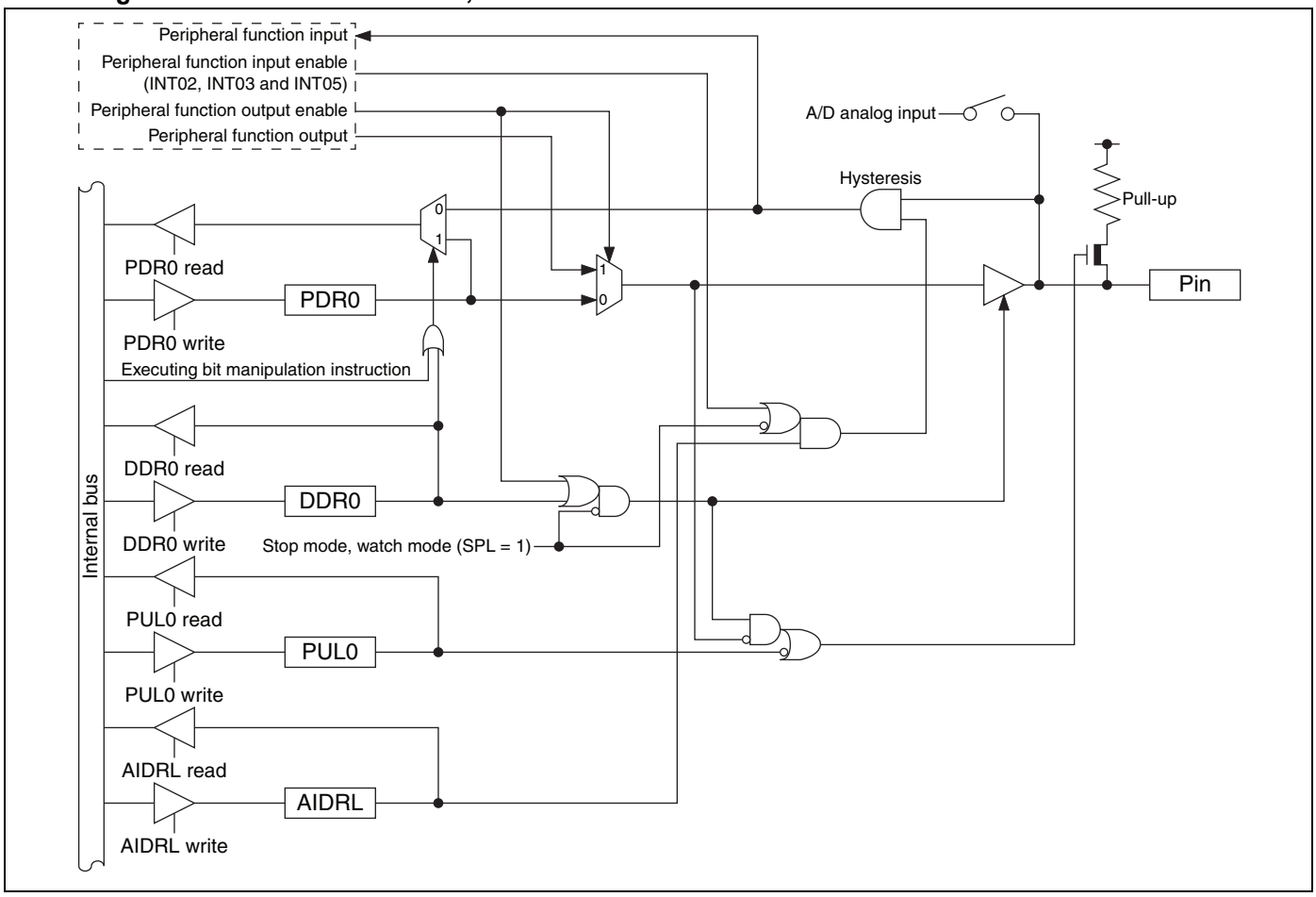
- External interrupt input pin (INT03)
- 8/12-bit A/D converter analog input pin (AN03)
- LIN-UART data output pin (SOT)

P05/INT05/AN05/TO00 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT05)
- 8/16-bit composite timer ch. 0 output pin (TO00)

Block diagram of P02/INT02/AN02/SCK, P03/INT03/AN03/SOT and P05/INT05/AN05/TO00



15.3 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95650L Series Hardware Manual”.

15.3.1 Port 6 configuration

Port 6 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 6 data register (PDR6)
- Port 6 direction register (DDR6)
- Port 6 pull-up register (PUL6)

15.3.2 Block diagrams of port 6

P62/TO10/UCK0 pin

This pin has the following peripheral functions:

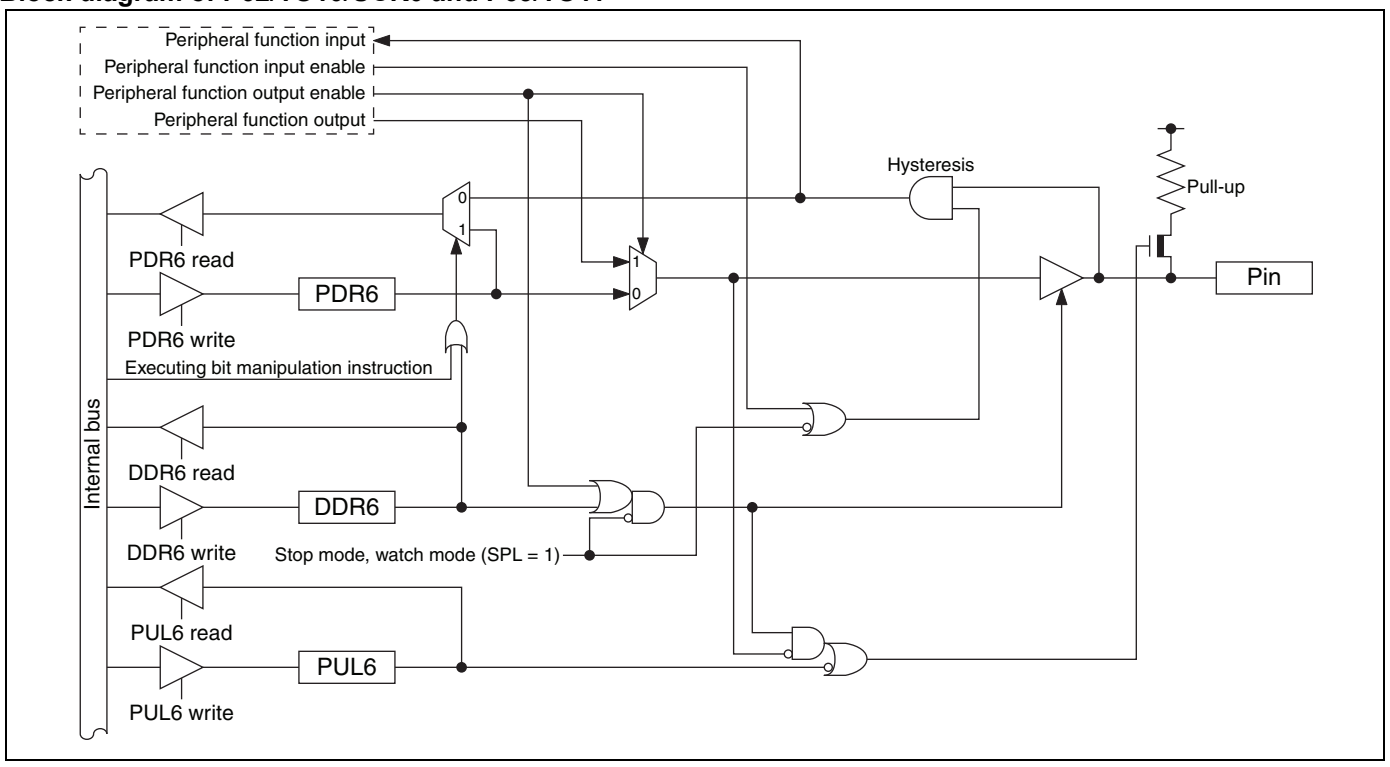
- 8/16-bit composite timer ch. 1 output pin (TO10)
- UART/SIO ch. 0 clock I/O pin (UCK0)

P63/TO11 pin

This pin has the following peripheral function:

- 8/16-bit composite timer ch. 1 output pin (TO11)

Block diagram of P62/TO10/UCK0 and P63/TO11

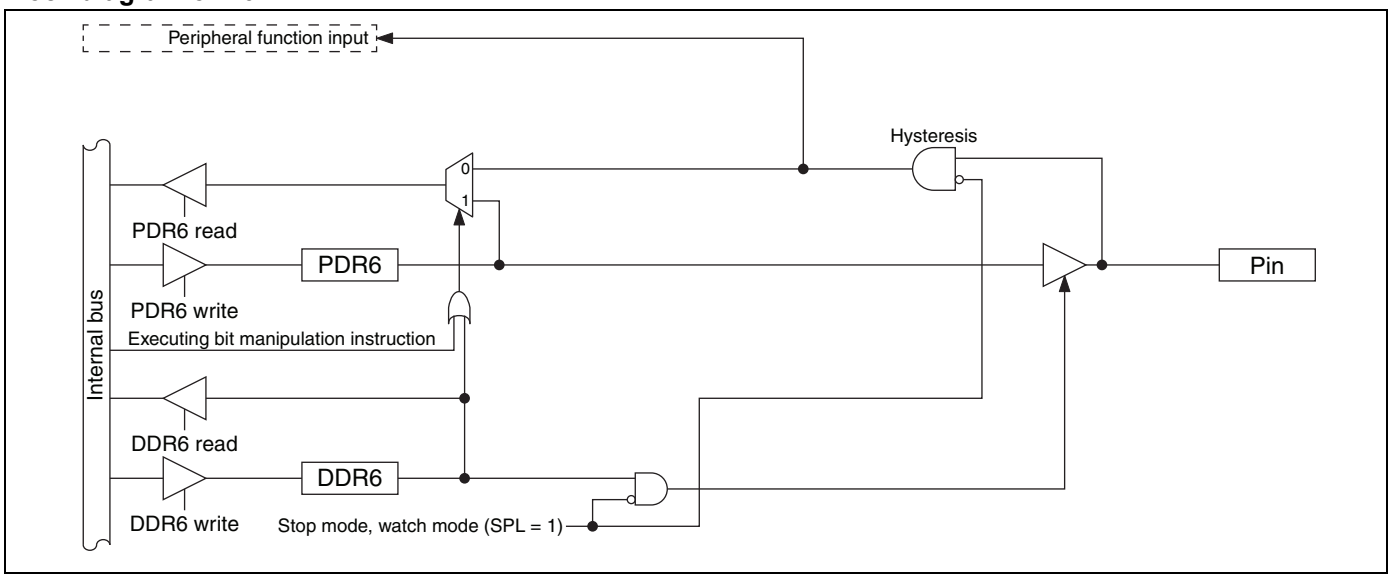


P64/EC1 pin

This pin has the following peripheral function:

- 8/16-bit composite timer ch. 1 clock input pin (EC1)

Block diagram of P64/EC1



17. Pin States in each Mode

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
PF0/X0	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PF1/X1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PF2/$\overline{\text{RST}}$	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input*4
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PG1/X0A	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PG2/X1A	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
P00/AN00	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked*2, *5	- Hi-Z*6 - Input blocked*2, *5	- Previous state kept - Input blocked*2, *5	- Hi-Z*6 - Input blocked*2, *5	- Hi-Z - Input blocked*2
P01/AN01							
P02/INT02/ AN02/SCK							
P03/INT03/ AN03/SOT							
P04/INT04/ AN04/SIN/ EC0							
P05/INT05/ AN05/TO00							

(Continued)

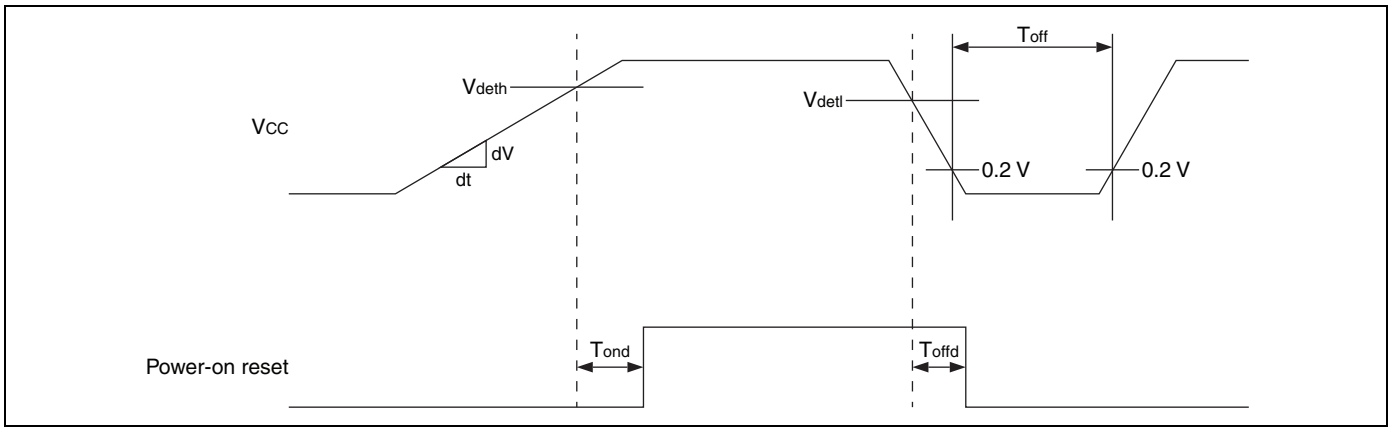
(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the suboscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	150	kHz	When the sub-CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	—	30.8	—	1000	ns	When an external clock is used
		X0, X1	—	—	250	—	ns	When the main PLL clock is used
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used
Input clock pulse width	t_{WH1}, t_{WL1}	X0	—	12.4	—	—	ns	When an external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1	—	—	125	—	ns	When the main PLL clock is used
	t_{WH2}, t_{WL2}	X0A	—	—	15.2	—	µs	When an external clock is used, the duty ratio should range between 40% and 60%.
Input clock rising time and falling time	t_{CR}, t_{CF}	X0, X0A	—	—	—	5	ns	When an external clock is used
CR oscillation start time	t_{CRHWK}	—	—	—	—	50	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	30	µs	When the sub-CR clock is used
PLL oscillation start time	$t_{MCRPLLWK}$	—	—	—	—	100	µs	When the main CR PLL clock is used

18.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply rising time	dV/dt	V_{CC}	0.1	—	—	V/ms	
Power supply cutoff time	T_{off}		1	—	—	ms	
Reset release voltage	V_{deth}		1.44	1.60	1.76	V	At voltage rise
Reset detection voltage	V_{detl}		1.39	1.55	1.71	V	At voltage fall
Reset release delay time	T_{ond}		—	—	10	ms	dV/dt ≥ 0.1 mV/µs
Reset detection delay time	T_{offd}		—	—	0.4	ms	dV/dt ≥ –0.04 mV/µs



*Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2.*
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 – t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 10	—	ns
SCK↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 60	ns
Valid SIN → SCK↓	t_{IVSLE}	SCK, SIN		30	—	ns
SCK↓→ valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 30	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.

18.4.8 I^2C Bus Interface Timing

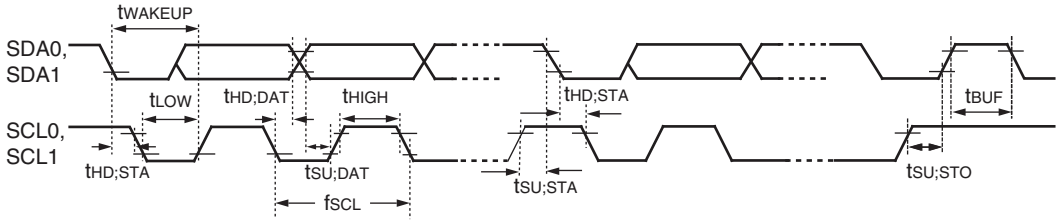
(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL0, SCL1	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL0, SCL1, SDA0, SDA1		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}	SCL0, SCL1		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}	SCL0, SCL1		4.0	—	0.6	—	µs
(Repeated) START condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL0, SCL1, SDA0, SDA1		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓↑	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓↑ → SCL ↑	$t_{SU;DAT}$	SCL0, SCL1, SDA0, SDA1		0.25	—	0.1	—	µs
STOP condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL0, SCL1, SDA0, SDA1		4	—	0.6	—	µs
Bus free time between STOP condition and START condition	t_{BUF}	SCL0, SCL1, SDA0, SDA1		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL0/1 and SDA0/1 lines, and C the load capacitor of the SCL0/1 and SDA0/1 lines.

*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at “L” (t_{LOW}) does not extend.

*3: A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, provided that the condition of $t_{SU;DAT} \geq 250$ ns is fulfilled.



18.5.3 Definitions of A/D Converter Terms

Resolution

It indicates the level of analog variation that can be distinguished by the A/D converter.

When the number of bits is 12, analog voltage can be divided into 2^{12} = 4096.

Linearity error (unit: LSB)

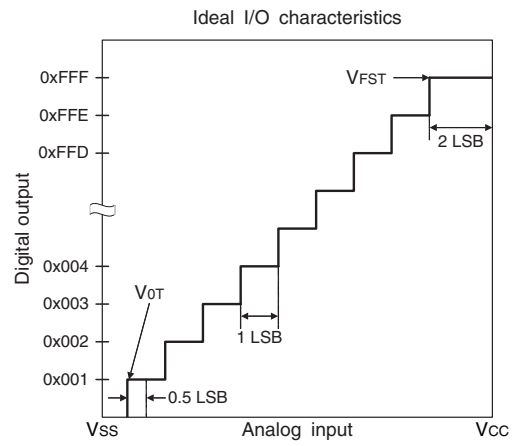
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“000000000000” ← → “000000000001”) of a device to the full-scale transition point (“111111111111” ← → “111111111110”) of the same device.

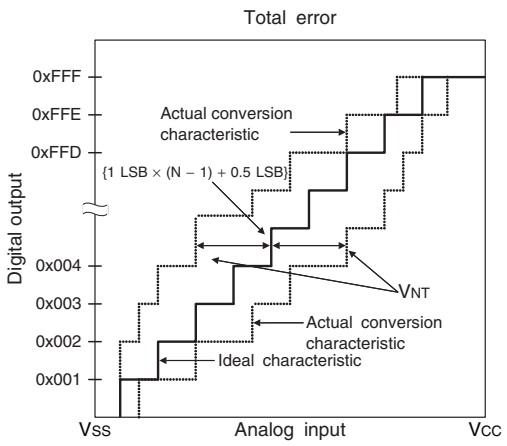
Differential linear error (unit: LSB)

It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.

Total error (unit: LSB)

It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.





$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{4096}\ \text{V}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{LSB}$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

(Continued)

20. Mask Options

No.	Part number	MB95F652E MB95F653E MB95F654E MB95F656E	MB95F652L MB95F653L MB95F654L MB95F656L
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset/interrupt	With low-voltage detection reset/interrupt	Without low-voltage detection reset/interrupt
2	Reset	Without dedicated reset input	With dedicated reset input

21. Ordering Information

Part number	Package
MB95F652EPFT-G-SNE2 MB95F652LPFT-G-SNE2 MB95F653EPFT-G-SNE2 MB95F653LPFT-G-SNE2 MB95F654EPFT-G-SNE2 MB95F654LPFT-G-SNE2 MB95F656EPFT-G-SNE2 MB95F656LPFT-G-SNE2	24-pin plastic TSSOP (FPT-24P-M10)
MB95F652EPF-G-SNE2 MB95F652LPF-G-SNE2 MB95F653EPF-G-SNE2 MB95F653LPF-G-SNE2 MB95F654EPF-G-SNE2 MB95F654LPF-G-SNE2 MB95F656EPF-G-SNE2 MB95F656LPF-G-SNE2	24-pin plastic SOP (FPT-24P-M34)
MB95F652EWQN-G-SNE1 MB95F652EWQN-G-SNERE1 MB95F652LWQN-G-SNE1 MB95F652LWQN-G-SNERE1 MB95F653EWQN-G-SNE1 MB95F653EWQN-G-SNERE1 MB95F653LWQN-G-SNE1 MB95F653LWQN-G-SNERE1 MB95F654EWQN-G-SNE1 MB95F654EWQN-G-SNERE1 MB95F654LWQN-G-SNE1 MB95F654LWQN-G-SNERE1 MB95F656EWQN-G-SNE1 MB95F656EWQN-G-SNERE1 MB95F656LWQN-G-SNE1 MB95F656LWQN-G-SNERE1	32-pin plastic QFN (LCC-32P-M19)

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	06/14/2013	Migrated to Cypress and assigned document number 002-04696. No change to document contents or format.
*A	5216808	AKIH	04/12/2016	Updated to Cypress format.
*B	5846146	YSAT	08/07/2017	Adapted new Cypress logo

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