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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	F ² MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x8/12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f656ewgn-g-sne1



Part number										
	MR95F652F	MB95F653F	MB95F654E	MB95F656E	MB95F652L	MB95F653L	MB95F654L	MB95F656L		
Parameter	B001 0022	B001 000E	W.Boo. 0042	1112001 0002	B001 0022	Boo! 0002	1112001 00-12	B001 0002		
	1 channel (Th	e channel car	n be used eith	er as a UART/	SIO channel c	or as an I ² C bu	us interface ch	annel.)		
UART/SIO	It has a full error detectIt uses the lLSB-first da	 Data transfer with UART/SIO is enabled. It has a full duplex double buffer, variable data length (5/6/7/8 bits), an internal baud rate generator and an error detection function. It uses the NRZ type transfer format. LSB-first data transfer and MSB-first data transfer are available to use. Both clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer are enabled. 								
I ² C bus	2 channels (C channel.)	ne of the two	channels can	be used eithe	r as an I ² C bu	s interface ch	annel or as a	JART/SIO		
interface		llowing function	ons: bus error	on function, arbitr erating and de				ction function,		
Watch prescaler	Eight different	time intervals	can be selec	ted.						
Flash memory	commands. • It has a flag	indicating the	completion o	nbedded Algor of the operation content of the	of Embedded	d Algorithm.	rase-suspend/	erase-resume		
	Number o	of program/era	ise cycles	1000	10000	10000	0			
	Data rete	ntion time		20 year	s 10 year	rs 5 year	rs .			
Standby mode	There are four standby modes as follows: • Stop mode • Sleep mode • Watch mode • Time-base timer mode									
Package		FPT-24P-M10 FPT-24P-M34 LCC-32P-M19								



3. Differences among Products and Notes on Product Selection

Current consumption

When using the on-chip debug function, take account of the current consumption of Flash memory program/erase.

For details of current consumption, see "18. Electrical Characteristics".

Package

For details of information on each package, see "2. Packages and Corresponding Products" and "22. Package Dimension".

Operating voltage

The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of operating voltage, see "18. Electrical Characteristics".

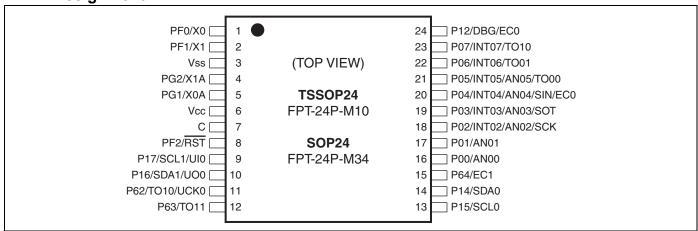
On-chip debug function

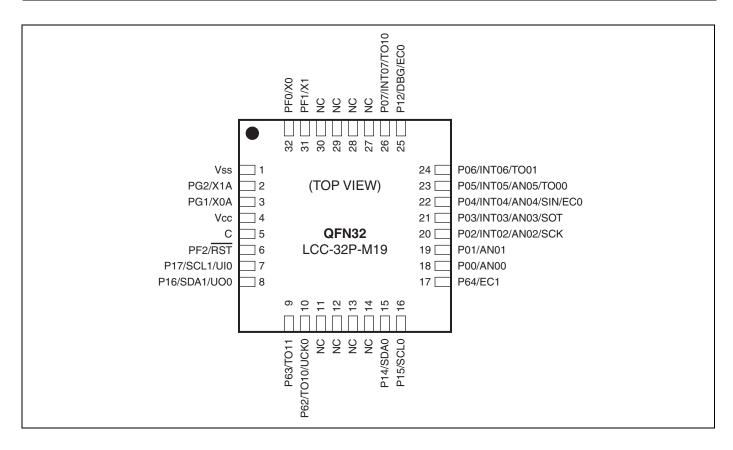
The on-chip debug function requires that V_{CC} , V_{SS} and one serial wire be connected to an evaluation tool. For details of the connection method, refer to "Chapter 20 Example Of Serial Programming Connection" in "New 8FX MB95650L Series Hardware Manual".

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4. Pin Assignment







5. Pin Functions

Pin n	0.		I/O			I/O type		
SOP24* ¹ , TSSOP24* ²	QFN32* ³	Pin name	circuit type* ⁴	Function	Input	Output	OD* ⁵	PU* ⁶
4	32	PF0	В	General-purpose I/O port	Lluotoropio	CMOS		
1	32	X0	В	Main clock input oscillation pin	Hysteresis	CMOS	_	
2	31	PF1	В	General-purpose I/O port	Hysteresis	CMOS		
2	31	X1	ь	Main clock I/O oscillation pin	TIYSICICSIS	CIVIOS	_	
3	1	V_{SS}		Power supply pin (GND)	_	_	_	_
4	2	PG2	С	General-purpose I/O port	Hysteresis	CMOS		0
4	2	X1A	C	Subclock I/O oscillation pin	TIYSICICSIS	CIVIOS	_	
5	3	PG1	С	General-purpose I/O port	Hysteresis	CMOS		0
5	3	X0A	C	Subclock input oscillation pin	TIYSICICSIS	CIVIOS	_	
6	4	V _{CC}	_	Power supply pin	_	_	_	_
7	5	С	_	Decoupling capacitor connection pin	_	_	_	_
		PF2		General-purpose I/O port				
8	6	RST	Α	Reset pin Dedicated reset pin on MB95F652L/F653L/F654L/F656L	Hysteresis	CMOS	O	_
		P17		General-purpose I/O port		CMOS	_/O* ⁷	
9	7	SCL1	J	I ² C bus interface ch. 1 clock I/O pin	CMOS			_
		UI0		UART/SIO ch. 0 data input pin				
		P16		General-purpose I/O port				
10	8	SDA1	J	I ² C bus interface ch. 1 data I/O pin	CMOS	CMOS	—/O* ⁷	—
		UO0		UART/SIO ch. 0 data output pin				
		P62		General-purpose I/O port High-current pin				
11	10	TO10	D	8/16-bit composite timer ch. 1 output pin	Hysteresis	CMOS	_	О
		UCK0		UART/SIO ch. 0 clock I/O pin				
12	9	P63	D	General-purpose I/O port High-current output	Hysteresis	CMOS	_	О
		TO11		8/16-bit composite timer ch. 1 output pin	·			
40	10	P15		General-purpose I/O port	CMOS	CMOC	0	
13	16	SCL0	I	I ² C bus interface ch. 0 clock I/O pin	CIVIOS	CMOS	О	_
14	15	P14	ı	General-purpose I/O port	CMOS	CMOS	0	
14	13	SDA0	I	I ² C bus interface ch. 0 data I/O pin	CIVIOS	CIVIUS	О	
		P64		General-purpose I/O port				
15	17	EC1	D	8/16-bit composite timer ch. 1 clock input pin	Hysteresis	CMOS	_	О



Туре	Circuit	Remarks
J	P-ch Digital output N-ch Standby control CMOS input	 CMOS output CMOS input N-ch open drain output in I²C mode
К	Pull-up control P-ch Digital output Digital output Analog input A/D control Standby control Hysteresis input	 CMOS output Hysteresis input Pull-up control Analog input High current output



Address	Register abbreviation	Register name	R/W	Initial value
0x0049	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0b00000000
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C to 0x004E	_	(Disabled)	_	_
0x004F	LVDC	LVD control register	R/W	0b00000100
0x0050	SCR	LIN-UART serial control register	R/W	0b00000000
0x0051	SMR	LIN-UART serial mode register	R/W	0b00000000
0x0052	SSR	LIN-UART serial status register	R/W	0b00001000
0.0050	RDR	LIN-UART receive data register	DAM	01-0000000
0x0053	TDR	LIN-UART transmit data register		0b00000000
0x0054	ESCR	LIN-UART extended status control register	R/W	0b00000100
0x0055	ECCR	LIN-UART extended communication control register	R/W	0b000000XX
0x0056	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register ch. 0	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register ch. 0	R/W	0b00000000
0x005A	RDR0	UART/SIO serial input data register ch. 0	R	0b00000000
0x005B to 0x005F	_	(Disabled)	_	_
0x0060	IBCR00	I ² C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I ² C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I ² C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I ² C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I ² C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I ² C clock control register ch. 0	R/W	0b00000000
0x0066	IBCR01	I ² C bus control register 0 ch. 1	R/W	0b00000000
0x0067	IBCR11	I ² C bus control register 1 ch. 1	R/W	0b00000000
0x0068	IBSR1	I ² C bus status register ch. 1	R/W	0b00000000
0x0069	IDDR1	I ² C data register ch. 1	R/W	0b00000000
0x006A	IAAR1	² C address register ch. 1		0b00000000
0x006B	ICCR1	¹² C clock control register ch. 1		0b00000000
0x006C	ADC1	8/12-bit A/D converter control register 1		0b00000000
0x006D	ADC2	8/12-bit A/D converter control register 2		0b00000000
0x006E	ADDH	8/12-bit A/D converter data register (upper)	R/W R/W	0b00000000
0x006F	ADDL	8/12-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	ADC3	8/12-bit A/D converter control register 3	R/W	0b01111100



Address	Register abbreviation	Register name	R/W	Initial value
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000
0x0073	SWRE0	Flash memory sector write control register 0	R/W	0b00000000
0x0074	FSR3	Flash memory status register 3	R	0b000XXXXX
0x0075	FSR4	Flash memory status register 4	R/W	0b00000000
0x0076	WREN	Wild register address compare enable register	R/W	0b00000000
0x0077	WROR	Wild register data test setting register	R/W	0b00000000
0x0078	_	Mirror of register bank pointer (RP) and direct bank pointer (DP)	_	_
0x0079	ILR0	Interrupt level setting register 0	R/W	0b11111111
0x007A	ILR1	Interrupt level setting register 1	R/W	0b11111111
0x007B	ILR2	Interrupt level setting register 2	R/W	0b11111111
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	_	(Disabled)	_	_
0x0F80	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0b00000000
0x0F81	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0b00000000
0x0F82	WRDR0	Wild register data setting register ch. 0	R/W	0b00000000
0x0F83	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0b00000000
0x0F84	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0b00000000
0x0F85	WRDR1	Wild register data setting register ch. 1	R/W	0b00000000
0x0F86	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0b00000000
0x0F87	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0b00000000
0x0F88	WRDR2	Wild register data setting register ch. 2	R/W	0b00000000
0x0F89 to 0x0F91	_	(Disabled)	_	_
0x0F92	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0b00000000
0x0F93	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0b00000000
0x0F94	T01DR	8/16-bit composite timer 01 data register	R/W	0b00000000
0x0F95	T00DR	8/16-bit composite timer 00 data register		0b00000000
0x0F96	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0b00000000
0x0F97	T11CR0	8/16-bit composite timer 11 status control register 0		0b00000000
0x0F98	T10CR0	8/16-bit composite timer 10 status control register 0		0b00000000
0x0F99	T11DR	8/16-bit composite timer 11 data register	R/W	0b00000000
0x0F9A	T10DR	8/16-bit composite timer 10 data register	R/W	0b00000000
0x0F9B	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	0b00000000



P02/INT02/AN02/SCK pin

This pin has the following peripheral functions:

- External interrupt input pin (INT02)
- 8/12-bit A/D converter analog input pin (AN02)
- LIN-UART clock I/O pin (SCK)

P03/INT03/AN03/SOT pin

This pin has the following peripheral functions:

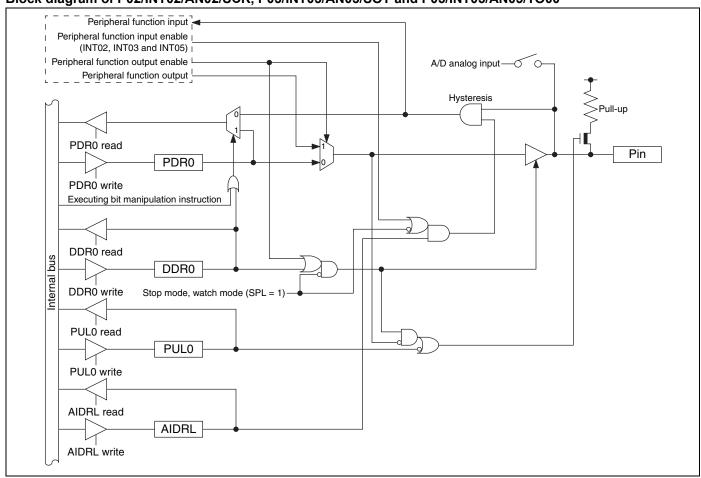
- External interrupt input pin (INT03)
- 8/12-bit A/D converter analog input pin (AN03)
- LIN-UART data output pin (SOT)

P05/INT05/AN05/TO00 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT05)
- 8/12-bit A/D converter analog input pin (AN05)
- 8/16-bit composite timer ch. 0 output pin (TO00)

Block diagram of P02/INT02/AN02/SCK, P03/INT03/AN03/SOT and P05/INT05/AN05/TO00





15.3 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95650L Series Hardware Manual".

15.3.1 Port 6 configuration

Port 6 is made up of the following elements.

- · General-purpose I/O pins/peripheral function I/O pins
- Port 6 data register (PDR6)
- Port 6 direction register (DDR6)
- Port 6 pull-up register (PUL6)

15.3.2 Block diagrams of port 6

P62/TO10/UCK0 pin

This pin has the following peripheral functions:

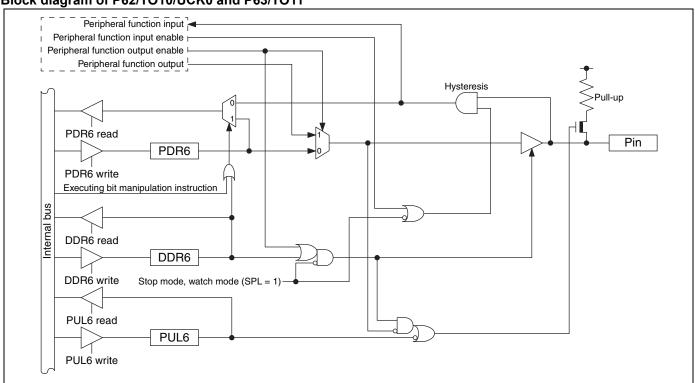
- 8/16-bit composite timer ch. 1 output pin (TO10)
- UART/SIO ch. 0 clock I/O pin (UCK0)

P63/TO11 pin

This pin has the following peripheral function:

• 8/16-bit composite timer ch. 1 output pin (TO11)

Block diagram of P62/TO10/UCK0 and P63/TO11



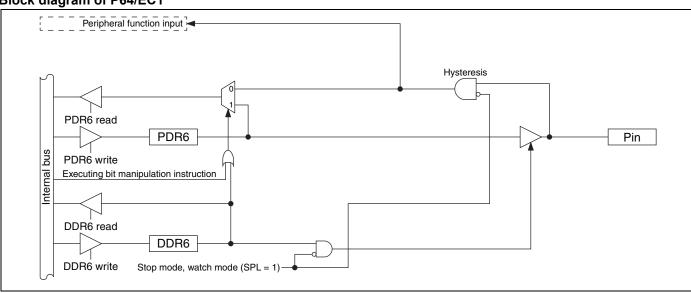


P64/EC1 pin

This pin has the following peripheral function:

• 8/16-bit composite timer ch. 1 clock input pin (EC1)

Block diagram of P64/EC1





17. Pin States in each Mode

Din nome	Normal	Class made	Stop	mode	Watch	mode	0::::::::::::::::::::::::::::::::::::::
Pin name	operation	Sleep mode	SPL=0	SPL=1	SPL=0	SPL=1	On reset
	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	_
PF0/X0	I/O port* ¹	I/O port* ¹	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked* ^{1, *2}	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked* ^{1,} * ²	- Hi-Z - Input enabled* ³ (However, it does not function.)
	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	_
PF1/X1	I/O port* ¹	I/O port* ¹	- Previous state kept - Input blocked* ^{1, *2}	- Hi-Z - Input blocked* ^{1,} * ²	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked* ^{1,} * ²	- Hi-Z - Input enabled* ³ (However, it does not function.)
	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input*4
PF2/RST	I/O port* ¹	I/O port* ¹	- Previous state kept - Input blocked* ^{1, *2}	- Hi-Z - Input blocked* ^{1,} * ²	- Previous state kept - Input blocked* ^{1, *2}	- Hi-Z - Input blocked* ^{1,} * ²	- Hi-Z - Input enabled* ³ (However, it does not function.)
	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	_
PG1/X0A	I/O port* ¹	I/O port* ¹	- Previous state kept - Input blocked* ^{1, *2}	- Hi-Z - Input blocked* ^{1,} * ²	- Previous state kept - Input blocked* ^{1, *2}	- Hi-Z - Input blocked* ^{1,} * ²	- Hi-Z - Input enabled* ³ (However, it does not function.)
	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	_
PG2/X1A	I/O port* ¹	I/O port* ¹	- Previous state kept - Input blocked* ^{1, *2}	- Hi-Z - Input blocked* ^{1,} * ²	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked* ^{1,} * ²	- Hi-Z - Input enabled* ³ (However, it does not function.)
P00/AN00							
P01/AN01							
P02/INT02/ AN02/SCK							
P03/INT03/ AN03/SOT	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	 Previous state kept Input blocked*^{2, *5} 	- Hi-Z* ⁶ - Input blocked* ^{2,} * ⁵	 Previous state kept Input blocked*^{2, *5} 	- Hi-Z* ⁶ - Input blocked* ^{2,} * ⁵	- Hi-Z - Input blocked* ²
AN04/SIN/ EC0 P05/INT05/ AN05/TO00		3			-		



(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

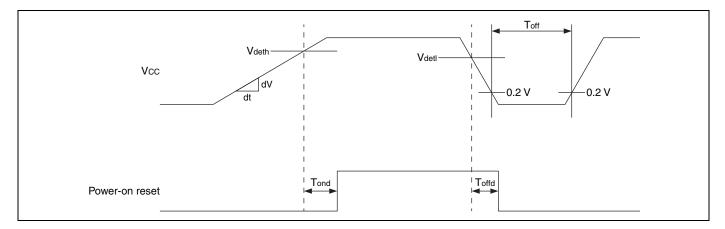
Danamatan	Compleal	Din nome	Condition		Value		I I mit	Domonico
Parameter	Symbol	Pin name	Condition	Min	Тур	Max	Unit	Remarks
	F _{CL}	X0A, X1A	_	_	32.768	_	kHz	When the suboscillation circuit is used
Clock frequency				_	32.768	_	kHz	When the sub-external clock is used
	F _{CRL}	_	_	50	100	150	kHz	When the sub-CR clock is used
		X0, X1	_	61.5	_	1000	ns	When the main oscillation circuit is used
Clock cycle time	t _{HCYL}	X0	_	30.8	_	1000	ns	When an external clock is used
		X0, X1	_	_	250	_	ns	When the main PLL clock is used
	t _{LCYL}	X0A, X1A	_	_	30.5	_	μs	When the subclock is used
	t _{WH1} , t _{WL1}	X0	_	12.4	_	_	ns	When an external clock is used, the duty ratio should range between 40% and 60%.
Input clock pulse width		X0, X1	_	_	125	_	ns	When the main PLL clock is used
pulse watt	t _{WH2} , t _{WL2}	X0A	_	_	15.2	_		When an external clock is used, the duty ratio should range between 40% and 60%.
Input clock rising time and falling time	t _{CR} , t _{CF}	X0, X0A	_	_	_	5	ns	When an external clock is used
CR oscillation	t _{CRHWK}	_	_	_	_	50	μs	When the main CR clock is used
start time	t _{CRLWK}	_	_		_	30	μs	When the sub-CR clock is used
PLL oscillation start time	t _{MCRPLLWK}	_	_			100	μs	When the main CR PLL clock is used



18.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin		Value		Unit	Remarks
Parameter	Symbol	name	Min	Тур	Max	Ollit	Remarks
Power supply rising time	dV/dt		0.1	_	_	V/ms	
Power supply cutoff time	T _{off}		1	_	_	ms	
Reset release voltage	V _{deth}	\ \ \	1.44	1.60	1.76	V	At voltage rise
Reset detection voltage	V _{detl}	V _{CC}	1.39	1.55	1.71	V	At voltage fall
Reset release delay time	T _{ond}		_	_	10	ms	dV/dt ≥ 0.1 mV/μs
Reset detection delay time	T _{offd}		_	_	0.4	ms	$dV/dt \ge -0.04 \text{ mV/}\mu\text{s}$





Sampling is executed at the falling edge of the sampling $clock^{*1}$, and serial clock delay is disabled clock (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 0)

 $(V_{CC} = 3.0 \text{ V to } 5.5 \text{ V}, V_{SS} = 0.0 \text{ V}, T_{A} = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C})$

Parameter	Symbol	Pin name	Condition	Value		Unit
Farameter	Symbol	Fill lialite	Condition	Min	Max	Oilit
Serial clock cycle time	t _{SCYC}	SCK		5 t _{MCLK} *3	_	ns
$SCK^{\uparrow} \rightarrow SOT$ delay time	t _{SHOVI}	SCK, SOT	Internal clock operation output pin:	-50	+50	ns
Valid SIN → SCK \downarrow	t _{IVSLI}	SCK, SIN	C _I = 80 pF + 1 TTL	t _{MCLK} *3 + 80	_	ns
SCK↓→ valid SIN hold time	t _{SLIXI}	SCK, SIN		0	_	ns
Serial clock "H" pulse width	t _{SHSL}	SCK		3 t _{MCLK} *3 – t _R	_	ns
Serial clock "L" pulse width	t _{SLSH}	SCK		t _{MCLK} *3 + 10	_	ns
$SCK^{\uparrow} \rightarrow SOT$ delay time	t _{SHOVE}	SCK, SOT	External clock operation	_	2 t _{MCLK} *3 + 60	ns
Valid SIN \rightarrow SCK↓	t _{IVSLE}	SCK, SIN	output pin:	30	_	ns
$SCK \downarrow \rightarrow valid SIN hold time$	t _{SLIXE}	SCK, SIN	C _L = 80 pF + 1 TTL	t _{MCLK} *3 + 30	_	ns
SCK fall time	t _F	SCK			10	ns
SCK rise time	t _R	SCK		_	10	ns

^{*1:} There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

^{*2:} The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

^{*3:} See "18.4.2. Source Clock/Machine Clock" for t_{MCLK}.

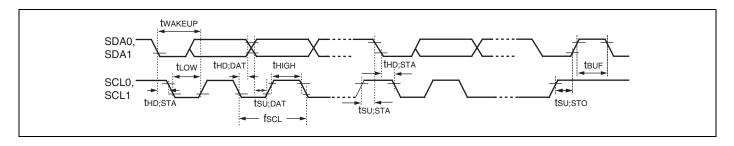


18.4.8 I²C Bus Interface Timing

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

				Value				
Parameter	Symbol	Pin name	Condition	Standa	d-mode	Fast-	mode	Unit
				Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	SCL0, SCL1		0	100	0	400	kHz
(Repeated) START condition hold time SDA \downarrow \rightarrow SCL \downarrow	t _{HD;STA}	SCL0, SCL1, SDA0, SDA1		4.0	_	0.6	_	μs
SCL clock "L" width	t _{LOW}	SCL0, SCL1		4.7	_	1.3	_	μs
SCL clock "H" width	t _{HIGH}	SCL0, SCL1		4.0	_	0.6	_	μs
(Repeated) START condition setup time SCL $\uparrow \rightarrow$ SDA \downarrow	t _{SU;STA}	SCL0, SCL1, SDA0, SDA1	R = 1.7 kΩ,	4.7	_	0.6	_	μs
Data hold time $SCL \downarrow \rightarrow SDA \downarrow \uparrow$	t _{HD;DAT}	SCL0, SCL1, SDA0, SDA1		0	3.45 ^{*2}	0	0.9*3	μs
Data setup time SDA $\downarrow\uparrow$ \rightarrow SCL \uparrow	t _{SU;DAT}	SCL0, SCL1, SDA0, SDA1		0.25	_	0.1	_	μs
STOP condition setup time SCL $\uparrow \rightarrow$ SDA \uparrow	t _{su;sto}	SCL0, SCL1, SDA0, SDA1		4	_	0.6	_	μs
Bus free time between STOP condition and START condition	t _{BUF}	SCL0, SCL1, SDA0, SDA1		4.7	_	1.3	_	μs

- *1: R represents the pull-up resistor of the SCL0/1 and SDA0/1 lines, and C the load capacitor of the SCL0/1 and SDA0/1 lines.
- *2: The maximum $t_{\text{HD;DAT}}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at "L" (t_{LOW}) does not extend.
- *3: A Fast-mode I^2C -bus device can be used in a Standard-mode I^2C -bus system, provided that the condition of $t_{SU;DAT} \ge 250$ ns is fulfilled.





18.5.3 Definitions of A/D Converter Terms

Resolution

It indicates the level of analog variation that can be distinguished by the A/D converter.

When the number of bits is 12, analog voltage can be divided into 2^{12} = 4096.

Linearity error (unit: LSB)

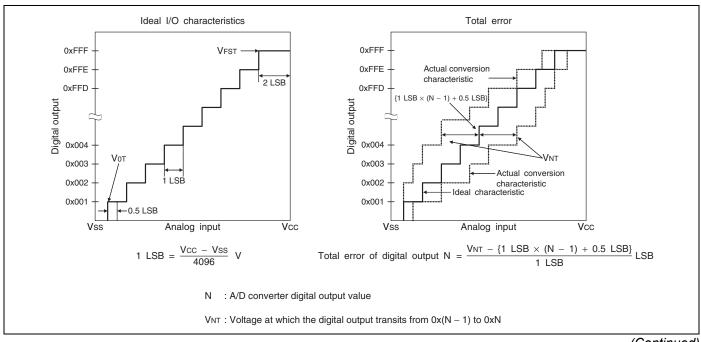
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("00000000000" $\leftarrow \rightarrow$ "000000000001") of a device to the full-scale transition point ("111111111111" $\leftarrow \rightarrow$ "111111111110") of the same device.

Differential linear error (unit: LSB)

It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.

Total error (unit: LSB)

It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.





20. Mask Options

No.	Part number	MB95F652E MB95F653E MB95F654E MB95F656E	MB95F652L MB95F653L MB95F654L MB95F656L
	Selectable/Fixed	Fix	red
1	Low-voltage detection reset/interrupt	IVVith low-voltage detection reset/interript	Without low-voltage detection reset/interrupt
2	Reset	Without dedicated reset input	With dedicated reset input



21. Ordering Information

Part number	Package
MB95F652EPFT-G-SNE2 MB95F652LPFT-G-SNE2 MB95F653EPFT-G-SNE2 MB95F653LPFT-G-SNE2 MB95F654EPFT-G-SNE2 MB95F654LPFT-G-SNE2 MB95F656EPFT-G-SNE2 MB95F656EPFT-G-SNE2	24-pin plastic TSSOP (FPT-24P-M10)
MB95F652EPF-G-SNE2 MB95F652LPF-G-SNE2 MB95F653EPF-G-SNE2 MB95F653LPF-G-SNE2 MB95F654EPF-G-SNE2 MB95F654LPF-G-SNE2 MB95F656EPF-G-SNE2 MB95F656LPF-G-SNE2	24-pin plastic SOP (FPT-24P-M34)
MB95F652EWQN-G-SNE1 MB95F652EWQN-G-SNERE1 MB95F652LWQN-G-SNERE1 MB95F652LWQN-G-SNERE1 MB95F653EWQN-G-SNERE1 MB95F653EWQN-G-SNERE1 MB95F653LWQN-G-SNERE1 MB95F653LWQN-G-SNERE1 MB95F654EWQN-G-SNERE1 MB95F654EWQN-G-SNERE1 MB95F654LWQN-G-SNERE1 MB95F656EWQN-G-SNERE1 MB95F656EWQN-G-SNERE1 MB95F656EWQN-G-SNERE1 MB95F656EWQN-G-SNERE1 MB95F656LWQN-G-SNERE1 MB95F656LWQN-G-SNERE1 MB95F656LWQN-G-SNERE1	32-pin plastic QFN (LCC-32P-M19)



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Revision	ECN	Orig. of Change	Submission Date	Description of Change	
**	_	AKIH	06/14/2013	Migrated to Cypress and assigned document number 002-04696. No change to document contents or format.	
*A	5216808	AKIH	04/12/2016	Updated to Cypress format.	
*B	5846146	YSAT	08/07/2017	Adapted new Cypress logo	

Document Number: 002-04696 Rev. *B



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