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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	20
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x8/12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	24-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f656lpft-g-sne2

MB95650L Series

New 8FX 8-bit Microcontrollers

The MB95650L Series is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral functions.

Features

F²MC-8FX CPU core

Instruction set optimized for controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- Bit test branch instructions
- Bit manipulation instructions, etc.

Clock

- Selectable main clock source
  - Main oscillation clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
  - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
  - Main CR clock (4 MHz ±2%)
  - Main CR PLL clock
    - The main CR PLL clock frequency becomes 8 MHz ±2% when the PLL multiplication rate is 2.
    - The main CR PLL clock frequency becomes 10 MHz ±2% when the PLL multiplication rate is 2.5.
    - The main CR PLL clock frequency becomes 12 MHz ±2% when the PLL multiplication rate is 3.
    - The main CR PLL clock frequency becomes 16 MHz ±2% when the PLL multiplication rate is 4.
  - Main PLL clock (maximum machine clock frequency: 16 MHz)
- Selectable subclock source
  - Suboscillation clock (32.768 kHz)
  - External clock (32.768 kHz)
  - Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 150 kHz)

Timer

- 8/16-bit composite timer × 2 channels
- Time-base timer × 1 channel
- Watch prescaler × 1 channel

UART/SIO × 1 channel (The channel can be used either as a UART/SIO channel or as an I²C bus interface channel.)

- The function of this channel can be switched between UART/SIO and I²C bus interface.
- Full duplex double buffer
- Capable of clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer

I²C bus interface × 2 channels (One of the two channels can be used either as an I²C bus interface channel or as a UART/SIO channel.)

- Supports Standard-mode and Fast-mode (400 kHz).
- Built-in wake-up function

LIN-UART

- Full duplex double buffer
- Capable of clock asynchronous serial data transfer and clock synchronous serial data transfer

External interrupt × 6 channels

- Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
- Can be used to wake up the device from different low power consumption (standby) modes

8/12-bit A/D converter × 6 channels

8-bit or 12-bit resolution can be selected.

Low power consumption (standby) modes

There are four standby modes as follows:

- Stop mode
- Sleep mode
- Watch mode
- Time-base timer mode

I/O port

- MB95F652E/F653E/F654E/F656E (number of I/O ports: 21)
  - General-purpose I/O ports (CMOS I/O) : 17
  - General-purpose I/O ports (N-ch open drain) : 4
- MB95F652L/F653L/F654L/F656L (number of I/O ports: 20)
  - General-purpose I/O ports (CMOS I/O) : 17
  - General-purpose I/O ports (N-ch open drain) : 3

On-chip debug

- 1-wire serial control
- Serial writing supported (asynchronous mode)

Hardware/software watchdog timer

- Built-in hardware watchdog timer
- Built-in software watchdog timer

Pin no.		Pin name	I/O circuit type*4	Function	I/O type			
SOP24*1, TSSOP24*2	QFN32*3				Input	Output	OD*5	PU*6
16	18	P00	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		AN00		8/12-bit A/D converter analog input pin				
17	18	P01	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		AN01		8/12-bit A/D converter analog input pin				
18	20	P02	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT02		External interrupt input pin				
		AN02		8/12-bit A/D converter analog input pin				
		SCK		LIN-UART clock I/O pin				
19	21	P03	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT03		External interrupt input pin				
		AN03		8/12-bit A/D converter analog input pin				
		SOT		LIN-UART data output pin				
20	22	P04	F	General-purpose I/O port	CMOS/ analog	CMOS	—	O
		INT04		External interrupt input pin				
		AN04		8/12-bit A/D converter analog input pin				
		SIN		LIN-UART data input pin				
		EC0		8/16-bit composite timer ch. 0 clock input pin				
21	23	P05	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
		INT05		External interrupt input pin				
		AN05		8/12-bit A/D converter analog input pin				
		TO00		8/16-bit composite timer ch. 0 output pin				
22	24	P06	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		INT06		External interrupt input pin				
		TO01		8/16-bit composite timer ch. 0 output pin				
23	26	P07	K	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		INT07		External interrupt input pin				
		TO10		8/16-bit composite timer ch. 1 output pin				

(Continued)

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Pin no.		Pin name	I/O circuit type*4	Function	I/O type			
SOP24*1, TSSOP24*2	QFN32*3				Input	Output	OD*5	PU*6
24	25	P12	H	General-purpose I/O port	Hysteresis	CMOS	O	—
		DBG		DBG input pin				
		EC0		8/16-bit composite timer ch. 0 clock input pin				
—	11	NC	—	It is an internally connected pin. Always leave it unconnected.	—	—	—	—
	12							
	13							
	14							
	27							
	28							
	29							
	30							

O: Available

*1: FPT-24P-M34

*2: FPT-24P-M10

*3: LCC-32P-M19

*4: For the I/O circuit types, see “6. I/O Circuit Type”.

*5: N-ch open drain

*6: Pull-up

*7: In I^2C mode, the pin becomes an N-ch open drain pin.

9. Pin Connection

Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 1.0 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

DBG pin

Connect the DBG pin to an external pull-up resistor of 2 kΩ or above.

After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released.

The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

$\overline{\text{RST}}$ pin

Connect the $\overline{\text{RST}}$ pin to an external pull-up resistor of 2 kΩ or above.

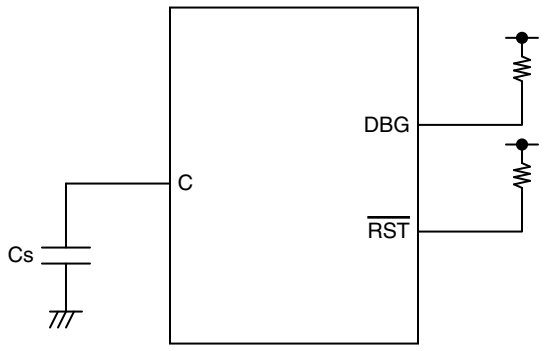
To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the $\overline{\text{RST}}$ pin and that between a pull-up resistor and the V_{CC} pin when designing the layout of the printed circuit board.

The PF2/$\overline{\text{RST}}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/$\overline{\text{RST}}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

C pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

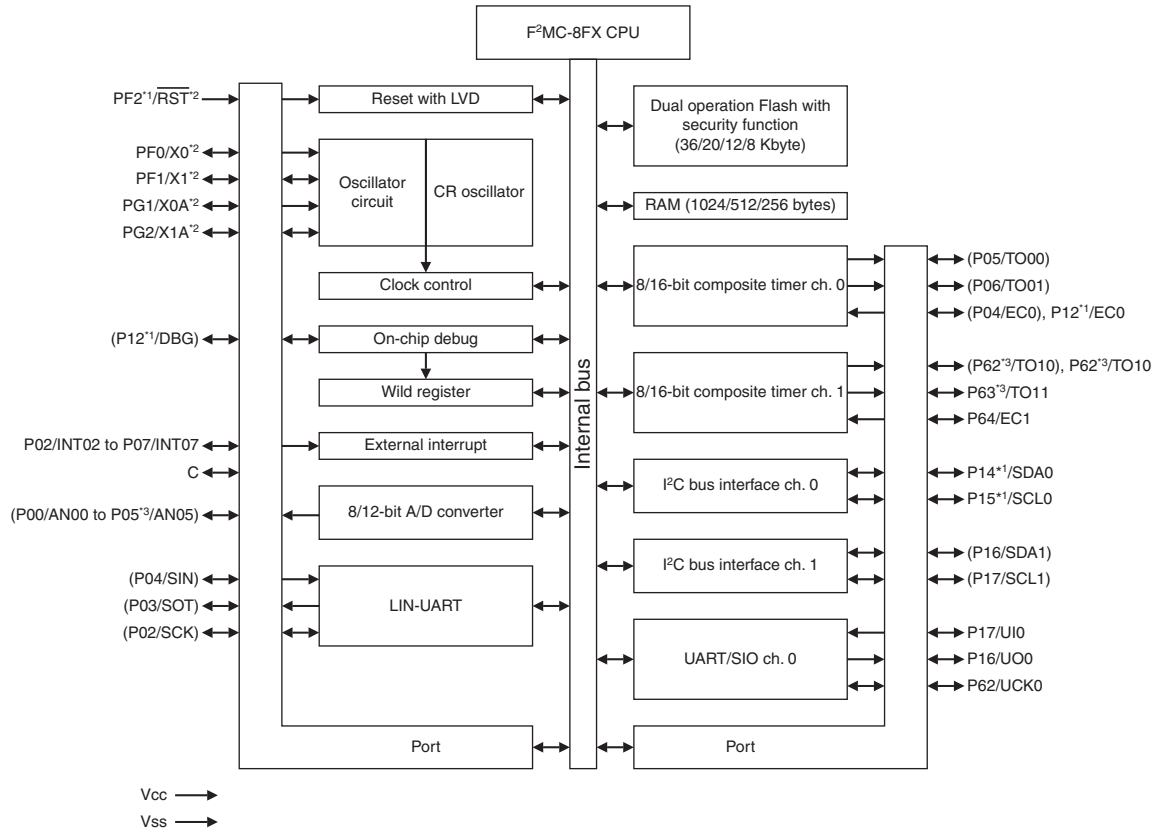
DBG/$\overline{\text{RST}}$/C pins connection diagram



Note on serial communication

In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, take measures such as adding a checksum to the end of data in order to detect errors. If an error is detected, retransmit the data.

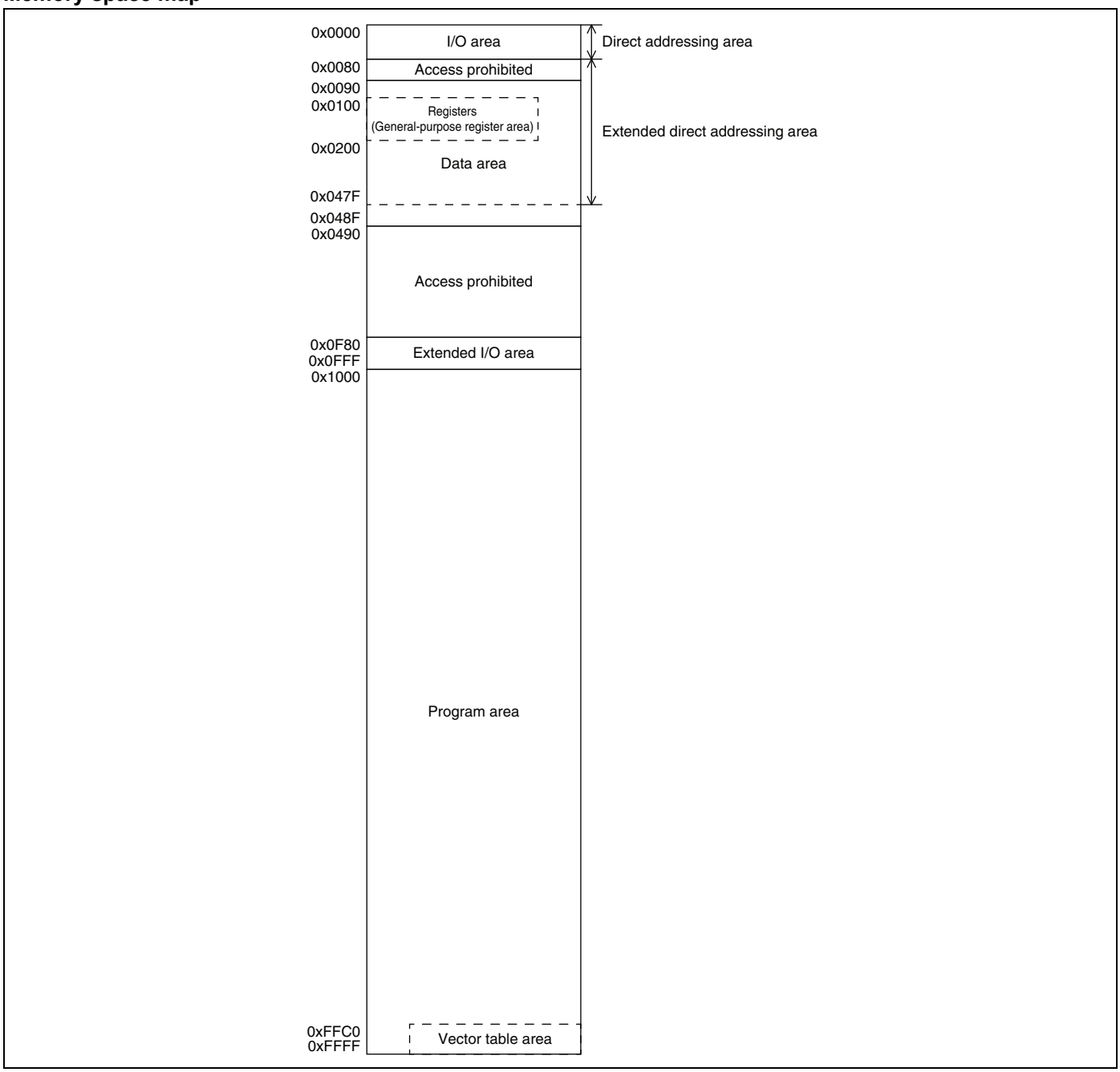
10. Block Diagram



*1: P12, P14, P15 and PF2 are N-ch open drain pins.
*2: Software select
*3: P05 to P07, P62 and P63 are high-current pins.

Note: Pins in parentheses indicate that those pins are shared among different peripheral functions.

Memory space map



15.2.3 Port 1 registers

Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR1	0	Pin state is “L” level.	PDR1 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR1 value is “1”.	As output port, outputs “H” level.*
DDR1	0	Port input enabled		
	1	Port output enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

Correspondence between registers and pins for port 1

	Correspondence between related register bits and pins							
Pin name	**P17**	**P16**	**P15**	**P14**	**-**	**P12**	**-**	**-**
PDR1	bit7	bit6	bit5	bit4	-	bit2	-	-
DDR1								

17. Pin States in each Mode

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
PF0/X0	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PF1/X1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PF2/$\overline{\text{RST}}$	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input*4
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PG1/X0A	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PG2/X1A	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
P00/AN00	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked*2, *5	- Hi-Z*6 - Input blocked*2, *5	- Previous state kept - Input blocked*2, *5	- Hi-Z*6 - Input blocked*2, *5	- Hi-Z - Input blocked*2
P01/AN01							
P02/INT02/ AN02/SCK							
P03/INT03/ AN03/SOT							
P04/INT04/ AN04/SIN/ EC0							
P05/INT05/ AN05/TO00							

18. Electrical Characteristics

18.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} − 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	−2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
"L" level maximum output current	I_{OL}	—	15	mA	
"L" level average current	I_{OLAV1}	—	4	mA	Other than P05 to P07, P62 and P63 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P05 to P07, P62 and P63 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	37	mA	Total average output current = operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH}	—	−15	mA	
"H" level average current	I_{OHAV1}	—	−4	mA	Other than P05 to P07, P62 and P63 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		−8		P05 to P07, P62 and P63 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	−100	mA	
"H" level total average output current	ΣI_{OHAV}	—	−47	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	−40	+85	°C	
Storage temperature	T_{stg}	−55	+150	°C	

*1: These parameters are based on the condition that V_{SS} is 0.0 V.

*2: V_1 and V_0 must not exceed V_{CC} + 0.3 V. V_1 must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

(Continued)

18.3 DC Characteristics

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI1}	P04, P16, P17	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input level
	V_{IHI2}	P14, P15	*1	0.7 V_{CC}	—	V_{CC} + 5.5	V	CMOS input level
	V_{IHS}	P00 to P03, P05 to P07, P12, P62 to P64, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{ILI}	P04, P14 to P17	*1	V_{SS} − 0.3	—	0.3 V_{CC}	V	CMOS input level
	V_{ILS}	P00 to P03, P05 to P07, P12, P62 to P64, PF0, PF1, PG1, PG2	*1	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_{D1}	P12, PF2	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	
	V_{D2}	P14, P15	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	
	V_{D3}	P16, P17	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	In I^2C mode
"H" level output voltage	V_{OH1}	Output pins other than P05 to P07, P12, P62, P63	I_{OH} = −4 mA*2	V_{CC} − 0.5	—	—	V	
	V_{OH2}	P05 to P07, P62, P63	I_{OH} = −8 mA*3	V_{CC} − 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P05 to P07, P62, P63	I_{OL} = 4 mA*4	—	—	0.4	V	
	V_{OL2}	P05 to P07, P62, P63	I_{OL} = 12 mA*5	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	−5	—	+5	µA	When the internal pull-up resistor is disabled
Internal pull-up resistor	R_{PULL}	P00 to P07, P62 to P64, PG1, PG2	V_I = 0 V	75	100	150	kΩ	When the internal pull-up resistor is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

(Continued)

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*1	Max*6		
Power supply current*7	I_{CCTS}	V_{CC} (External clock operation)	F_{CH} = 32 MHz Time-base timer mode T_A = +25 °C	—	450	500	µA	
	I_{CCH}		Substop mode T_A = +25 °C	—	0.7	5	µA	
	I_{PLVD}	V_{CC}	Current consumption of the low-voltage detection reset circuit in operation	—	6	26	µA	
	I_{ILVD}		Current consumption of the low-voltage detection interrupt circuit operating in normal mode	—	6	14	µA	
	I_{ILVDL}		Current consumption of the low-voltage detection interrupt circuit operating in low power consumption mode	—	3	10	µA	
	I_{CRH}		Current consumption of the main CR oscillator	—	270	320	µA	
	I_{CRL}		Current consumption of the sub-CR oscillator oscillating at 100 kHz	—	5	20	µA	
	I_{SOSC}		Current consumption of the suboscillator	—	0.8	7	µA	

*1: V_{CC} = 3.0 V, T_A = +25 °C

*2: When V_{CC} is smaller than 4.5 V, the condition becomes I_{OH} = –2 mA.

*3: When V_{CC} is smaller than 4.5 V, the condition becomes I_{OH} = –4 mA.

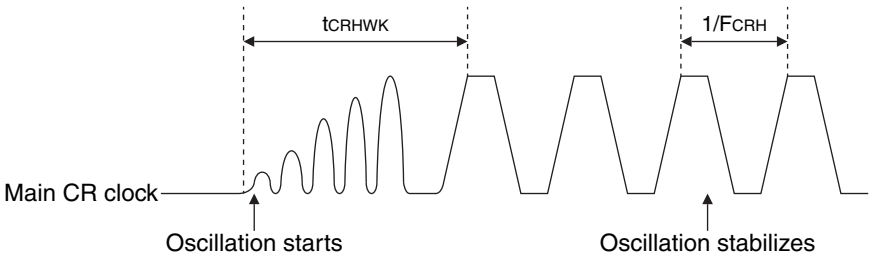
*4: When V_{CC} is smaller than 4.5 V, the condition becomes I_{OL} = 2 mA.

*5: When V_{CC} is smaller than 4.5 V, the condition becomes I_{OH} = 6 mA.

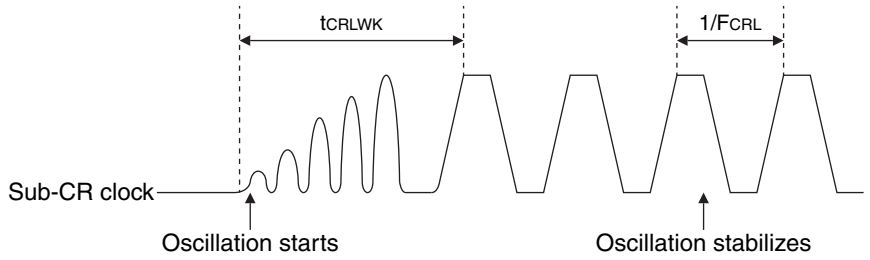
*6: V_{CC} = 3.3 V, T_A = +85 °C (unless otherwise specified)

*7:
- The power supply current is determined by the external clock. When the low-voltage detection reset circuit is selected, the power supply current is the sum of adding the current consumption of the low-voltage detection reset circuit (I_{PLVD}) to one of the values from I_{CC} to I_{CCH}. In addition, when the low-voltage detection reset circuit and a CR oscillator are selected, the power supply current is the sum of adding up the current consumption of the low-voltage detection reset circuit (I_{PLVD}), the current consumption of the CR oscillator (I_{CRH} or I_{CRL}) and one of the values from I_{CC} to I_{CCH}. In on-chip debug mode, the main CR oscillator (I_{CRH}) and the low-voltage detection reset circuit are always in operation, and current consumption therefore increases accordingly.
- See “18.4. AC Characteristics 18.4.1. Clock Timing” for F_{CH}, F_{CL}, F_{CRH}, F_{MCRPLL} and F_{MPLL}.
- See “18.4. AC Characteristics 18.4.2. Source Clock/Machine Clock” for F_{MP} and F_{MPL}.
- The power supply current in subclock mode is determined by the external clock. In subclock mode, current consumption in using the crystal oscillator is higher than that in using the external clock. When the crystal oscillator is used, the power supply current is the sum of adding I_{SOSC} (current consumption of the suboscillator) to the power supply current in using the external clock. For details of controlling the subclock, refer to “Chapter 3 Clock Controller” And “chapter 24 System Configuration Register” in “New 8FX MB95650L Series Hardware Manual”.

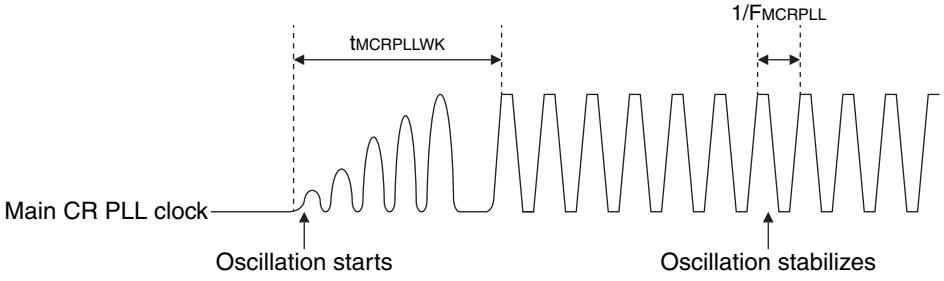
Input waveform generated when an internal clock (main CR clock) is used



Input waveform generated when an internal clock (sub-CR clock) is used



Input waveform generated when an internal clock (main CR PLL clock) is used



18.4.6 LIN-UART Timing

*Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2.*
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3–t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 10	—	ns
SCK↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 60	ns
Valid SIN → SCK↑	t_{IVSHE}	SCK, SIN		30	—	ns
SCK↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 30	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.

18.4.7 Low-vo ltage Detection

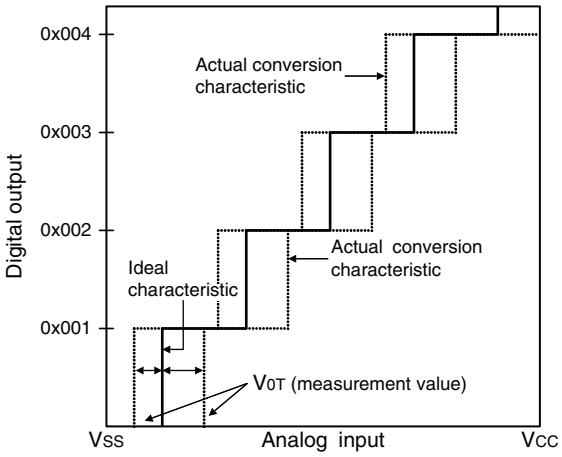
Normal mode

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

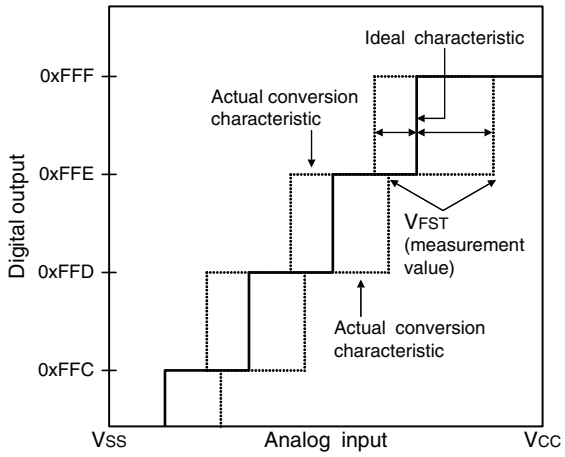
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Reset release voltage	V_{PDL+}	1.88	2.03	2.18	V	At power supply rise
Reset detection voltage	$V_{PDL–}$	1.8	1.93	2.06	V	At power supply fall
Interrupt release voltage 0	V_{IDL0+}	2.13	2.3	2.47	V	At power supply rise
Interrupt detection voltage 0	$V_{IDL0–}$	2.05	2.2	2.35	V	At power supply fall
Interrupt release voltage 1	V_{IDL1+}	2.41	2.6	2.79	V	At power supply rise
Interrupt detection voltage 1	$V_{IDL1–}$	2.33	2.5	2.67	V	At power supply fall
Interrupt release voltage 2	V_{IDL2+}	2.69	2.9	3.11	V	At power supply rise
Interrupt detection voltage 2	$V_{IDL2–}$	2.61	2.8	2.99	V	At power supply fall
Interrupt release voltage 3	V_{IDL3+}	3.06	3.3	3.54	V	At power supply rise
Interrupt detection voltage 3	$V_{IDL3–}$	2.98	3.2	3.42	V	At power supply fall
Interrupt release voltage 4	V_{IDL4+}	3.43	3.7	3.97	V	At power supply rise
Interrupt detection voltage 4	$V_{IDL4–}$	3.35	3.6	3.85	V	At power supply fall
Interrupt release voltage 5	V_{IDL5+}	3.81	4.1	4.39	V	At power supply rise
Interrupt detection voltage 5	$V_{IDL5–}$	3.73	4	4.27	V	At power supply fall
Power supply start voltage	V_{off}	—	—	1.6	V	
Power supply end voltage	V_{on}	4.39	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	697.5	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{PDL+}/V_{IDL+})
Power supply voltage change time (at power supply fall)	t_f	697.5	—	—	µs	Slope of power supply that the reset release signal generates within the rating ($V_{PDL–}$/$V_{IDL–}$)
Reset release delay time	t_{dp1}	—	—	30	µs	
Reset detection delay time	t_{dp2}	—	—	30	µs	
Interrupt release delay time	t_{di1}	—	—	30	µs	
Interrupt detection delay time	t_{di2}	—	—	30	µs	
LVD reset threshold voltage transition stabilization time	t_{stb}	—	—	30	µs	

(Continued)

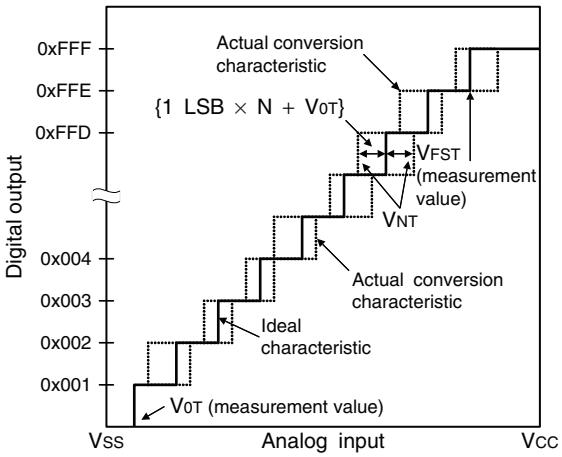
Zero transition error



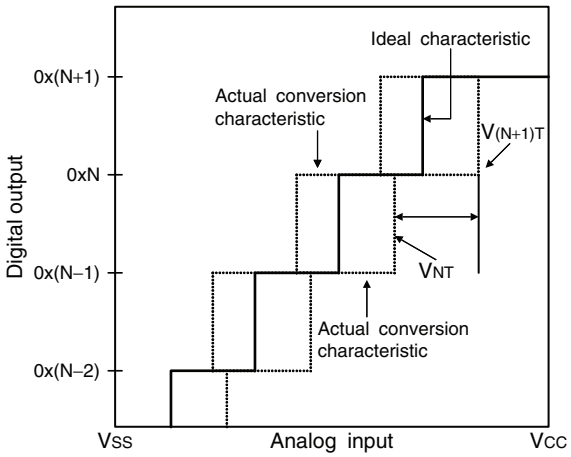
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} – 2 LSB [V]

18.6 Flash Memory Program/Erase Characteristics

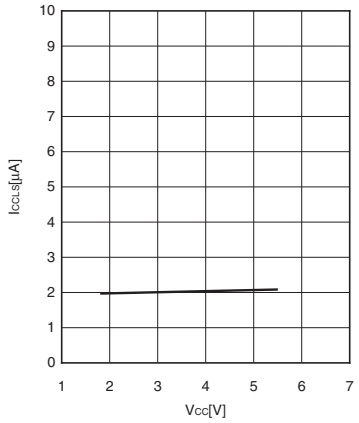
Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.3*1	1.6*2	s	The time of writing “0x00” prior to erasure is excluded.
Sector erase time (32 Kbyte sector)	—	0.6*1	3.1*2	s	The time of writing “0x00” prior to erasure is excluded.
Byte writing time	—	17	272	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	1.8	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85 °C Number of program/erase cycles: 1000 or below
	10*3	—	—		Average T_A = +85 °C Number of program/erase cycles: 1001 to 10000 inclusive
	5*3	—	—		Average T_A = +85 °C Number of program/erase cycles: 10001 or above

*1: V_{CC} = 5.5 V, T_A = +25 °C, 0 cycle

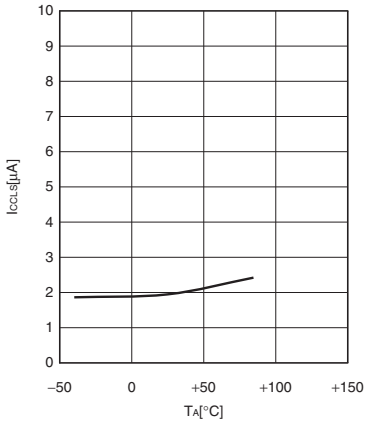
*2: V_{CC} = 1.8 V, T_A = +85 °C, 100000 cycles

*3: These values were converted from the result of a technology reliability assessment. (These values were converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85 °C.)

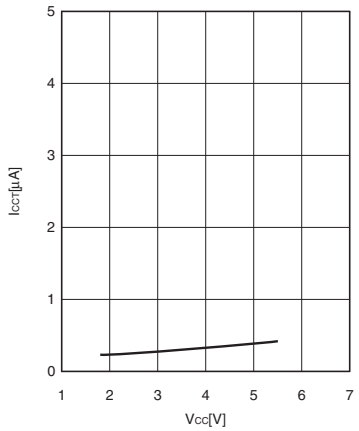
I_{CCLS} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



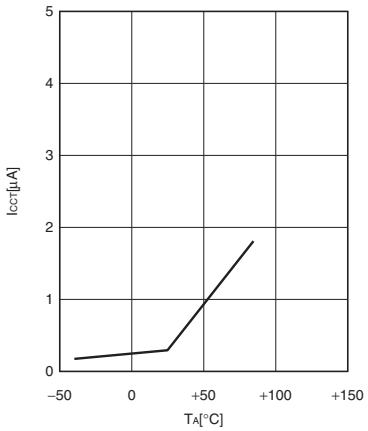
I_{CCLS} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



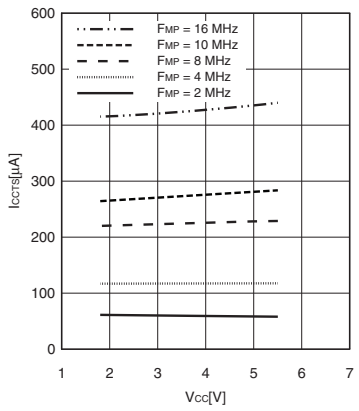
I_{CCT} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



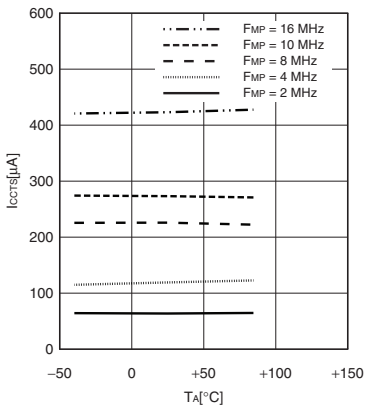
I_{CCT} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



I_{CCTS} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating

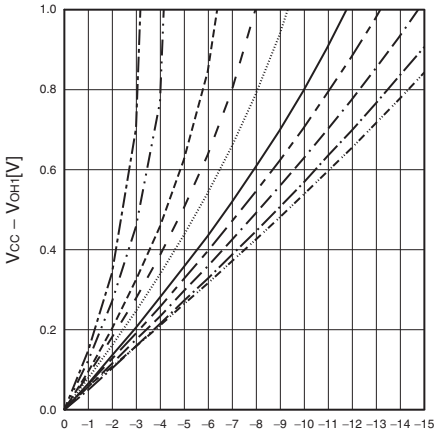


I_{CCTS} – T_A
V_{CC} = 3.3 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



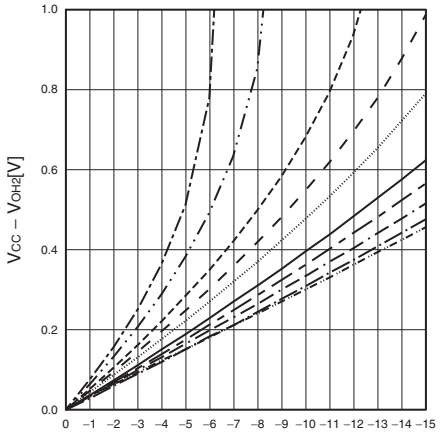
Output voltage characteristics

$(V_{CC} - V_{OH1}) - I_{OH}$
$T_A = +25\ °C$



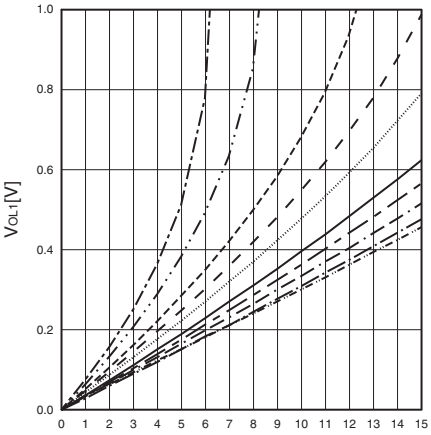
VCC = 1.8 V
VCC = 2.0 V
VCC = 2.4 V
VCC = 2.7 V
VCC = 3.0 V
VCC = 3.6 V
VCC = 4.0 V
VCC = 4.5 V
VCC = 5.0 V
VCC = 5.5 V

$(V_{CC} - V_{OH2}) - I_{OH}$
$T_A = +25\ °C$



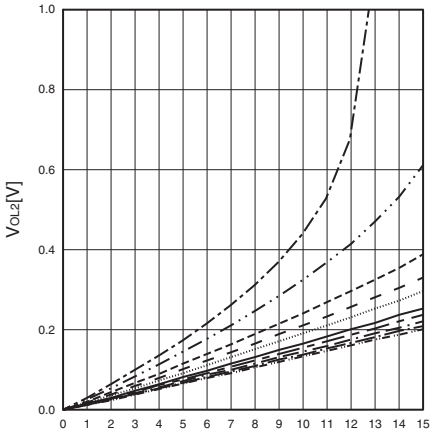
VCC = 1.8 V
VCC = 2.0 V
VCC = 2.4 V
VCC = 2.7 V
VCC = 3.0 V
VCC = 3.6 V
VCC = 4.0 V
VCC = 4.5 V
VCC = 5.0 V
VCC = 5.5 V

$V_{OL1} - I_{OL}$
$T_A = +25\ °C$



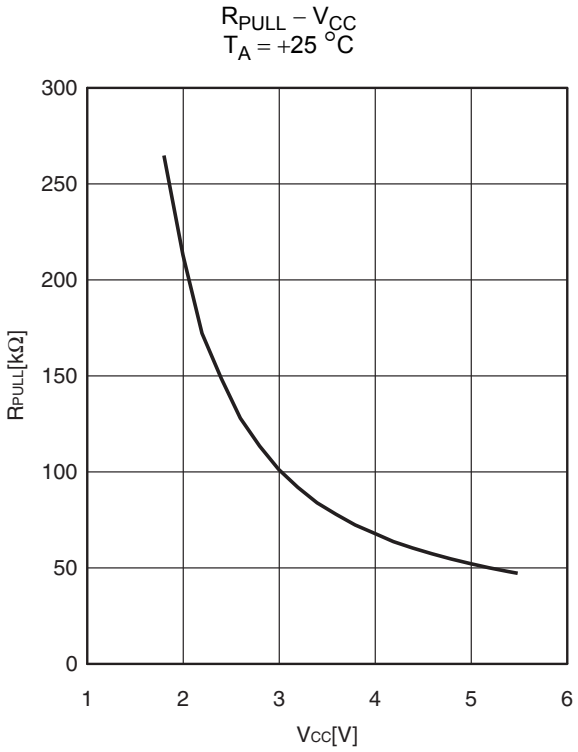
VCC = 1.8 V
VCC = 2.0 V
VCC = 2.4 V
VCC = 2.7 V
VCC = 3.0 V
VCC = 3.6 V
VCC = 4.0 V
VCC = 4.5 V
VCC = 5.0 V
VCC = 5.5 V

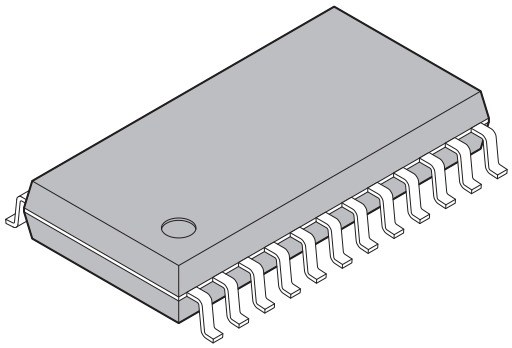
$V_{OL2} - I_{OL}$
$T_A = +25\ °C$



VCC = 1.8 V
VCC = 2.0 V
VCC = 2.4 V
VCC = 2.7 V
VCC = 3.0 V
VCC = 3.6 V
VCC = 4.0 V
VCC = 4.5 V
VCC = 5.0 V
VCC = 5.5 V

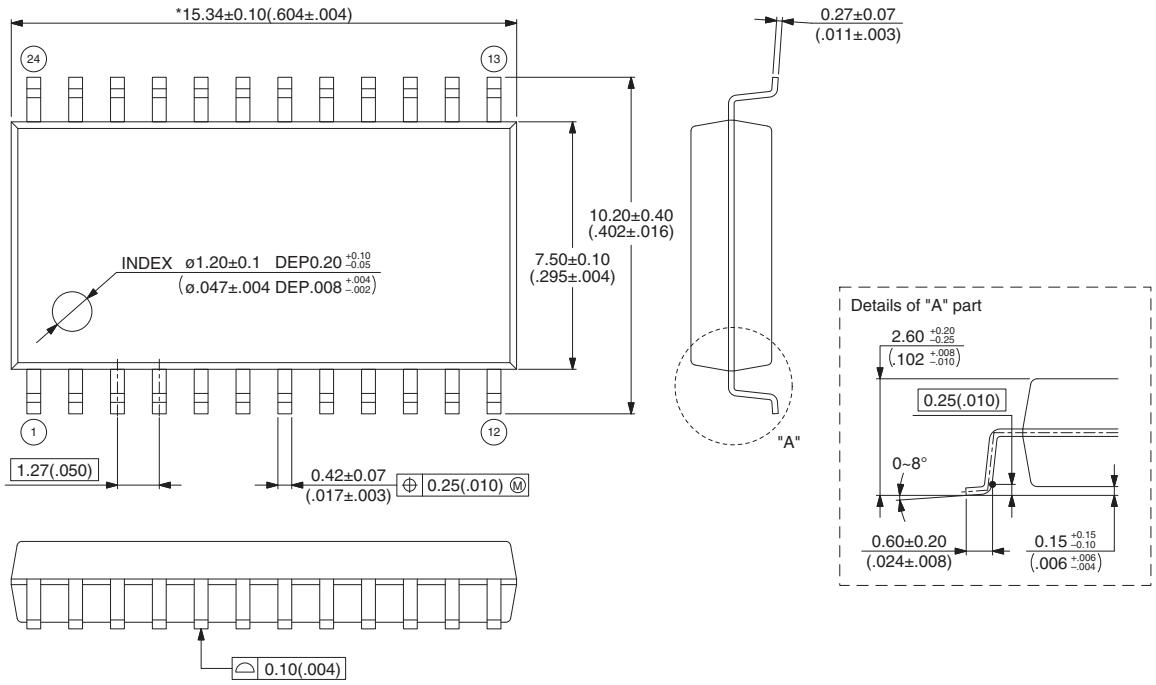
Pull-up characteristics



24-pin plastic SOP		
	Lead pitch	1.27 mm
	Package width × package length	7.50 mm × 15.34 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	2.80 mm MAX
(FPT-24P-M34)	Weight	0.44 g

24-pin plastic SOP
(FPT-24P-M34)

Note 1) * : These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)