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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	20
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x8/12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f656lwqn-g-sne1

1. Product Line-up

Part number / Parameter	MB95F652E	MB95F653E	MB95F654E	MB95F656E	MB95F652L	MB95F653L	MB95F654L	MB95F656L
Type	Flash memory product							
Clock supervisor counter	It supervises the main clock oscillation and the subclock oscillation.							
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	36 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte	36 Kbyte
RAM capacity	256 bytes	512 bytes	1024 bytes	1024 bytes	256 bytes	512 bytes	1024 bytes	1024 bytes
Power-on reset	Yes							
Low-voltage detection reset	Yes				No			
Reset input	Selected through software				With dedicated reset input			
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)							
General-purpose I/O	• I/O port : 21 • CMOS I/O : 17 • N-ch open drain : 4				• I/O port : 20 • CMOS I/O : 17 • N-ch open drain : 3			
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)							
Hardware/software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the software watchdog timer.							
Wild register	It can be used to replace 3 bytes of data.							
LIN-UART	• A wide range of communication speed can be selected by a dedicated reload timer. • It has a full duplex double buffer. • Both clock synchronous serial data transfer and clock asynchronous serial data transfer are enabled. • The LIN function can be used as a LIN master or a LIN slave.							
8/12-bit A/D converter	6 channels							
	8-bit or 12-bit resolution can be selected.							
8/16-bit composite timer	2 channels							
	• The timer can be configured as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”. • It has the following functions: interval timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.							
External interrupt	6 channels							
	• Interrupt by edge detection (The rising edge, falling edge, and both edges can be selected.) • It can be used to wake up the device from different standby modes.							
On-chip debug	• 1-wire serial control • It supports serial writing (asynchronous mode).							

(Continued)

Pin no.		Pin name	I/O circuit type*4	Function	I/O type			
SOP24*1, TSSOP24*2	QFN32*3				Input	Output	OD*5	PU*6
16	18	P00	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		AN00		8/12-bit A/D converter analog input pin				
17	18	P01	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		AN01		8/12-bit A/D converter analog input pin				
18	20	P02	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT02		External interrupt input pin				
		AN02		8/12-bit A/D converter analog input pin				
		SCK		LIN-UART clock I/O pin				
19	21	P03	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT03		External interrupt input pin				
		AN03		8/12-bit A/D converter analog input pin				
		SOT		LIN-UART data output pin				
20	22	P04	F	General-purpose I/O port	CMOS/ analog	CMOS	—	O
		INT04		External interrupt input pin				
		AN04		8/12-bit A/D converter analog input pin				
		SIN		LIN-UART data input pin				
		EC0		8/16-bit composite timer ch. 0 clock input pin				
21	23	P05	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
		INT05		External interrupt input pin				
		AN05		8/12-bit A/D converter analog input pin				
		TO00		8/16-bit composite timer ch. 0 output pin				
22	24	P06	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		INT06		External interrupt input pin				
		TO01		8/16-bit composite timer ch. 0 output pin				
23	26	P07	K	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		INT07		External interrupt input pin				
		TO10		8/16-bit composite timer ch. 1 output pin				

(Continued)

(Continued)

Pin no.		Pin name	I/O circuit type*4	Function	I/O type			
SOP24*1, TSSOP24*2	QFN32*3				Input	Output	OD*5	PU*6
24	25	P12	H	General-purpose I/O port	Hysteresis	CMOS	O	—
		DBG		DBG input pin				
		EC0		8/16-bit composite timer ch. 0 clock input pin				
—	11	NC	—	It is an internally connected pin. Always leave it unconnected.	—	—	—	—
	12							
	13							
	14							
	27							
	28							
	29							
	30							

O: Available

*1: FPT-24P-M34

*2: FPT-24P-M10

*3: LCC-32P-M19

*4: For the I/O circuit types, see “6. I/O Circuit Type”.

*5: N-ch open drain

*6: Pull-up

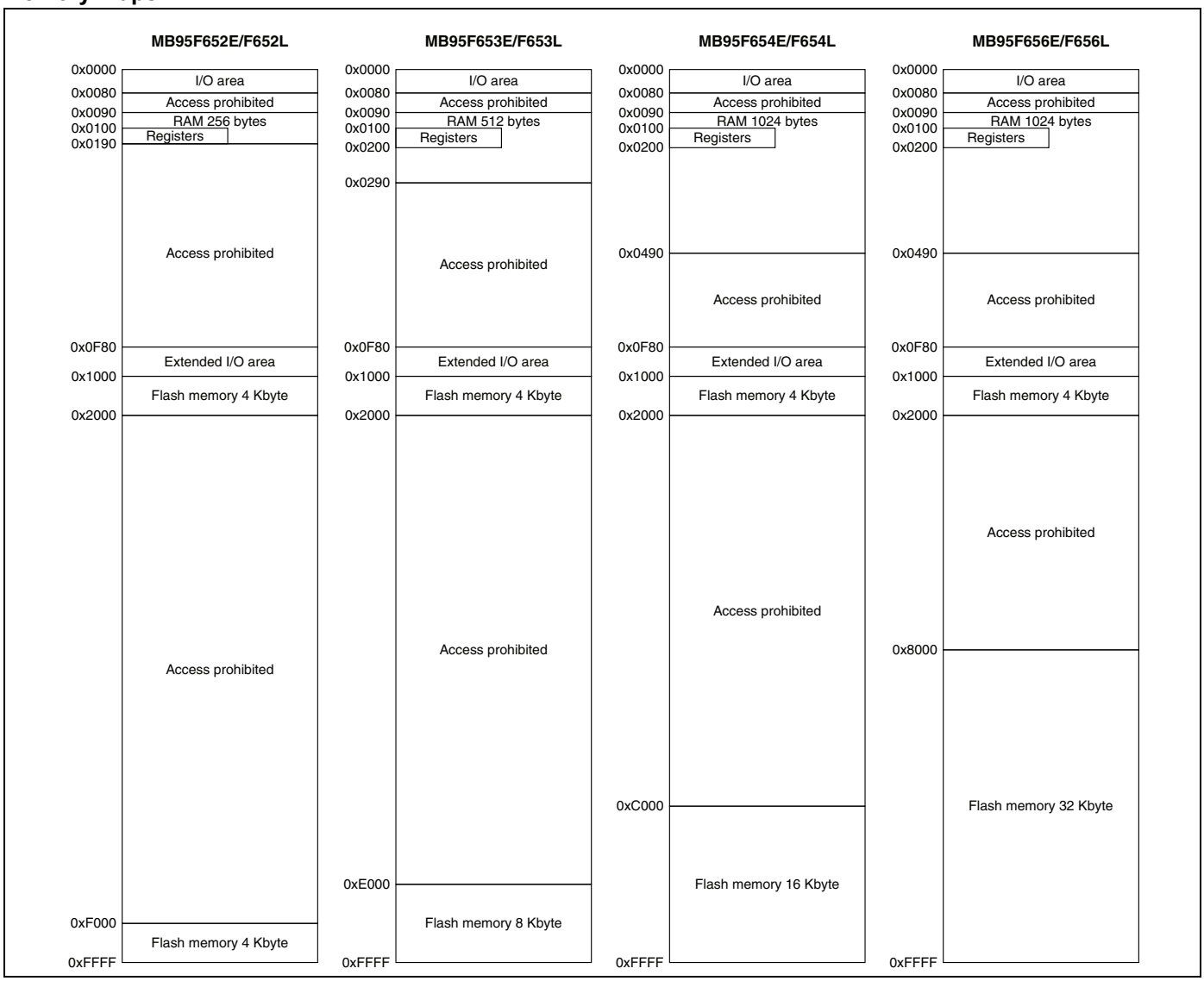
*7: In I^2C mode, the pin becomes an N-ch open drain pin.

11. CPU Core

Memory space

The memory space of the MB95650L Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95650L Series are shown below.

Memory maps



12. Memory Space

The memory space of the MB95650L Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas for specific applications such as general-purpose registers and a vector table.

I/O area (addresses: 0x0000 to 0x007F)

- This area contains the control registers and data registers for built-in peripheral functions.
- As the I/O area forms part of the memory space, it can be accessed in the same way as the memory. It can also be accessed at high-speed by using direct addressing instructions.

Extended I/O area (addresses: 0x0F80 to 0x0FFF)

- This area contains the control registers and data registers for built-in peripheral functions.
- As the extended I/O area forms part of the memory space, it can be accessed in the same way as the memory.

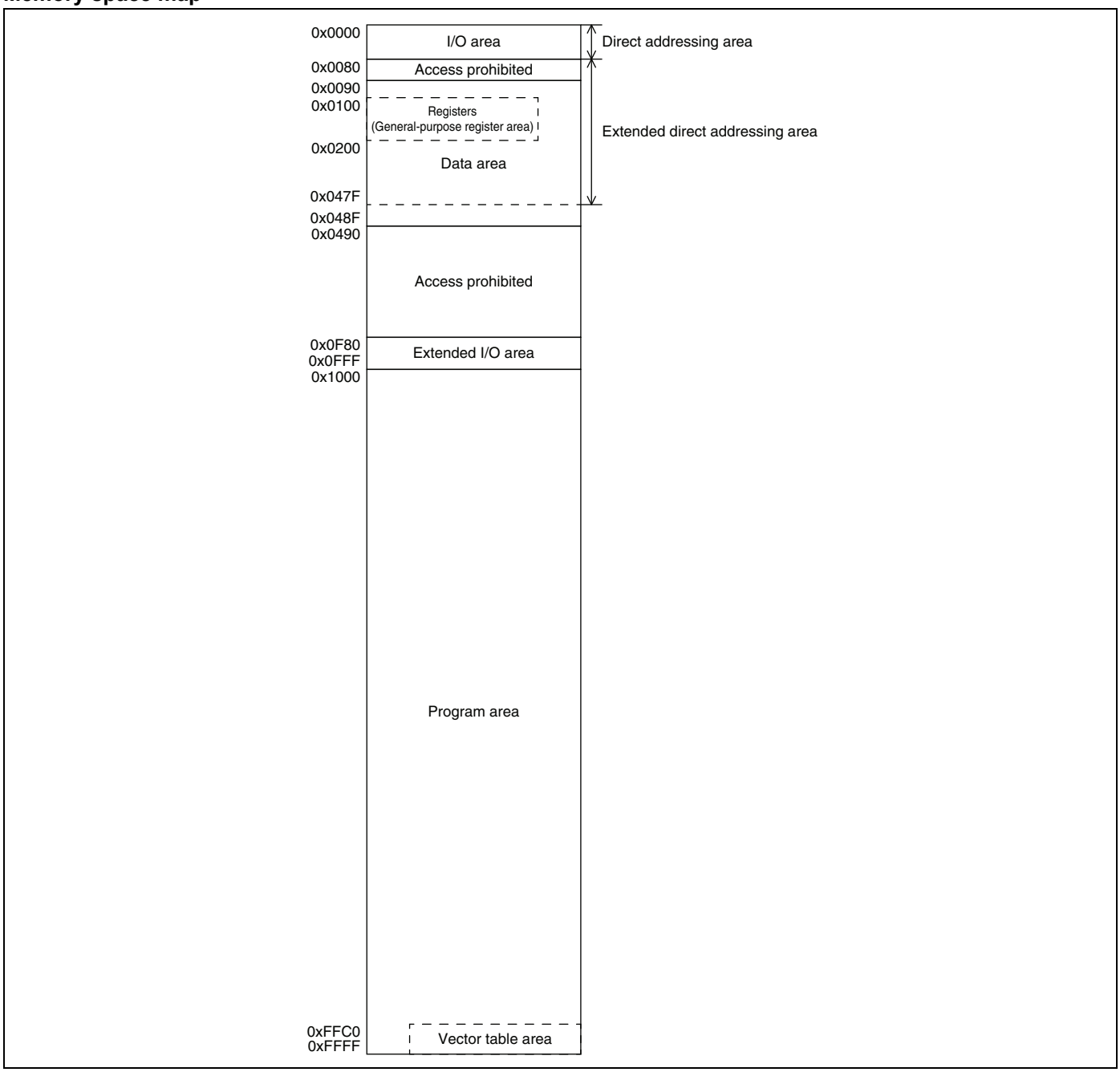
Data area

- Static RAM is incorporated in the data area as the internal data area.
- The internal RAM size varies according to product.
- The RAM area from 0x0090 to 0x00FF can be accessed at high-speed by using direct addressing instructions.
- In MB95F656E/F656L, the area from 0x0090 to 0x047F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
- In MB95F654E/F654L, the area from 0x0090 to 0x047F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
- In MB95F653E/F653L, the area from 0x0090 to 0x028F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
- In MB95F652E/F652L, the area from 0x0090 to 0x018F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
- In MB95F653E/F653L/F654E/F654L/F656E/F656L, the area from 0x0100 to 0x01FF can be used as a general-purpose register area.
- In MB95F652E/F652L, the area from 0x0100 to 0x018F can be used as a general-purpose register area.

Program area

- The Flash memory is incorporated in the program area as the internal program area.
- The Flash memory size varies according to product.
- The area from 0xFFC0 to 0xFFFF is used as the vector table.
- The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register.

Memory space map



14. I/O Map

Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	—	(Disabled)	—	—
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E to 0x0015	—	(Disabled)	—	—
0x0016	PDR6	Port 6 data register	R/W	0b00000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018 to 0x0027	—	(Disabled)	—	—
0x0028	PDRF	Port F data register	R/W	0b00000000
0x0029	DDRF	Port F direction register	R/W	0b00000000
0x002A	PDRG	Port G data register	R/W	0b00000000
0x002B	DDRG	Port G direction register	R/W	0b00000000
0x002C	PUL0	Port 0 pull-up register	R/W	0b00000000
0x002D to 0x0032	—	(Disabled)	—	—
0x0033	PUL6	Port 6 pull-up register	R/W	0b00000000
0x0034	—	(Disabled)	—	—
0x0035	PULG	Port G pull-up register	R/W	0b00000000
0x0036	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0b00000000
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0b00000000
0x0039	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	0b00000000
0x003A to 0x0048	—	(Disabled)	—	—

(Continued)

15.1 Port 0

Port 0 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95650L Series Hardware Manual”.

15.1.1 Port 0 configuration

Port 0 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 0 data register (PDR0)
- Port 0 direction register (DDR0)
- Port 0 pull-up register (PUL0)
- A/D input disable register (lower) (AIDRL)

15.1.2 Block diagrams of port 0

P00/AN00 pin

This pin has the following peripheral function:

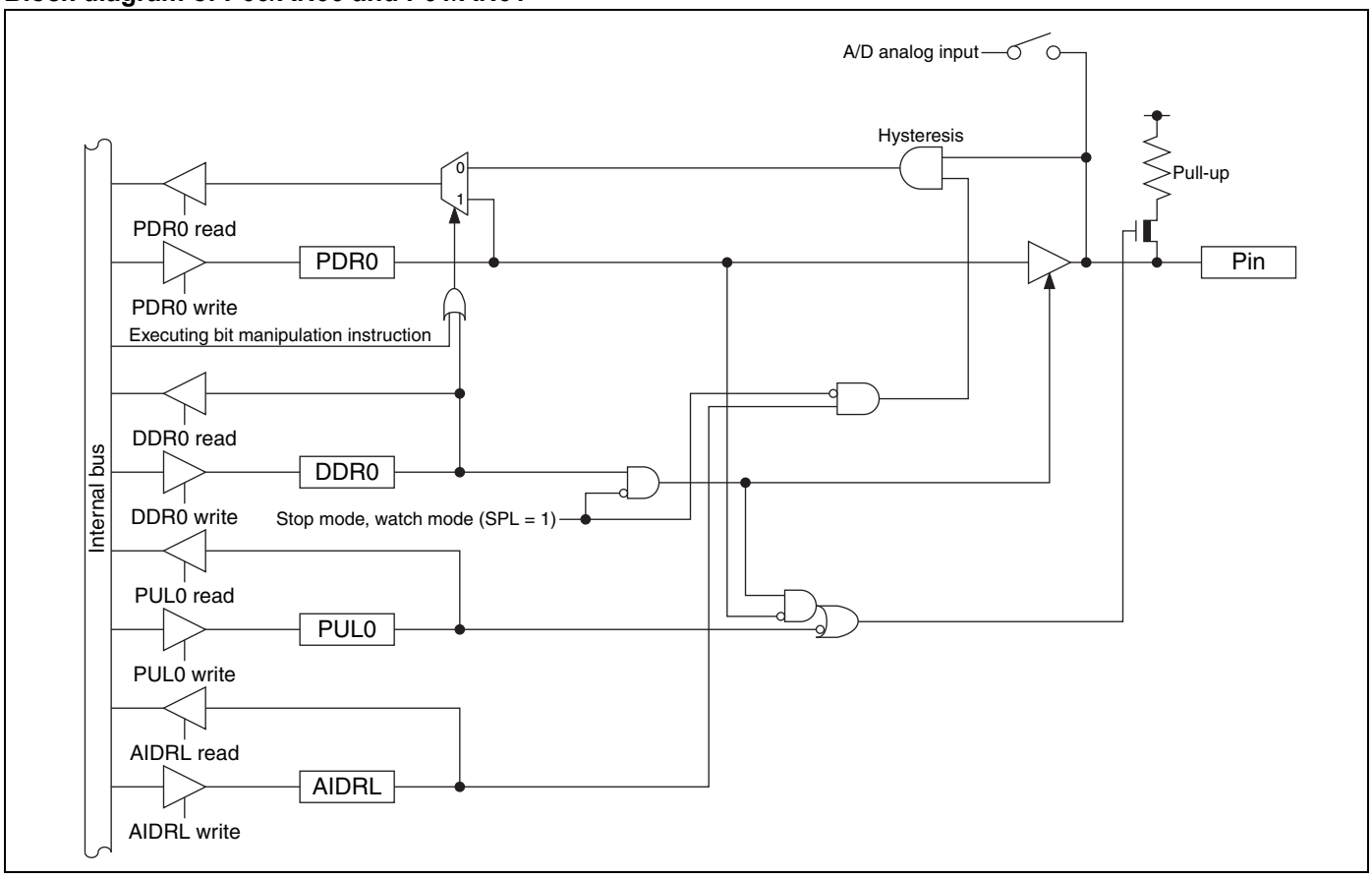
- 8/12-bit A/D converter analog input pin (AN00)

P01/AN01 pin

This pin has the following peripheral function:

- 8/12-bit A/D converter analog input pin (AN01)

Block diagram of P00/AN00 and P01/AN01



P06/INT06/TO01 pin

This pin has the following peripheral functions:

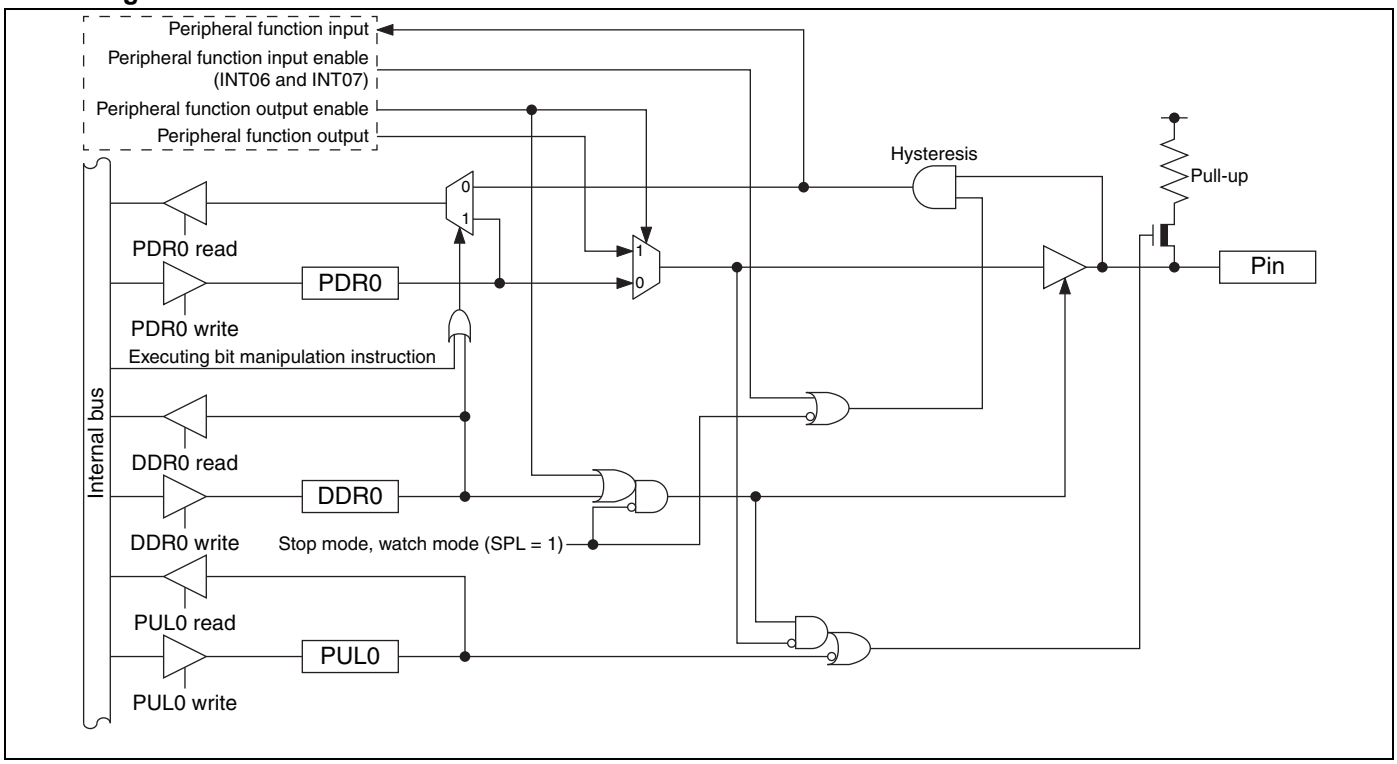
- External interrupt input pin (INT06)
- 8/16-bit composite timer ch. 0 output pin (TO01)

P07/INT07/TO10 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT07)
- 8/16-bit composite timer ch. 1 output pin (TO10)

Block diagram of P06/INT06/TO01 and P07/INT07/TO10



15.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95650L Series Hardware Manual”.

15.2.1 Port 1 configuration

Port 1 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 1 data register (PDR1)
- Port 1 direction register (DDR1)

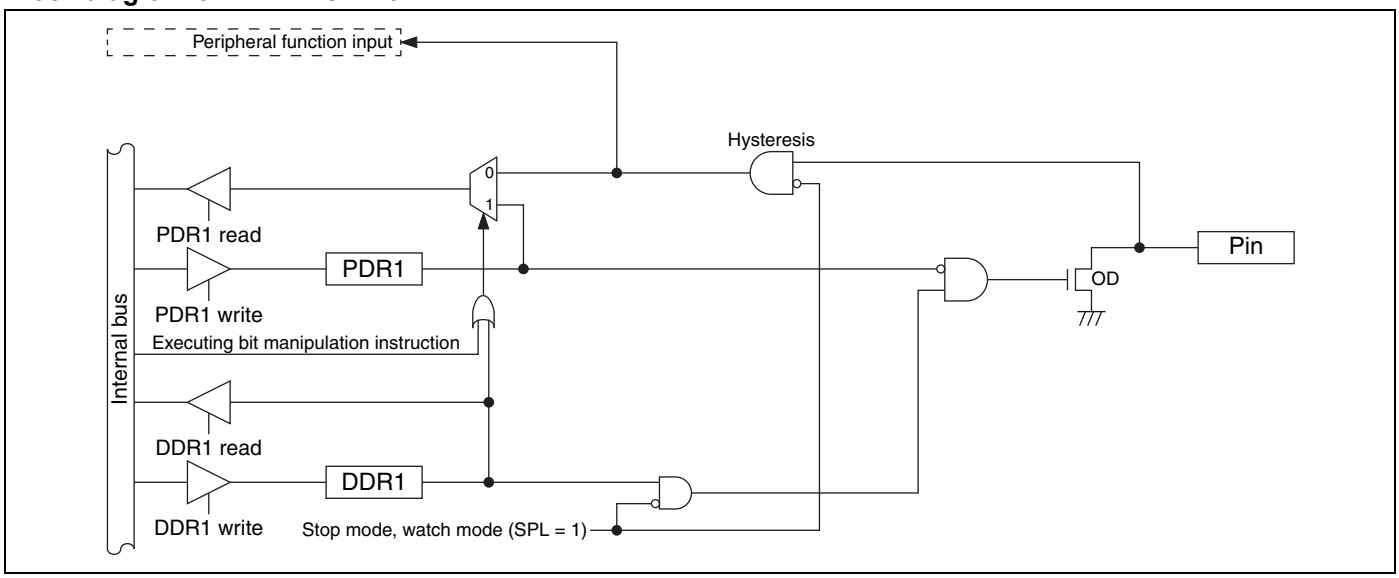
15.2.2 (2)Block diagrams of port 1

P12/DBG/EC0 pin

This pin has the following peripheral functions:

- DBG input pin (DBG)
- 8/16-bit composite timer ch. 0 clock input pin (EC0)

Block diagram of P12/DBG/EC0



15.3.3 Port 6 registers

Port 6 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR6	0	Pin state is “L” level.	PDR6 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR6 value is “1”.	As output port, outputs “H” level.*
DDR6	0	Port input enabled		
	1	Port output enabled		
PUL6	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

Correspondence between registers and pins for port 6

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**P64**	**P63**	**P62**	**-**	**-**
PDR6	-	-	-	bit4	bit3	bit2	-	-
DDR6								
PUL6								

15.3.4 Port 6 operations

Operation as an output port
- A pin becomes an output port if the bit in the DDR6 register corresponding to that pin is set to “1”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- When a pin is used as an output port, it outputs the value of the PDR6 register to external pins.
- If data is written to the PDR6 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- Reading the PDR6 register returns the PDR6 register value.

Operation as an input port
- A pin becomes an input port if the bit in the DDR6 register corresponding to that pin is set to “0”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDR6 register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDR6 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

Operation as a peripheral function output pin
- A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- The pin value can be read from the PDR6 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR6 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

Operation as a peripheral function input pin
- To set a pin as an input port, set the bit in the DDR6 register corresponding to the input pin of a peripheral function to “0”.
- Reading the PDR6 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR6 register, the PDR6 register value is returned.

Operation at reset

If the CPU is reset, all bits in the DDR6 register are initialized to “0” and port input is enabled.

Operation in stop mode and watch mode
- If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR6 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

Operation of the pull-up register

Setting the bit in the PUL6 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL6 register.

15.4.3 Port F registers

Port F register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRF	0	Pin state is “L” level.	PDRF value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRF value is “1”.	As output port, outputs “H” level.*
DDRF	0	Port input enabled		
	1	Port output enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

Correspondence between registers and pins for port F

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**PF2***	**PF1**	**PF0**
PDRF	-	-	-	-	-	bit2	bit1	bit0
DDRF								

*: PF2/$\overline{\text{RST}}$ is the dedicated reset pin on MB95F652L/F653L/F654L/F656L.

16. Interrupt Source Table

Interrupt source	Interrupt request number	Vector table address		Interrupt level setting register		Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower	Register	Bit	
External interrupt ch. 4	IRQ00	0xFFFA	0xFFFB	ILR0	L00 [1:0]	High
External interrupt ch. 5	IRQ01	0xFFF8	0xFFF9	ILR0	L01 [1:0]	
External interrupt ch. 2	IRQ02	0xFFF6	0xFFF7	ILR0	L02 [1:0]	
External interrupt ch. 6						
External interrupt ch. 3	IRQ03	0xFFF4	0xFFF5	ILR0	L03 [1:0]	
External interrupt ch. 7						
Low-voltage detection interrupt circuit	IRQ04	0xFFF2	0xFFF3	ILR1	L04 [1:0]	
UART/SIO ch. 0						
8/16-bit composite timer ch. 0 (lower)	IRQ05	0xFFF0	0xFFF1	ILR1	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	0xFFEE	0xFFEF	ILR1	L06 [1:0]	
LIN-UART (reception)	IRQ07	0xFFEC	0xFFED	ILR1	L07 [1:0]	
LIN-UART (transmission)	IRQ08	0xFFEA	0xFFEB	ILR2	L08 [1:0]	
—	IRQ09	0xFFE8	0xFFE9	ILR2	L09 [1:0]	
I^2C bus interface ch. 1	IRQ10	0xFFE6	0xFFE7	ILR2	L10 [1:0]	
—	IRQ11	0xFFE4	0xFFE5	ILR2	L11 [1:0]	
—	IRQ12	0xFFE2	0xFFE3	ILR3	L12 [1:0]	
—	IRQ13	0xFFE0	0xFFE1	ILR3	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	0xFFDE	0xFFDF	ILR3	L14 [1:0]	
—	IRQ15	0xFFDC	0xFFDD	ILR3	L15 [1:0]	
I^2C bus interface ch. 0	IRQ16	0xFFDA	0xFFDB	ILR4	L16 [1:0]	
—	IRQ17	0xFFD8	0xFFD9	ILR4	L17 [1:0]	
8/12-bit A/D converter	IRQ18	0xFFD6	0xFFD7	ILR4	L18 [1:0]	
Time-base timer	IRQ19	0xFFD4	0xFFD5	ILR4	L19 [1:0]	
Watch prescaler	IRQ20	0xFFD2	0xFFD3	ILR5	L20 [1:0]	
—	IRQ21	0xFFD0	0xFFD1	ILR5	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	0xFFCE	0xFFCF	ILR5	L22 [1:0]	
Flash memory	IRQ23	0xFFCC	0xFFCD	ILR5	L23 [1:0]	Low

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*1	Max*6		
Power supply current*7	I_{CCTS}	V_{CC} (External clock operation)	F_{CH} = 32 MHz Time-base timer mode T_A = +25 °C	—	450	500	µA	
	I_{CCH}		Substop mode T_A = +25 °C	—	0.7	5	µA	
	I_{PLVD}	V_{CC}	Current consumption of the low-voltage detection reset circuit in operation	—	6	26	µA	
	I_{ILVD}		Current consumption of the low-voltage detection interrupt circuit operating in normal mode	—	6	14	µA	
	I_{ILVDL}		Current consumption of the low-voltage detection interrupt circuit operating in low power consumption mode	—	3	10	µA	
	I_{CRH}		Current consumption of the main CR oscillator	—	270	320	µA	
	I_{CRL}		Current consumption of the sub-CR oscillator oscillating at 100 kHz	—	5	20	µA	
	I_{SOSC}		Current consumption of the suboscillator	—	0.8	7	µA	

*1: V_{CC} = 3.0 V, T_A = +25 °C

*2: When V_{CC} is smaller than 4.5 V, the condition becomes I_{OH} = –2 mA.

*3: When V_{CC} is smaller than 4.5 V, the condition becomes I_{OH} = –4 mA.

*4: When V_{CC} is smaller than 4.5 V, the condition becomes I_{OL} = 2 mA.

*5: When V_{CC} is smaller than 4.5 V, the condition becomes I_{OH} = 6 mA.

*6: V_{CC} = 3.3 V, T_A = +85 °C (unless otherwise specified)

*7:
- The power supply current is determined by the external clock. When the low-voltage detection reset circuit is selected, the power supply current is the sum of adding the current consumption of the low-voltage detection reset circuit (I_{PLVD}) to one of the values from I_{CC} to I_{CCH}. In addition, when the low-voltage detection reset circuit and a CR oscillator are selected, the power supply current is the sum of adding up the current consumption of the low-voltage detection reset circuit (I_{PLVD}), the current consumption of the CR oscillator (I_{CRH} or I_{CRL}) and one of the values from I_{CC} to I_{CCH}. In on-chip debug mode, the main CR oscillator (I_{CRH}) and the low-voltage detection reset circuit are always in operation, and current consumption therefore increases accordingly.
- See “18.4. AC Characteristics 18.4.1. Clock Timing” for F_{CH}, F_{CL}, F_{CRH}, F_{MCRPLL} and F_{MPLL}.
- See “18.4. AC Characteristics 18.4.2. Source Clock/Machine Clock” for F_{MP} and F_{MPL}.
- The power supply current in subclock mode is determined by the external clock. In subclock mode, current consumption in using the crystal oscillator is higher than that in using the external clock. When the crystal oscillator is used, the power supply current is the sum of adding I_{SOSC} (current consumption of the suboscillator) to the power supply current in using the external clock. For details of controlling the subclock, refer to “Chapter 3 Clock Controller” And “chapter 24 System Configuration Register” in “New 8FX MB95650L Series Hardware Manual”.

18.4.7 Low-vo ltage Detection

Normal mode

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Reset release voltage	V_{PDL+}	1.88	2.03	2.18	V	At power supply rise
Reset detection voltage	$V_{PDL–}$	1.8	1.93	2.06	V	At power supply fall
Interrupt release voltage 0	V_{IDL0+}	2.13	2.3	2.47	V	At power supply rise
Interrupt detection voltage 0	$V_{IDL0–}$	2.05	2.2	2.35	V	At power supply fall
Interrupt release voltage 1	V_{IDL1+}	2.41	2.6	2.79	V	At power supply rise
Interrupt detection voltage 1	$V_{IDL1–}$	2.33	2.5	2.67	V	At power supply fall
Interrupt release voltage 2	V_{IDL2+}	2.69	2.9	3.11	V	At power supply rise
Interrupt detection voltage 2	$V_{IDL2–}$	2.61	2.8	2.99	V	At power supply fall
Interrupt release voltage 3	V_{IDL3+}	3.06	3.3	3.54	V	At power supply rise
Interrupt detection voltage 3	$V_{IDL3–}$	2.98	3.2	3.42	V	At power supply fall
Interrupt release voltage 4	V_{IDL4+}	3.43	3.7	3.97	V	At power supply rise
Interrupt detection voltage 4	$V_{IDL4–}$	3.35	3.6	3.85	V	At power supply fall
Interrupt release voltage 5	V_{IDL5+}	3.81	4.1	4.39	V	At power supply rise
Interrupt detection voltage 5	$V_{IDL5–}$	3.73	4	4.27	V	At power supply fall
Power supply start voltage	V_{off}	—	—	1.6	V	
Power supply end voltage	V_{on}	4.39	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	697.5	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{PDL+}/V_{IDL+})
Power supply voltage change time (at power supply fall)	t_f	697.5	—	—	µs	Slope of power supply that the reset release signal generates within the rating ($V_{PDL–}$/$V_{IDL–}$)
Reset release delay time	t_{dp1}	—	—	30	µs	
Reset detection delay time	t_{dp2}	—	—	30	µs	
Interrupt release delay time	t_{di1}	—	—	30	µs	
Interrupt detection delay time	t_{di2}	—	—	30	µs	
LVD reset threshold voltage transition stabilization time	t_{stb}	—	—	30	µs	

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL0, SCL1	R = 1.7 kΩ, C = 50 pF*1	$(2 + nm/2)t_{MCLK} - 20$	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL0, SCL1		$(nm/2)t_{MCLK} - 20$	$(nm/2)t_{MCLK} + 20$	ns	Master mode
START condition hold time	$t_{HD;STA}$	SCL0, SCL1, SDA0, SDA1		$(-1 + nm/2)t_{MCLK} - 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	$t_{SU;STO}$	SCL0, SCL1, SDA0, SDA1		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
START condition setup time	$t_{SU;STA}$	SCL0, SCL1, SDA0, SDA1		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
Bus free time between STOP condition and START condition	t_{BUF}	SCL0, SCL1, SDA0, SDA1		$(2\ nm + 4)\ t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		$3\ t_{MCLK} - 20$	—	ns	Master mode

(Continued)

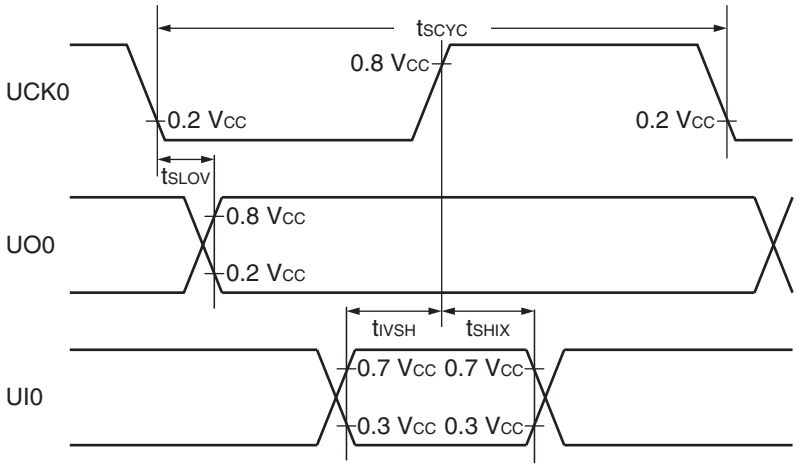
18.4.9 UART/SIO, Serial I/O Timing

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

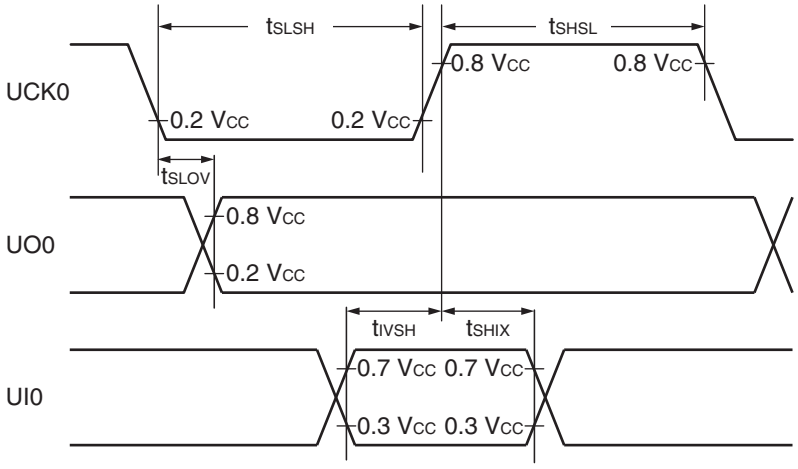
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0	Internal clock operation	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		–190	+190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK0	External clock operation	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK0		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		—	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns

*: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.

Internal shift clock mode



External shift clock mode



18.6 Flash Memory Program/Erase Characteristics

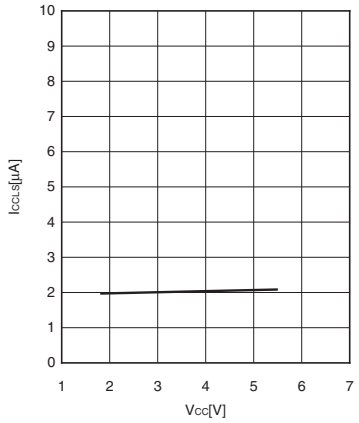
Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.3*1	1.6*2	s	The time of writing “0x00” prior to erasure is excluded.
Sector erase time (32 Kbyte sector)	—	0.6*1	3.1*2	s	The time of writing “0x00” prior to erasure is excluded.
Byte writing time	—	17	272	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	1.8	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85 °C Number of program/erase cycles: 1000 or below
	10*3	—	—		Average T_A = +85 °C Number of program/erase cycles: 1001 to 10000 inclusive
	5*3	—	—		Average T_A = +85 °C Number of program/erase cycles: 10001 or above

*1: V_{CC} = 5.5 V, T_A = +25 °C, 0 cycle

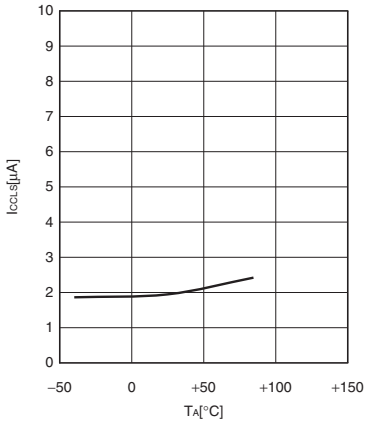
*2: V_{CC} = 1.8 V, T_A = +85 °C, 100000 cycles

*3: These values were converted from the result of a technology reliability assessment. (These values were converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85 °C.)

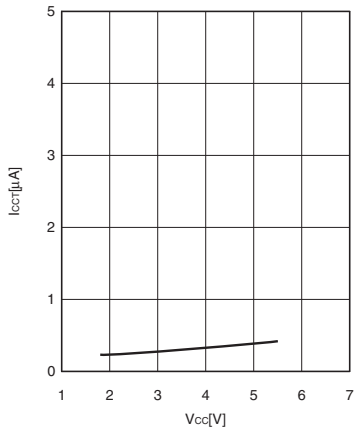
I_{CCLS} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



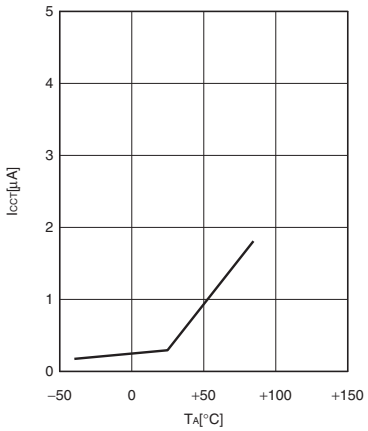
I_{CCLS} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



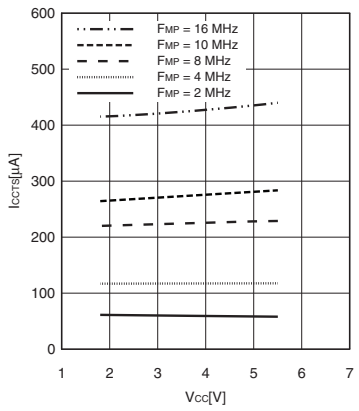
I_{CCT} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



I_{CCT} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



I_{CCTS} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



I_{CCTS} – T_A
V_{CC} = 3.3 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating