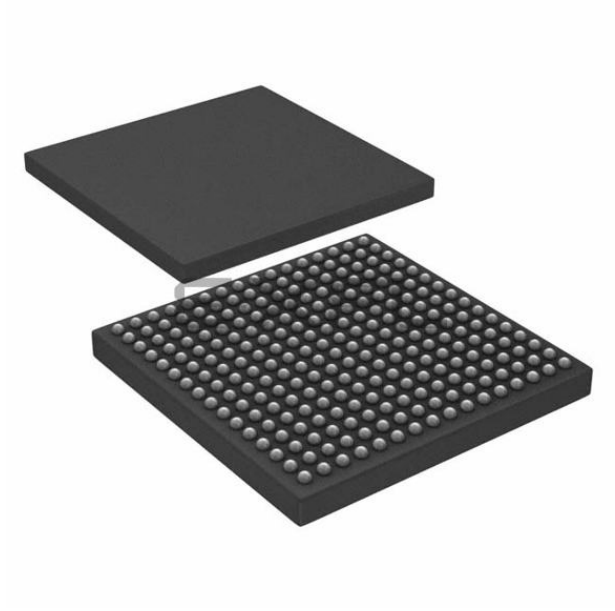

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	533MHz
Non-Volatile Memory	External
On-Chip RAM	328kB
Voltage - I/O	3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-BGA, CSPBGA
Supplier Device Package	256-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf561wbbcz505

- ADSP-BF561: Blackfin Embedded Symmetric Multiprocessor Data Sheet

Emulator Manuals

- HPUSB, USB, and HPPCI Emulator User's Guide
- ICE-1000/ICE-2000 Emulator User's Guide
- ICE-100B Emulator User's Guide

Evaluation Kit Manuals

- ADSP-BF561 EZ-KIT Lite® Evaluation System Manual
- Blackfin® A-V EZ-Extender® Manual
- Blackfin® EZ-Extender® Manual
- Blackfin® FPGA EZ-Extender® Manual
- Blackfin®/SHARC® USB EZ-Extender® Manual

Integrated Circuit Anomalies

- ADSP-BF561 Blackfin Anomaly List for Revisions 0.3, 0.5

Processor Manuals

- ADSP-BF561 Blackfin ® Processor Hardware Reference
- ADSP-BF5xx/ADSP-BF60x Blackfin® Processor Programming Reference
- Blackfin Processors: Manuals

Product Highlight

- ADSP-BF561 Blackfin Dual-Core Embedded Processor
- Blackfin Processor Family Product Highlight
- EZ-KIT Lite for Analog Devices ADSP-BF561 Blackfin Processor

Software Manuals

- CrossCore® Embedded Studio 2.5.0 Assembler and Preprocessor Manual
- CrossCore® Embedded Studio 2.5.0 C/C++ Compiler and Library Manual for Blackfin Processors
- CrossCore® Embedded Studio 2.5.0 Linker and Utilities Manual
- CrossCore® Embedded Studio 2.5.0 Loader and Utilities Manual
- CrossCore® Software Licensing Guide
- lwIP for CrossCore® Embedded Studio 1.0.0 User's Guide
- VisualDSP++® 5.0 Assembler and Preprocessor Manual
- VisualDSP++® 5.0 C/C++ Compiler and Library Manual for Blackfin Processors
- VisualDSP++® 5.0 Device Drivers and System Services Manual for Blackfin Processors
- VisualDSP++® 5.0 Kernel (VDK) Users Guide
- VisualDSP++® 5.0 Licensing Guide
- VisualDSP++® 5.0 Linker and Utilities Manual
- VisualDSP++® 5.0 Loader and Utilities Manual
- VisualDSP++® 5.0 Product Release Bulletin
- VisualDSP++® 5.0 Quick Installation Reference Card
- VisualDSP++® 5.0 Users Guide

SOFTWARE AND SYSTEMS REQUIREMENTS

- Software and Tools Anomalies Search

TOOLS AND SIMULATIONS

- ADSP-BF561 Blackfin Processor BSDL File 256-Ball CSP BGA Package
- ADSP-BF561 Blackfin Processor BSDL File 256-Ball Sparse CSP_BGA Package
- ADSP-BF561 Blackfin Processor BSDL File 297-Ball PBGA Package
- ADSP-BF561 Blackfin Processor Core B BSDL File All Packages
- Designing with BGA
- Blackfin Processors Software and Tools
- ADSP-BF561 Blackfin Processor IBIS Datafile for 12x12 CSP BGA Package (02/2008)
- ADSP-BF561 Blackfin Processor IBIS Datafile for 17x17 CSP BGA Package (11/2008)
- ADSP-BF561 Blackfin Processor IBIS Datafile for 27x27 PBGA Package (02/2008)

REFERENCE MATERIALS

Customer Case Studies

- Dahua Case Study
- UTAS Medical Equipment Ensures High Quality Patient Care with Help from Analog Devices

Technical Articles

- An Efficient Asynchronous Sampling-rate Conversion Algorithm for Multi-channel Audio Applications
- Blackfin Processor Targets Digital Media Open Source Applications
- Blackfin Processor's Parallel Peripheral Interface Simplifies LCD Connection in Portable Multimedia
- Designing IPTV Set-top Boxes Without Getting Boxed In
- Enhance Processor Performance in Open-Source Applications
- High Performance DSPs for Portable Applications
- Is it Really Possible to Play DVD Quality Media While Executing Linux Applications?
- Understanding Advanced Processor Features Promotes Efficient Coding
- Video Filtering Considerations for Media Processors

White Papers

- A BDTI Analysis of the Analog Devices ADSP-BF5xx
- Blackfin Car Telematics Platform Brings Low Cost Telematics to the Mass Market
- Device-Based Social Networking
- LabVIEW 1000m Below the Waves: Synchronized Sampling of Autonomous Units Through Sound
- Secure, Field Upgradeable OS Architecture for Blackfin
- Security Without Compromise
- Unifying Microarchitecture for Embedded Media Processing

DESIGN RESOURCES

- ADSP-BF561 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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TABLE OF CONTENTS

REVISION HISTORY

9/09—Rev. D to Rev. E

Correct all outstanding document errata.

Revised Figure 5 13

Added 533 MHz operation Table 10 20

Removed reference to 1.8 V operation Table 12 21

Added Table 17 and Figure 9 Power-Up Reset Timing 23

Removed references to T_J from t_{SCLK} parameter
Table 20 26

Added new SPORT timing parameters and diagram
Table 23 32
Figure 21 33

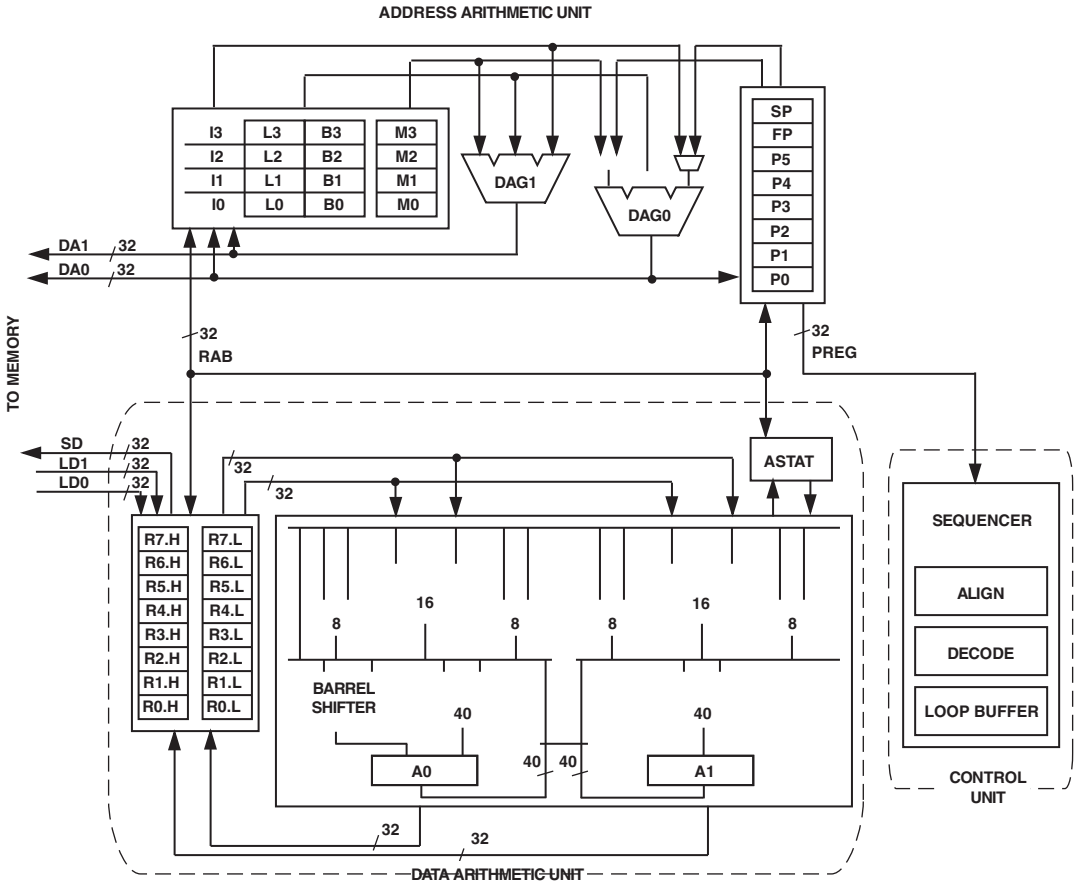

Figure 2. Blackfin Processor Core

MEMORY ARCHITECTURE

The ADSP-BF561 views memory as a single unified 4G byte address space, using 32-bit addresses. All resources including internal memory, external memory, and I/O control registers occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low latency memory as cache or SRAM very close to the processor, and larger, lower cost and performance memory systems farther away from the processor. The ADSP-BF561 memory map is shown in Figure 3.

The L1 memory system in each core is the highest performance memory available to each Blackfin core. The L2 memory provides additional capacity with lower performance. Lastly, the off-chip memory system, accessed through the External Bus Interface Unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing more than 768M bytes of physical memory. The memory DMA controllers provide high bandwidth data movement capability. They can perform block transfers of code or data between the internal L1/L2 memories and the external memory spaces.

Internal (On-Chip) Memory

The ADSP-BF561 has four blocks of on-chip memory providing high bandwidth access to the core.

The first is the L1 instruction memory of each Blackfin core consisting of 16K bytes of four-way set-associative cache memory and 16K bytes of SRAM. The cache memory may also be configured as an SRAM. This memory is accessed at full processor speed. When configured as SRAM, each of the two 16K banks of memory is broken into 4K sub-banks which can be independently accessed by the processor and DMA.

The second on-chip memory block is the L1 data memory of each Blackfin core which consists of four banks of 16K bytes each. Two of the L1 data memory banks can be configured as one way of a two-way set-associative cache or as an SRAM. The other two banks are configured as SRAM. All banks are accessed at full processor speed. When configured as SRAM, each of the four 16K banks of memory is broken into 4K sub-banks which can be independently accessed by the processor and DMA.

The third memory block associated with each core is a 4K byte scratchpad SRAM which runs at the same speed as the L1 memories, but is only accessible as data SRAM (it cannot be configured as cache memory and is not accessible via DMA).

flexible configuration and upgradability of system memory while allowing the core to view all SDRAM as a single, contiguous, physical address space.

The asynchronous memory controller can also be programmed to control up to four banks of devices with very flexible timing parameters for a wide variety of devices. Each bank occupies a 64M byte segment regardless of the size of the devices used so that these banks will only be contiguous if fully populated with 64M bytes of memory.

I/O Memory Space

Blackfin processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The core MMRs are accessible only by the core and only in supervisor mode and appear as reserved space by on-chip peripherals. The system MMRs are accessible by the core in supervisor mode and can be mapped as either visible or reserved to other devices, depending on the system protection model desired.

Booting

The ADSP-BF561 contains a small boot kernel, which configures the appropriate peripheral for booting. If the ADSP-BF561 is configured to boot from boot ROM memory space, the processor starts executing from the on-chip boot ROM.

Event Handling

The event controller on the ADSP-BF561 handles all asynchronous and synchronous events to the processor. The ADSP-BF561 provides event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher priority event takes precedence over servicing of a lower priority event. The controller provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset – This event resets the processor.
- Nonmaskable Interrupt (NMI) – The NMI event can be generated by the software watchdog timer or by the NMI input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions – Events that occur synchronously to program flow, i.e., the exception will be taken before the instruction is allowed to complete. Conditions such as data alignment violations or undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by timers, peripherals, input pins, and an explicit software instruction.

Each event has an associated register to hold the return address and an associated "return from event" instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The ADSP-BF561 event controller consists of two stages: the Core Event Controller (CEC) and the System Interrupt Controller (SIC). The Core Event Controller works with the System Interrupt Controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC, and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the ADSP-BF561. Table 1 describes the inputs to the CEC, identifies their names in the Event Vector Table (EVT), and lists their priorities.

Table 1. Core Event Controller (CEC)

Priority (0 is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Nonmaskable Interrupt	NMI
3	Exceptions	EVX
4	Global Enable	
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General Interrupt 7	IVG7
8	General Interrupt 8	IVG8
9	General Interrupt 9	IVG9
10	General Interrupt 10	IVG10
11	General Interrupt 11	IVG11
12	General Interrupt 12	IVG12
13	General Interrupt 13	IVG13
14	General Interrupt 14	IVG14
15	General Interrupt 15	IVG15

System Interrupt Controller (SIC)

The System Interrupt Controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the ADSP-BF561 provides a default mapping, the user can alter the mappings and priorities of interrupt events by

regulator for the processor can be shut off by writing b#00 to the FREQ bits of the VR_CTL register. This disables both CCLK and SCLK. Furthermore, it sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the lowest static power dissipation. Any critical information stored internally (memory contents, register contents, etc.) must be written to a nonvolatile storage device prior to removing power if the processor state is to be preserved. Since V_{DDEXT} is still supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to have power still applied without drawing unwanted current. The internal supply regulator can be woken up by asserting the $\overline{\text{RESET}}$ pin.

Power Savings

As shown in Table 4, the ADSP-BF561 supports two different power domains. The use of multiple power domains maximizes flexibility, while maintaining compliance with industry standards and conventions. By isolating the internal logic of the ADSP-BF561 into its own power domain, separate from the I/O, the processor can take advantage of Dynamic Power Management, without affecting the I/O devices. There are no sequencing requirements for the various power domains.

Table 4. ADSP-BF561 Power Domains

Power Domain	V_{DD} Range
All internal logic	V_{DDINT}
I/O	V_{DDEXT}

The power dissipated by a processor is largely a function of the clock frequency of the processor and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic.

The dynamic power management feature of the ADSP-BF561 allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The savings in power dissipation can be modeled using the power savings factor and % power savings calculations.

The power savings factor is calculated as:

$$\textit{power savings factor} = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{t_{RED}}{t_{NOM}}\right)$$

where the variables in the equations are:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

t_{NOM} is the duration running at $f_{CCLKNOM}$

t_{RED} is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as:

$$\%\ \textit{power savings} = (1 - \textit{power savings factor}) \times 100\%$$

VOLTAGE REGULATION

The ADSP-BF561 processor provides an on-chip voltage regulator that can generate appropriate V_{DDINT} voltage levels from the V_{DDEXT} supply. See Operating Conditions on Page 20 for regulator tolerances and acceptable V_{DDEXT} ranges for specific models.

Figure 4 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power (V_{DDEXT}) supplied. While in the hibernate state, V_{DDEXT} can still be applied, thus eliminating the need for external buffers. The voltage regulator can be activated from this power-down state by asserting $\overline{\text{RESET}}$, which will then initiate a boot sequence. The regulator can also be disabled and bypassed at the user's discretion.

The internal voltage regulation feature is not available on any of the 600 MHz speed grade models or automotive grade models. External voltage regulation is required to ensure correct operation of these parts at 600 MHz.

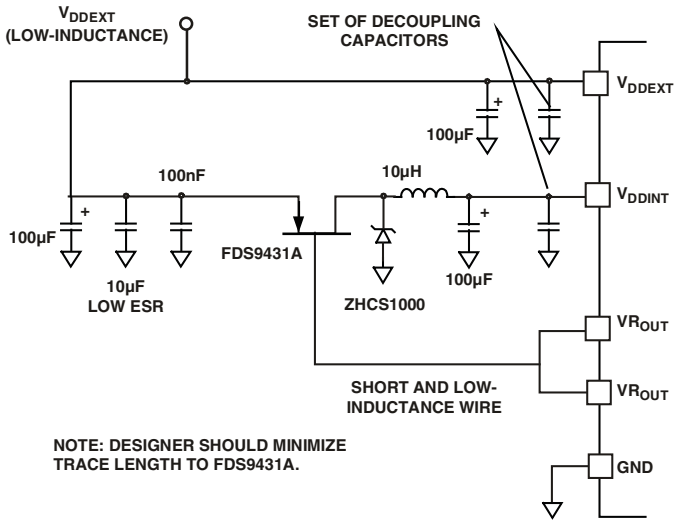

Figure 4. Voltage Regulator Circuit

Voltage Regulator Layout Guidelines

Regulator external component placement, board routing, and bypass capacitors all have a significant effect on noise injected into the other analog circuits on-chip. The VROUT1–0 traces and voltage regulator external components should be considered as noise sources when doing board layout and should not be routed or placed near sensitive circuits or components on the

Parallel Peripheral Interface Timing

Table 22, and Figure 14 through Figure 17 on Page 30, describe default Parallel Peripheral Interface operations.

If bit 4 of the PLL_CTL register is set, then Figure 18 on Page 30 and Figure 19 on Page 31 apply.

Table 22. Parallel Peripheral Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	PPIxCLK Width[1]	5.0		ns
t_{PCLK}	PPIxCLK Period[1]	13.3		ns
t_{SFSPE}	External Frame Sync Setup Before PPIxCLK	4.0		ns
t_{HFSPE}	External Frame Sync Hold After PPIxCLK	1.0		ns
t_{SDRPE}	Receive Data Setup Before PPIxCLK	3.5		ns
t_{HDRPE}	Receive Data Hold After PPIxCLK	2.0		ns
Switching Characteristics				
t_{DFSPE}	Internal Frame Sync Delay After PPIxCLK		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPIxCLK	1.7		ns
t_{DDTPE}	Transmit Data Delay After PPIxCLK		8.0	ns
t_{HDTPE}	Transmit Data Hold After PPIxCLK	2.0		ns

[1] For PPI modes that use an internally generated frame sync, the PPIxCLK frequency cannot exceed $f_{SCLK}/2$. For modes with no frame syncs or external frame syncs, PPIxCLK cannot exceed 75 MHz and f_{SCLK} should be equal to or greater than PPIxCLK.

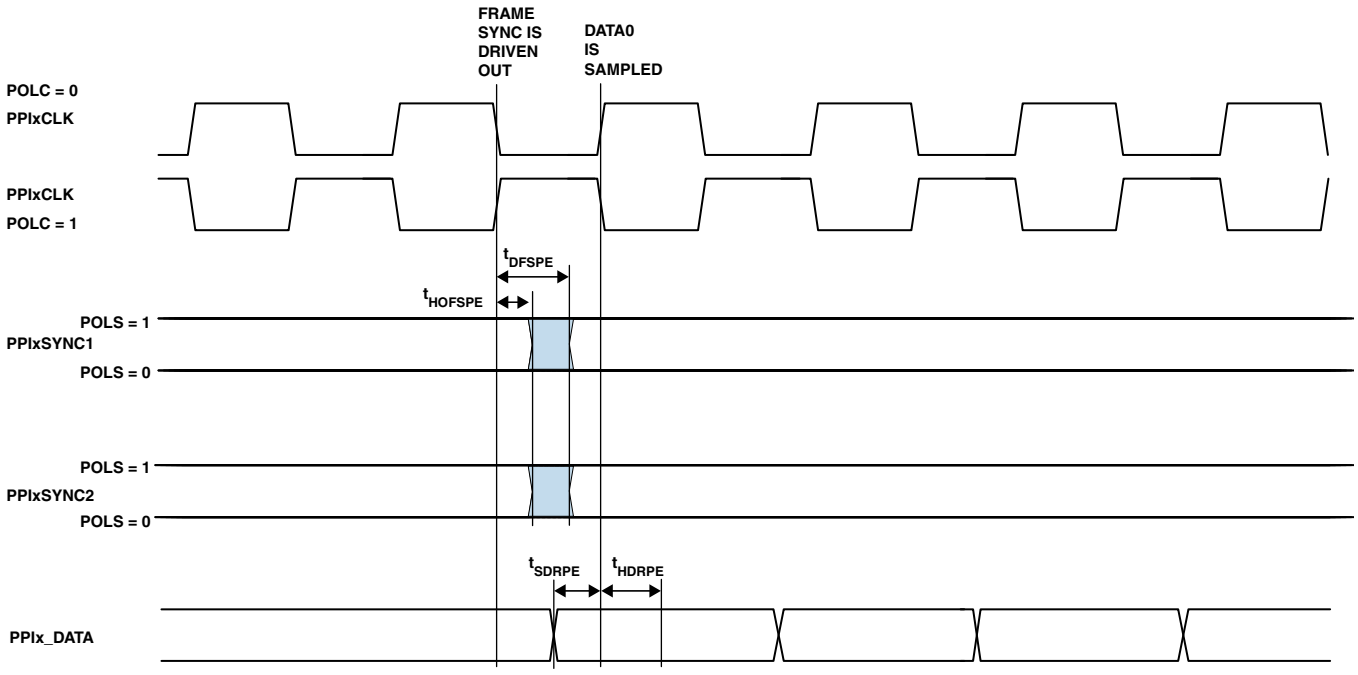

Figure 14. PPI GP Rx Mode with Internal Frame Sync Timing (Default)

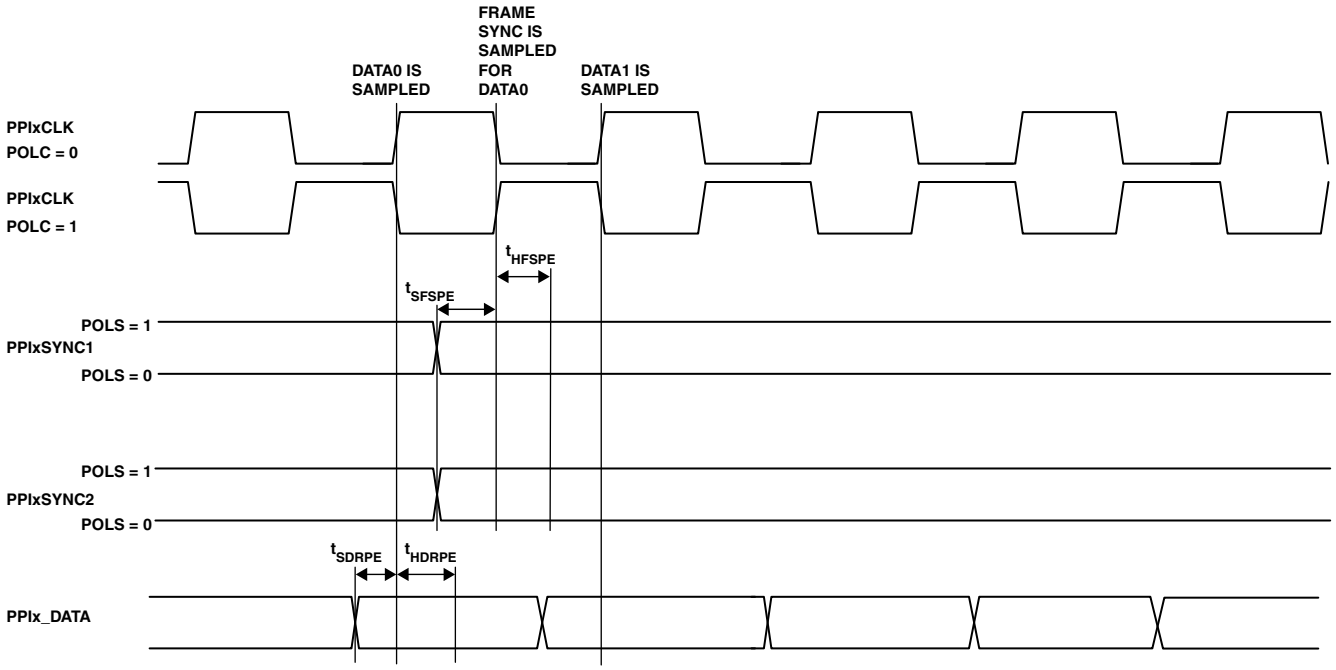

Figure 15. PPI GP Rx Mode with External Frame Sync Timing (Default)

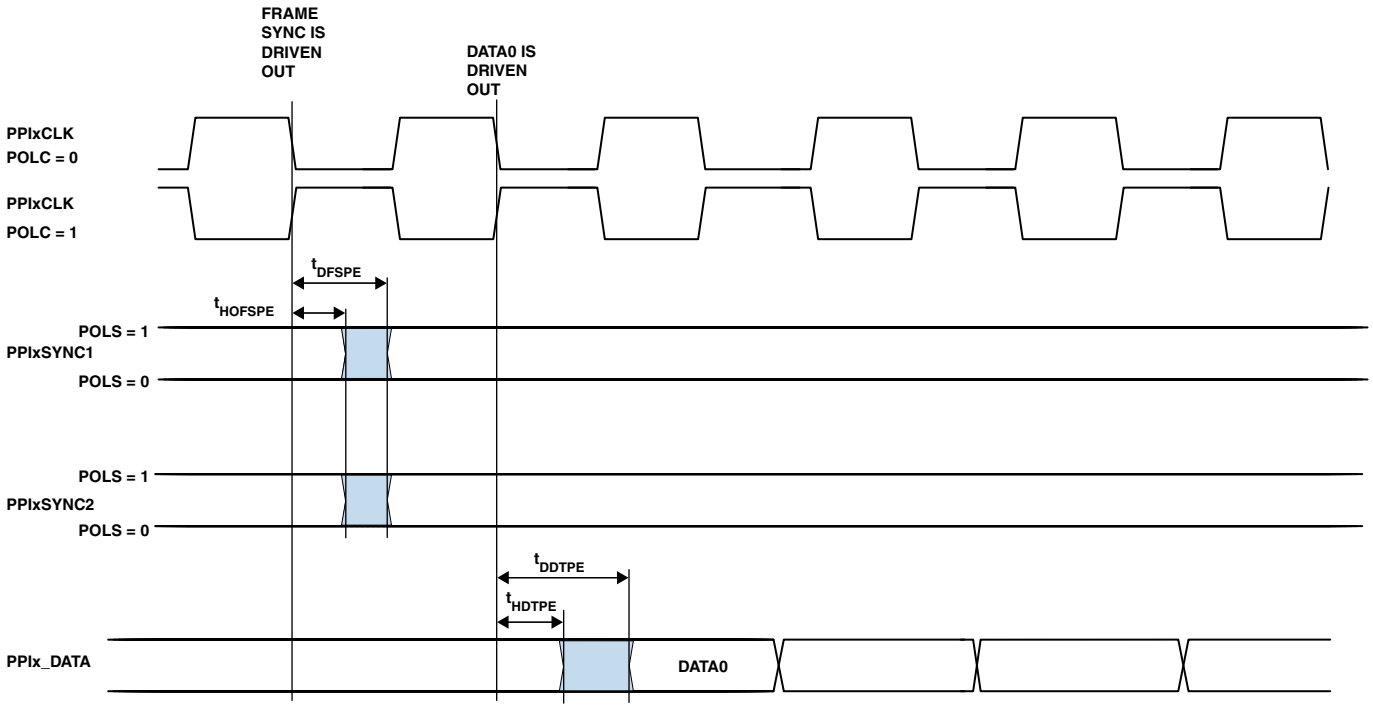

Figure 16. PPI GP Tx Mode with Internal Frame Sync Timing (Default)

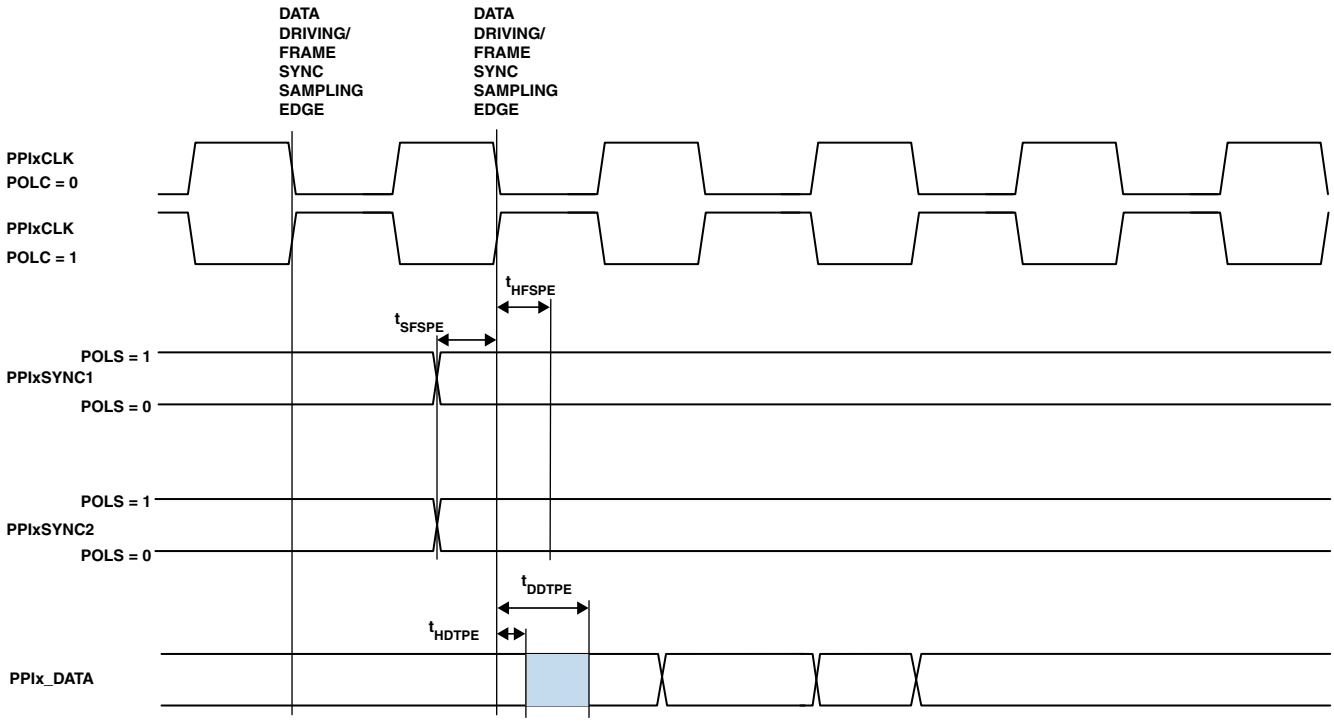

Figure 19. PPI GP Tx Mode with External Frame Sync Timing (Bit 4 of PLL_CTL Set)

Serial Ports

Table 23 through Table 26 on Page 34 and Figure 20 on Page 33 through Figure 22 on Page 34 describe Serial Port operations.

Table 23. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	3.0		ns
t_{HFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	3.0		ns
t_{SDRE}	Receive Data Setup Before RSCLKx[1]	3.0		ns
t_{HDRE}	Receive Data Hold After RSCLKx[1]	3.0		ns
t_{SCLKW}	TSCLKx/RSCLKx Width	4.5		ns
t_{SCLK}	TSCLKx/RSCLKx Period	15.0		ns
t_{SUDTE}	Start-Up Delay From SPORT Enable To First External TFSx	4.0		TSCLKx
t_{SUDRE}	Start-Up Delay From SPORT Enable To First External RFSx	4.0		RSCLKx
Switching Characteristics				
t_{DFSE}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]		10.0	ns
t_{HOFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]	0.0		ns
t_{DDTE}	Transmit Data Delay After TSCLKx[2]		10.0	ns
t_{HDTE}	Transmit Data Hold After TSCLKx[2]	0.0		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 24. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	8.0		ns
t_{HFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	–2.0		ns
t_{SDRI}	Receive Data Setup Before RSCLKx[1]	6.0		ns
t_{HDRI}	Receive Data Hold After RSCLKx[1]	0.0		ns
t_{SCLKW}	TSCLKx/RSCLKx Width	4.5		ns
t_{SCLK}	TSCLKx/RSCLKx Period	15.0		ns
Switching Characteristics				
t_{DFSI}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]		3.0	ns
t_{HOFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]	–1.0		ns
t_{DDTI}	Transmit Data Delay After TSCLKx[2]		3.0	ns
t_{HDTI}	Transmit Data Hold After TSCLKx[2]	–2.0		ns
t_{SCLKIW}	TSCLKx/RSCLKx Width	4.5		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

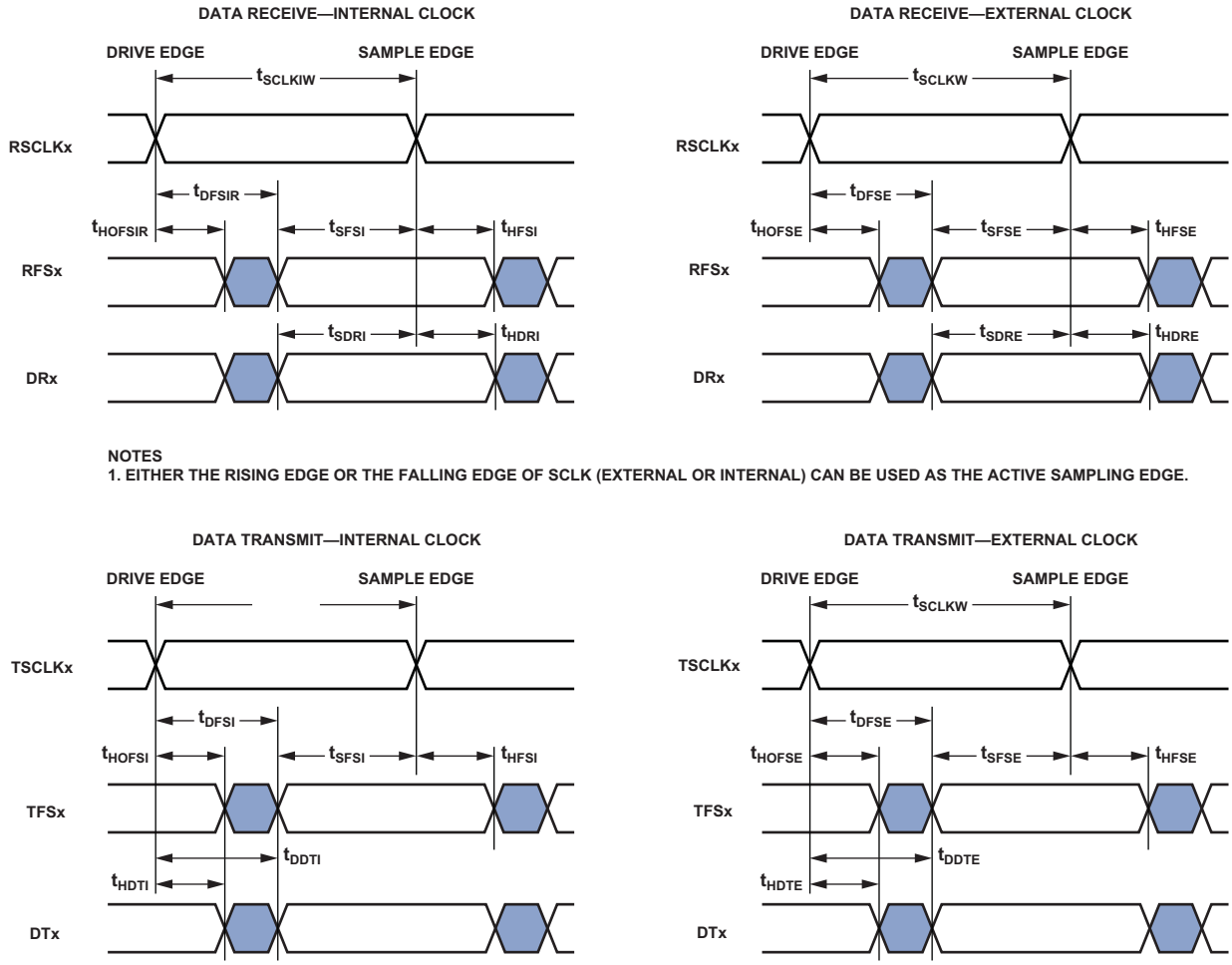

Figure 20. Serial Ports

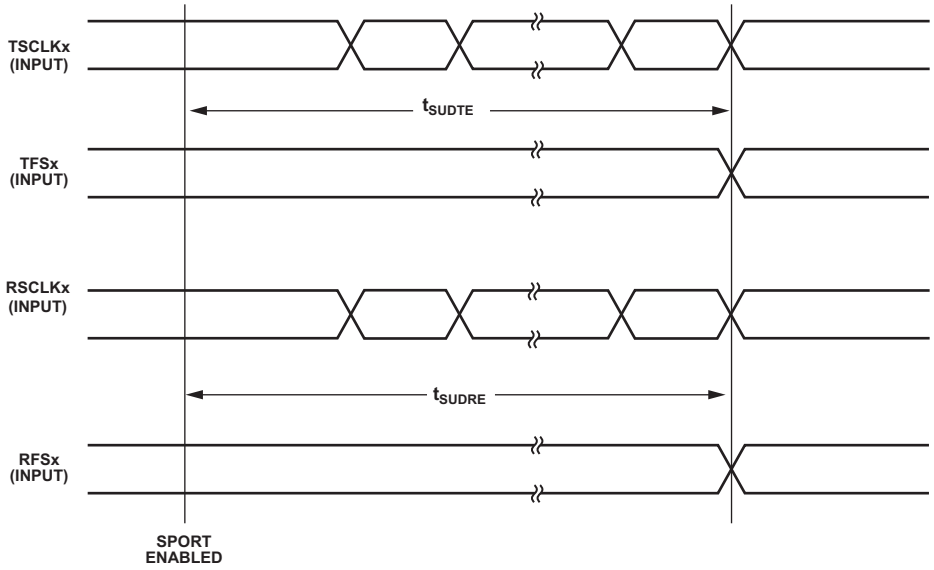

Figure 21. Serial Port Start Up with External Clock and Frame Sync

Programmable Flags Cycle Timing

Table 29 and Figure 26 describe programmable flag operations.

Table 29. Programmable Flags Cycle Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	Flag Input Pulse Width	t_{SCLK} + 1		ns
Switching Characteristic				
t_{DFO}	Flag Output Delay from CLKOUT Low		6	ns

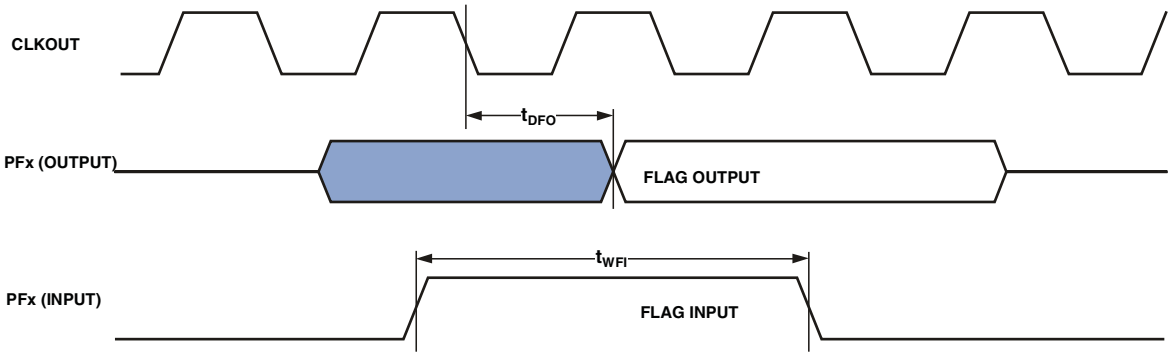

Figure 26. Programmable Flags Cycle Timing

OUTPUT DRIVE CURRENTS

Figure 29 through Figure 36 on Page 42 show typical current voltage characteristics for the output drivers of the ADSP-BF561 processor. The curves represent the current drive capability of the output drivers as a function of output voltage. Refer to Table 8 on Page 17 to identify the driver type for a pin.

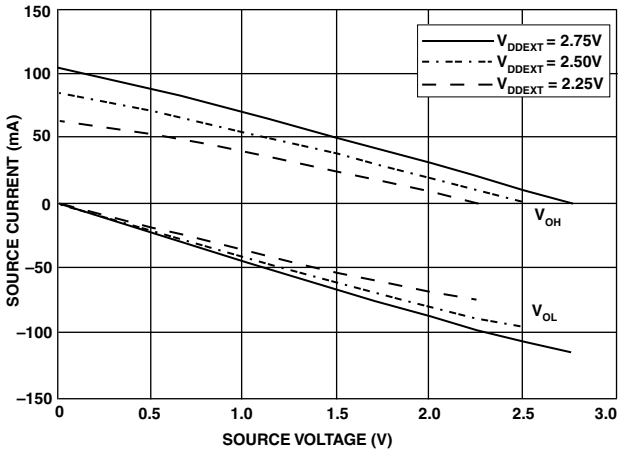

Figure 29. Drive Current A (Low V_{DDEXT})

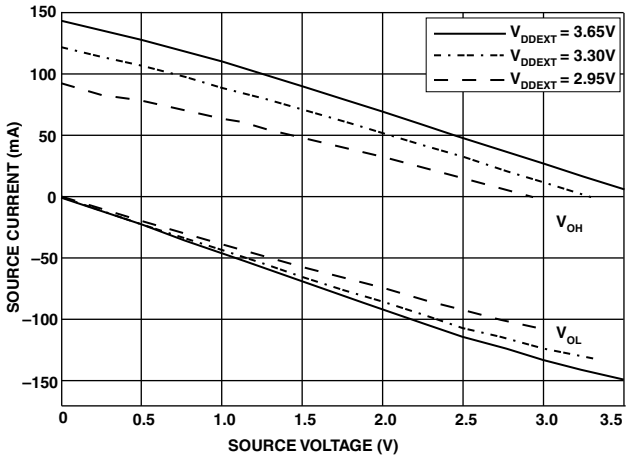

Figure 30. Drive Current A (High V_{DDEXT})

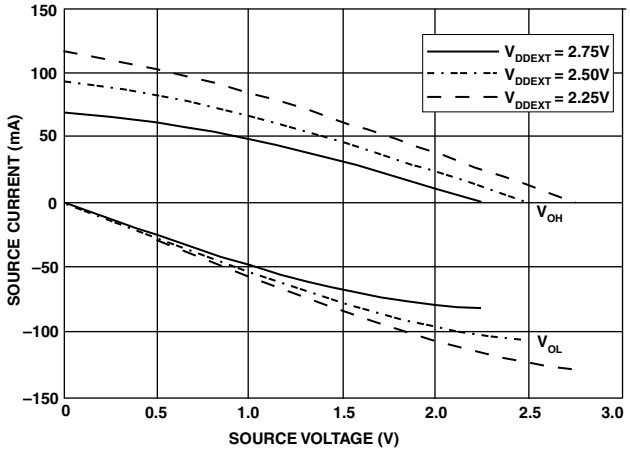

Figure 31. Drive Current B (Low V_{DDEXT})

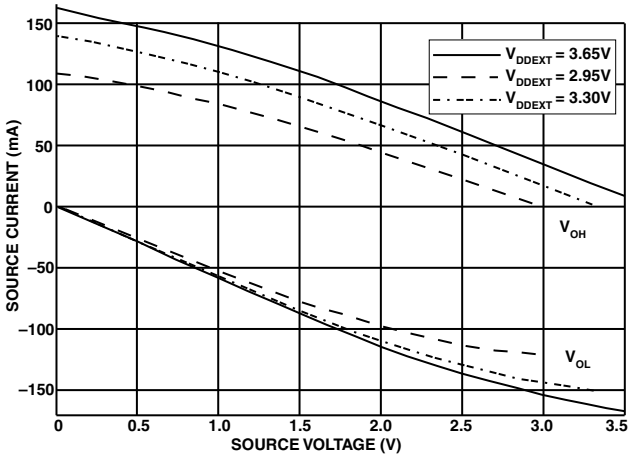

Figure 32. Drive Current B (High V_{DDEXT})

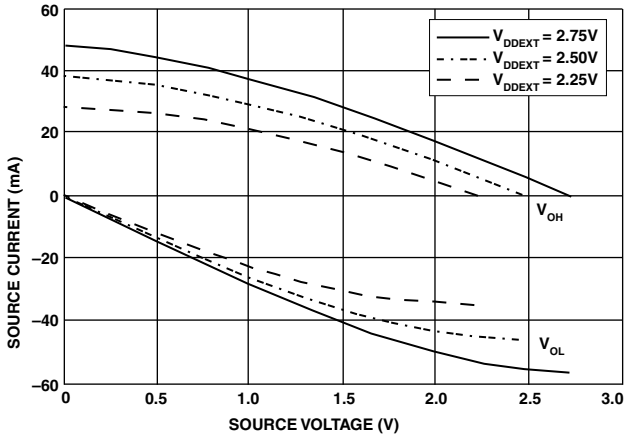

Figure 33. Drive Current C (Low V_{DDEXT})

In Table 32 through Table 34, airflow measurements comply with JEDEC standards JESD51–2 and JESD51–6, and the junction-to-board measurement complies with JESD51–8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Thermal resistance θ_{JA} in Table 32 through Table 34 is the figure of merit relating to performance of the package and board in a convective environment. θ_{JMA} represents the thermal resistance under two conditions of airflow. θ_{JB} represents the heat extracted from the periphery of the board. Ψ_{JT} represents the correlation between T_J and T_{CASE}. Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

Table 32. Thermal Characteristics for BC-256-4 (17 mm × 17 mm) Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	18.1	°C/W
θ_{JMA}	1 Linear m/s Airflow	15.9	°C/W
θ_{JMA}	2 Linear m/s Airflow	15.1	°C/W
θ_{JC}	Not Applicable	3.72	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.11	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.18	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.18	°C/W

Table 33. Thermal Characteristics for BC-256-1 (12 mm × 12 mm) Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	25.6	°C/W
θ_{JMA}	1 Linear m/s Airflow	22.4	°C/W
θ_{JMA}	2 Linear m/s Airflow	21.6	°C/W
θ_{JB}	Not Applicable	18.9	°C/W
θ_{JC}	Not Applicable	4.85	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.15	°C/W
Ψ_{JT}	1 Linear m/s Airflow	n/a	°C/W
Ψ_{JT}	2 Linear m/s Airflow	n/a	°C/W

Table 34. Thermal Characteristics for B-297 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	20.6	°C/W
θ_{JMA}	1 Linear m/s Airflow	17.8	°C/W
θ_{JMA}	2 Linear m/s Airflow	17.4	°C/W
θ_{JB}	Not Applicable	16.3	°C/W
θ_{JC}	Not Applicable	7.15	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.37	°C/W
Ψ_{JT}	1 Linear m/s Airflow	n/a	°C/W
Ψ_{JT}	2 Linear m/s Airflow	n/a	°C/W

256-BALL CSP_BGA (17 mm) BALL ASSIGNMENT

Table 35 lists the 256-Ball CSP_BGA (17 mm × 17 mm) ball assignment by ball number. Table 36 on Page 48 lists the ball assignment alphabetically by signal.

Table 35. 256-Ball CSP_BGA (17 mm × 17 mm) Ball Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	VDDEXT	C9	$\overline{\text{SMS3}}$	F1	CLKIN	H9	GND	L1	PPI0D3
A2	ADDR22	C10	$\overline{\text{SWE}}$	F2	PPI0D10	H10	GND	L2	PPI0D2
A3	ADDR18	C11	SA10	F3	$\overline{\text{RESET}}$	H11	GND	L3	PPI0D1
A4	ADDR14	C12	$\overline{\text{ABE0}}$	F4	BYPASS	H12	GND	L4	PPI0D0
A5	ADDR11	C13	ADDR07	F5	VDDEXT	H13	GND	L5	VDDEXT
A6	$\overline{\text{AMS3}}$	C14	ADDR04	F6	VDDEXT	H14	DATA21	L6	VDDEXT
A7	$\overline{\text{AMS0}}$	C15	DATA0	F7	VDDEXT	H15	DATA19	L7	VDDEXT
A8	ARDY	C16	DATA05	F8	GND	H16	DATA23	L8	VDDEXT
A9	$\overline{\text{SMS2}}$	D1	PPI0D15	F9	GND	J1	VROUT1	L9	GND
A10	SCLK0	D2	PPI0SYNC3	F10	VDDEXT	J2	PPI0D8	L10	VDDEXT
A11	SCLK1	D3	PPI0SYNC2	F11	VDDEXT	J3	PPI0D7	L11	VDDEXT
A12	$\overline{\text{ABE2}}$	D4	ADDR21	F12	VDDEXT	J4	PPI0D9	L12	VDDEXT
A13	$\overline{\text{ABE3}}$	D5	ADDR15	F13	DATA11	J5	GND	L13	NC
A14	ADDR06	D6	ADDR09	F14	DATA08	J6	GND	L14	DT0PRI
A15	ADDR03	D7	$\overline{\text{AWE}}$	F15	DATA10	J7	GND	L15	DATA31
A16	VDDEXT	D8	$\overline{\text{SMS0}}$	F16	DATA16	J8	GND	L16	DATA28
B1	ADDR24	D9	$\overline{\text{SRAS}}$	G1	XTAL	J9	GND	M1	PPI1SYNC2
B2	ADDR23	D10	$\overline{\text{SCAS}}$	G2	VDDEXT	J10	GND	M2	PPI1D15
B3	ADDR19	D11	$\overline{\text{BGH}}$	G3	VDDEXT	J11	GND	M3	PPI1D14
B4	ADDR17	D12	$\overline{\text{ABE1}}$	G4	GND	J12	VDDINT	M4	PPI1D9
B5	ADDR12	D13	DATA02	G5	GND	J13	VDDINT	M5	VDDINT
B6	ADDR10	D14	DATA01	G6	VDDEXT	J14	DATA20	M6	VDDINT
B7	$\overline{\text{AMS1}}$	D15	DATA03	G7	GND	J15	DATA22	M7	GND
B8	$\overline{\text{AOE}}$	D16	DATA07	G8	GND	J16	DATA24	M8	VDDINT
B9	$\overline{\text{SMS1}}$	E1	PPI0D11	G9	GND	K1	PPI0D6	M9	GND
B10	SCKE	E2	PPI0D13	G10	GND	K2	PPI0D5	M10	VDDINT
B11	$\overline{\text{BR}}$	E3	PPI0D12	G11	VDDEXT	K3	PPI0D4	M11	GND
B12	$\overline{\text{BG}}$	E4	PPI0D14	G12	VDDEXT	K4	PPI1SYNC3	M12	VDDINT
B13	ADDR08	E5	PPI1CLK	G13	DATA17	K5	VDDEXT	M13	RSCLK0
B14	ADDR05	E6	VDDINT	G14	DATA14	K6	VDDEXT	M14	DR0PRI
B15	ADDR02	E7	GND	G15	DATA15	K7	GND	M15	TSCLK0
B16	DATA04	E8	VDDINT	G16	DATA18	K8	GND	M16	DATA29
C1	PPI0SYNC1	E9	GND	H1	VROUT0	K9	GND	N1	PPI1SYNC1
C2	ADDR25	E10	VDDINT	H2	GND	K10	GND	N2	PPI1D10
C3	PPI0CLK	E11	GND	H3	GND	K11	VDDEXT	N3	PPI1D7
C4	ADDR20	E12	VDDINT	H4	VDDINT	K12	GND	N4	PPI1D5
C5	ADDR16	E13	DATA06	H5	VDDINT	K13	GND	N5	PF0
C6	ADDR13	E14	DATA13	H6	GND	K14	DATA26	N6	PF04
C7	$\overline{\text{AMS2}}$	E15	DATA09	H7	GND	K15	DATA25	N7	PF09
C8	$\overline{\text{ARE}}$	E16	DATA12	H8	GND	K16	DATA27	N8	PF12

Figure 50 lists the top view of the 256-Ball CSP_BGA (12 mm × 12 mm) ball configuration. Figure 51 lists the bottom view.

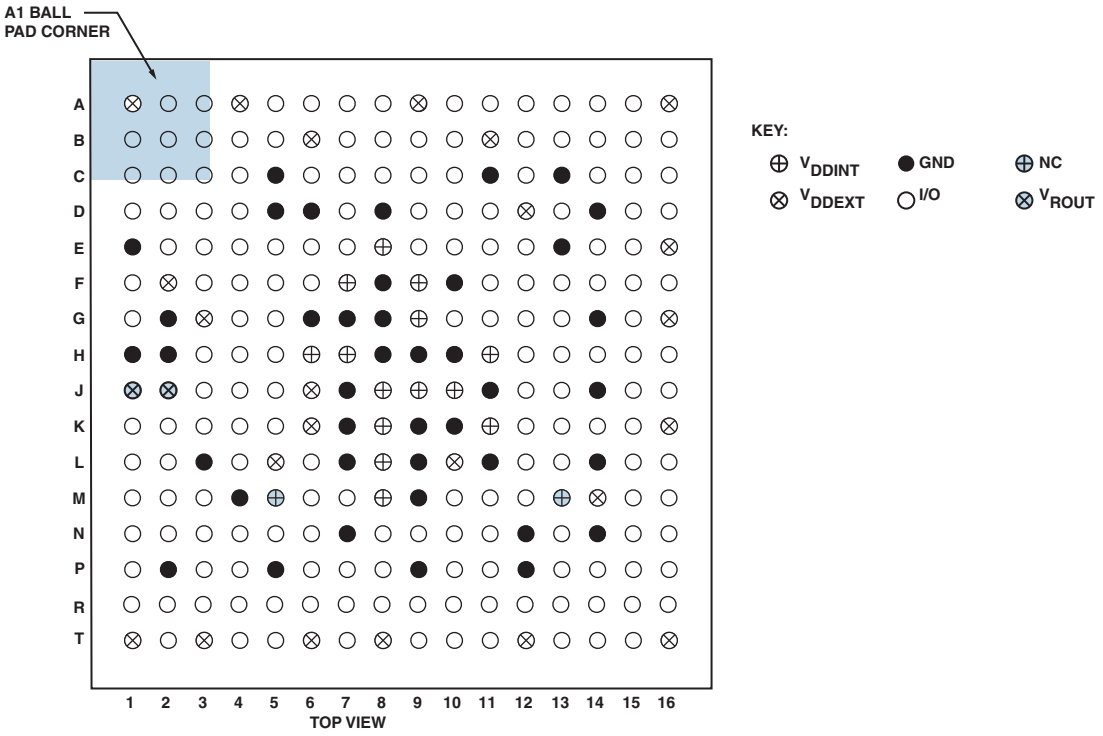

Figure 50. 256-Ball CSP_BGA Ball Configuration (Top View)

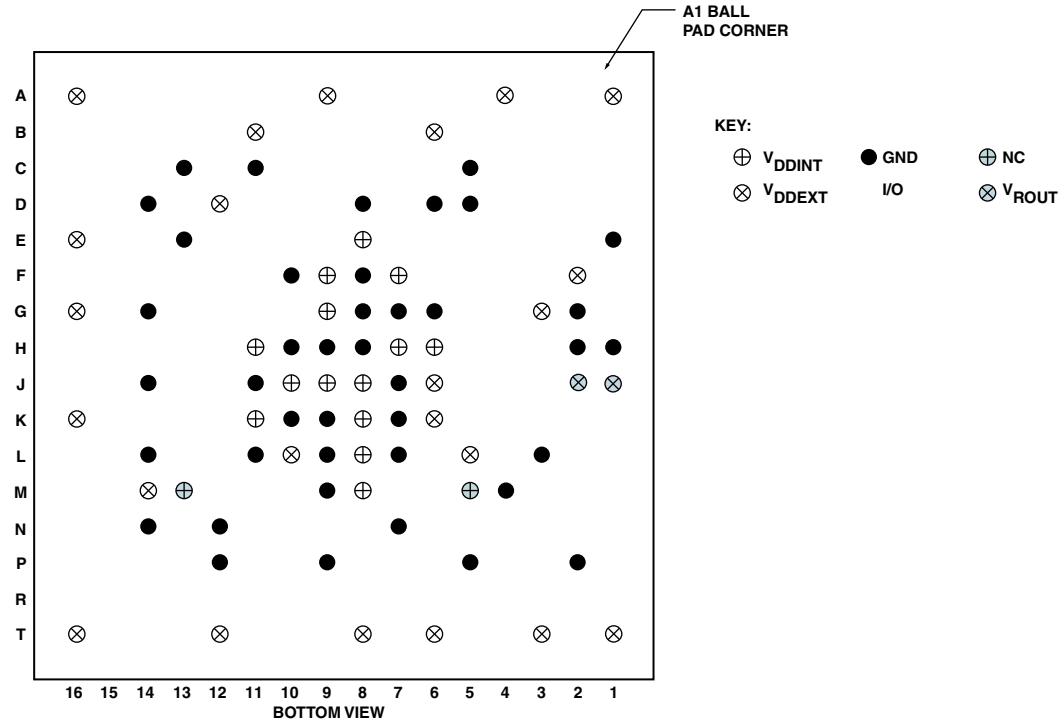

Figure 51. 256-Ball CSP_BGA Ball Configuration (Bottom View)

297-BALL PBGA BALL ASSIGNMENT

Table 39 lists the 297-Ball PBGA ball assignment numerically by ball number. Table 40 on Page 58 lists the ball assignment alphabetically by signal.

Table 39. 297-Ball PBGA Ball Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A01	GND	B15	$\overline{\text{SMS1}}$	G01	PPI0D11	L14	GND
A02	ADDR25	B16	$\overline{\text{SMS3}}$	G02	PPI0D10	L15	GND
A03	ADDR23	B17	SCKE	G25	DATA4	L16	GND
A04	ADDR21	B18	$\overline{\text{SWE}}$	G26	DATA7	L17	GND
A05	ADDR19	B19	SA10	H01	BYPASS	L18	VDDINT
A06	ADDR17	B20	$\overline{\text{BR}}$	H02	$\overline{\text{RESET}}$	L25	DATA12
A07	ADDR15	B21	$\overline{\text{BG}}$	H25	DATA6	L26	DATA15
A08	ADDR13	B22	$\overline{\text{ABE1}}$	H26	DATA9	M01	VROUT0
A09	ADDR11	B23	$\overline{\text{ABE3}}$	J01	CLKIN	M02	GND
A10	ADDR09	B24	ADDR07	J02	GND	M10	VDDEXT
A11	$\overline{\text{AMS3}}$	B25	GND	J10	VDDEXT	M11	GND
A12	$\overline{\text{AMS1}}$	B26	ADDR05	J11	VDDEXT	M12	GND
A13	$\overline{\text{AWE}}$	C01	PPI0SYNC3	J12	VDDEXT	M13	GND
A14	$\overline{\text{ARE}}$	C02	PPI0CLK	J13	VDDEXT	M14	GND
A15	$\overline{\text{SMS0}}$	C03	GND	J14	VDDEXT	M15	GND
A16	$\overline{\text{SMS2}}$	C04	GND	J15	VDDEXT	M16	GND
A17	$\overline{\text{SRAS}}$	C05	GND	J16	VDDINT	M17	GND
A18	$\overline{\text{SCAS}}$	C22	GND	J17	VDDINT	M18	VDDINT
A19	SCLK0	C23	GND	J18	VDDINT	M25	DATA14
A20	SCLK1	C24	GND	J25	DATA8	M26	DATA17
A21	$\overline{\text{BGH}}$	C25	ADDR04	J26	DATA11	N01	VROUT1
A22	$\overline{\text{ABE0}}$	C26	ADDR03	K01	XTAL	N02	PPI0D9
A23	$\overline{\text{ABE2}}$	D01	PPI0SYNC1	K02	NC	N10	VDDEXT
A24	ADDR08	D02	PPI0SYNC2	K10	VDDEXT	N11	GND
A25	ADDR06	D03	GND	K11	VDDEXT	N12	GND
A26	GND	D04	GND	K12	VDDEXT	N13	GND
B01	PPI1CLK	D23	GND	K13	VDDEXT	N14	GND
B02	GND	D24	GND	K14	VDDEXT	N15	GND
B03	ADDR24	D25	ADDR02	K15	VDDEXT	N16	GND
B04	ADDR22	D26	DATA1	K16	VDDINT	N17	GND
B05	ADDR20	E01	PPI0D15	K17	VDDINT	N18	VDDINT
B06	ADDR18	E02	PPI0D14	K18	VDDINT	N25	DATA16
B07	ADDR16	E03	GND	K25	DATA10	N26	DATA19
B08	ADDR14	E24	GND	K26	DATA13	P01	PPI0D7
B09	ADDR12	E25	DATA0	L01	NC	P02	PPI0D8
B10	ADDR10	E26	DATA3	L02	NC	P10	VDDEXT
B11	$\overline{\text{AMS2}}$	F01	PPI0D13	L10	VDDEXT	P11	GND
B12	$\overline{\text{AMS0}}$	F02	PPI0D12	L11	GND	P12	GND
B13	$\overline{\text{AOE}}$	F25	DATA2	L12	GND	P13	GND
B14	ARDY	F26	DATA5	L13	GND	P14	GND

Table 39. 297-Ball PBGA Ball Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
P15	GND	U11	VDDEXT	AC04	GND	AE21	RX
P16	GND	U12	VDDEXT	AC23	GND	AE22	RFS1
P17	GND	U13	VDDEXT	AC24	GND	AE23	DR1SEC
P18	VDDINT	U14	GND	AC25	DR0SEC	AE24	TFS1
P25	DATA18	U15	VDDINT	AC26	RFS0	AE25	GND
P26	DATA21	U16	VDDINT	AD01	PPI1D7	AE26	NC
R01	PPI0D5	U17	VDDINT	AD02	PPI1D6	AF01	GND
R02	PPI0D6	U18	VDDINT	AD03	GND	AF02	PPI1D4
R10	VDDEXT	U25	DATA24	AD04	GND	AF03	PPI1D2
R11	GND	U26	DATA27	AD05	GND	AF04	PPI1D0
R12	GND	V01	PPI1SYNC3	AD22	GND	AF05	PF1
R13	GND	V02	PPI0D0	AD23	GND	AF06	PF3
R14	GND	V25	DATA26	AD24	GND	AF07	PF5
R15	GND	V26	DATA29	AD25	NC	AF08	PF7
R16	GND	W01	PPI1SYNC1	AD26	RSCLK0	AF09	PF9
R17	GND	W02	PPI1SYNC2	AE01	PPI1D5	AF10	PF11
R18	VDDINT	W25	DATA28	AE02	GND	AF11	PF13
R25	DATA20	W26	DATA31	AE03	PPI1D3	AF12	PF15
R26	DATA23	Y01	PPI1D15	AE04	PPI1D1	AF13	NMI1
T01	PPI0D3	Y02	PPI1D14	AE05	PF0	AF14	TCK
T02	PPI0D4	Y25	DATA30	AE06	PF2	AF15	TDI
T10	VDDEXT	Y26	DT0PRI	AE07	PF4	AF16	TMS
T11	GND	AA01	PPI1D13	AE08	PF6	AF17	SLEEP
T12	GND	AA02	PPI1D12	AE09	PF8	AF18	NMI0
T13	GND	AA25	DT0SEC	AE10	PF10	AF19	SCK
T14	GND	AA26	TSCLK0	AE11	PF12	AF20	TX
T15	GND	AB01	PPI1D11	AE12	PF14	AF21	RSCLK1
T16	GND	AB02	PPI1D10	AE13	NC	AF22	DR1PRI
T17	GND	AB03	GND	AE14	TDO	AF23	TSCLK1
T18	VDDINT	AB24	GND	AE15	$\overline{\text{TRST}}$	AF24	DT1SEC
T25	DATA22	AB25	TFS0	AE16	$\overline{\text{EMU}}$	AF25	DT1PRI
T26	DATA25	AB26	DR0PRI	AE17	BMODE1	AF26	GND
U01	PPI0D1	AC01	PPI1D9	AE18	BMODE0		
U02	PPI0D2	AC02	PPI1D8	AE19	MISO		
U10	VDDEXT	AC03	GND	AE20	MOSI		

Figure 52 lists the top view of the 297-Ball PBGA ball configuration. Figure 53 lists the bottom view.

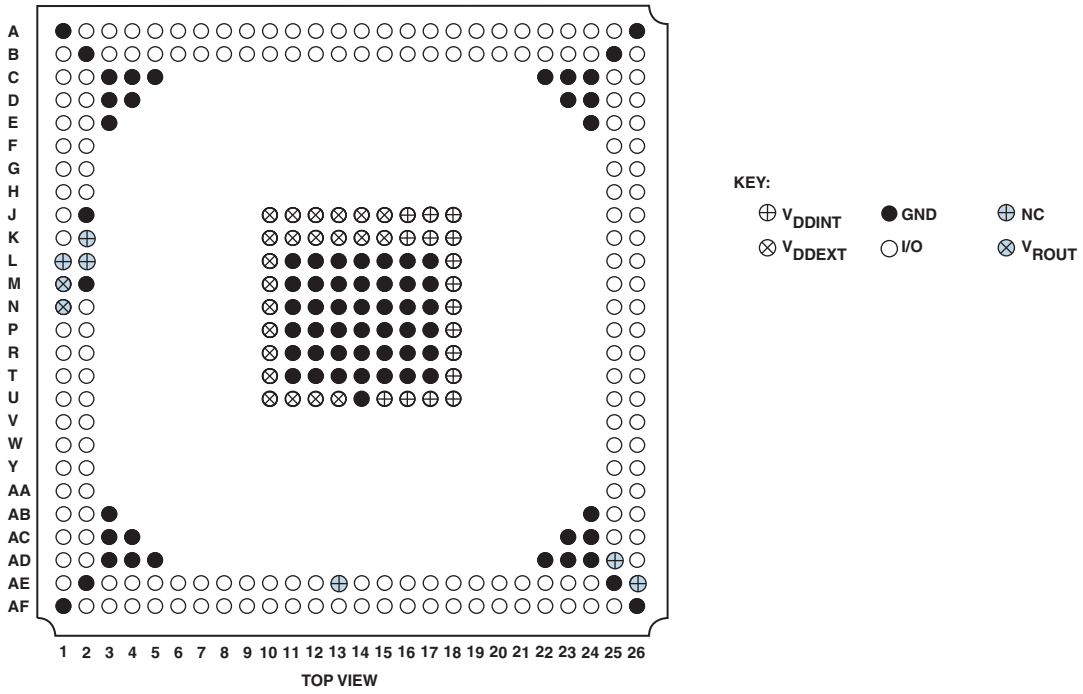

Figure 52. 297-Ball PBGA Ball Configuration (Top View)

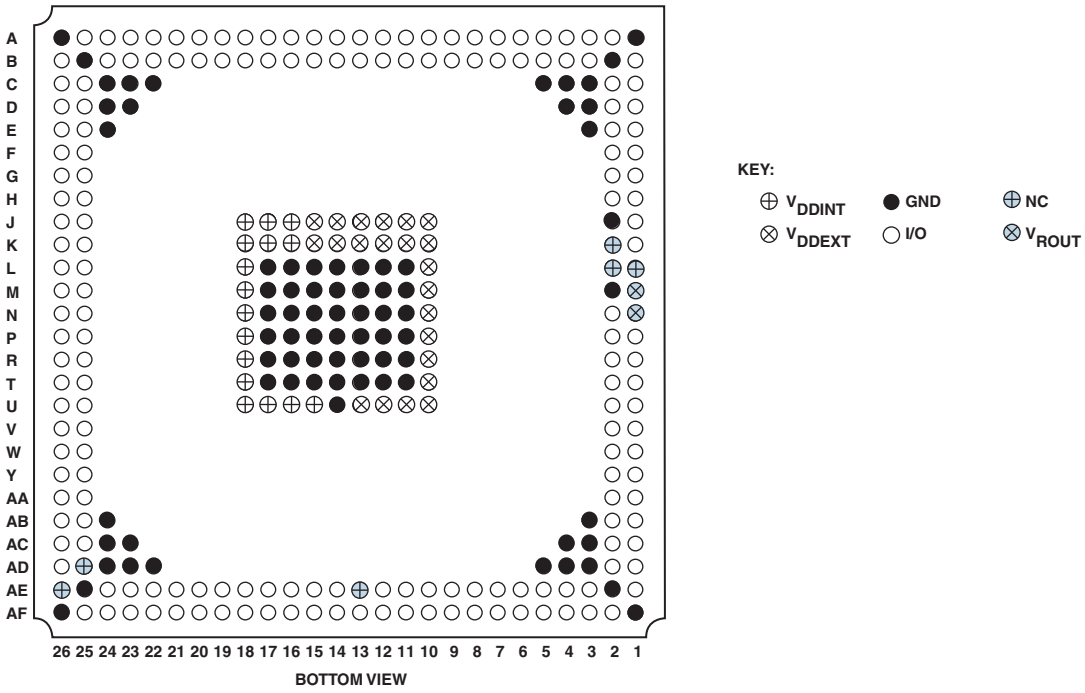

Figure 53. 297-Ball PBGA Ball Configuration (Bottom View)

OUTLINE DIMENSIONS

Dimensions in the outline dimension figures are shown in millimeters.

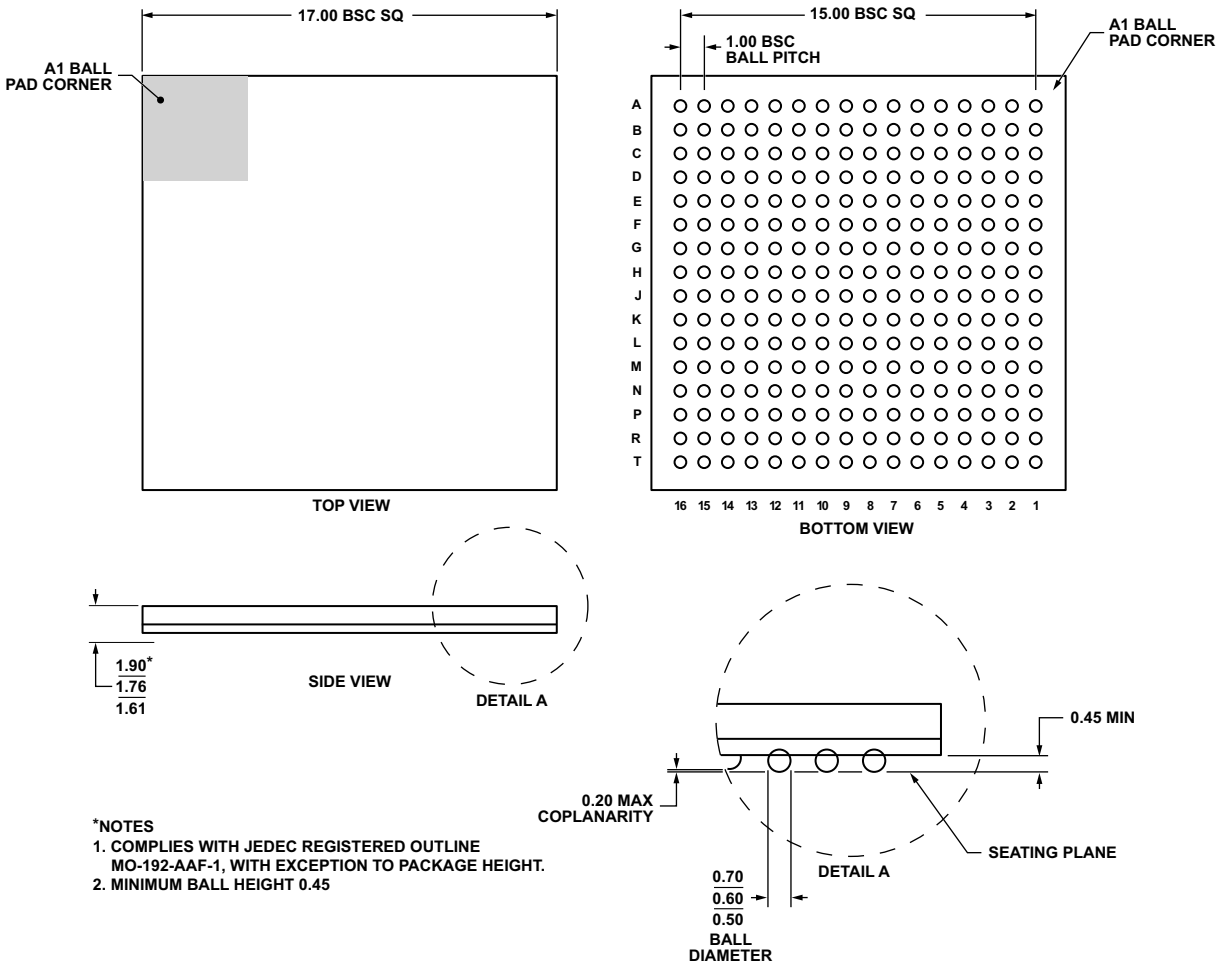

Figure 54. 256-Ball Chip Scale Package Ball Grid Array (CSP_BGA) (BC-256-4)