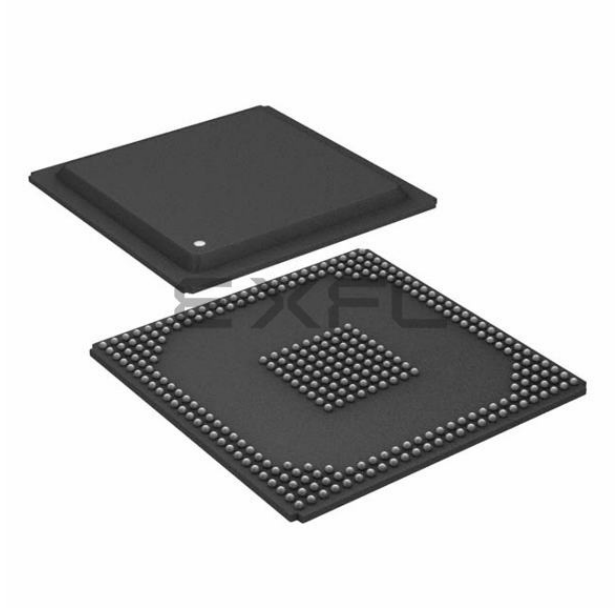

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	533MHz
Non-Volatile Memory	External
On-Chip RAM	328kB
Voltage - I/O	3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	297-BGA
Supplier Device Package	297-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf561wbbz505

- ADSP-BF561: Blackfin Embedded Symmetric Multiprocessor Data Sheet

Emulator Manuals

- HPUSB, USB, and HPPCI Emulator User's Guide
- ICE-1000/ICE-2000 Emulator User's Guide
- ICE-100B Emulator User's Guide

Evaluation Kit Manuals

- ADSP-BF561 EZ-KIT Lite® Evaluation System Manual
- Blackfin® A-V EZ-Extender® Manual
- Blackfin® EZ-Extender® Manual
- Blackfin® FPGA EZ-Extender® Manual
- Blackfin®/SHARC® USB EZ-Extender® Manual

Integrated Circuit Anomalies

- ADSP-BF561 Blackfin Anomaly List for Revisions 0.3, 0.5

Processor Manuals

- ADSP-BF561 Blackfin ® Processor Hardware Reference
- ADSP-BF5xx/ADSP-BF60x Blackfin® Processor Programming Reference
- Blackfin Processors: Manuals

Product Highlight

- ADSP-BF561 Blackfin Dual-Core Embedded Processor
- Blackfin Processor Family Product Highlight
- EZ-KIT Lite for Analog Devices ADSP-BF561 Blackfin Processor

Software Manuals

- CrossCore® Embedded Studio 2.5.0 Assembler and Preprocessor Manual
- CrossCore® Embedded Studio 2.5.0 C/C++ Compiler and Library Manual for Blackfin Processors
- CrossCore® Embedded Studio 2.5.0 Linker and Utilities Manual
- CrossCore® Embedded Studio 2.5.0 Loader and Utilities Manual
- CrossCore® Software Licensing Guide
- lwIP for CrossCore® Embedded Studio 1.0.0 User's Guide
- VisualDSP++® 5.0 Assembler and Preprocessor Manual
- VisualDSP++® 5.0 C/C++ Compiler and Library Manual for Blackfin Processors
- VisualDSP++® 5.0 Device Drivers and System Services Manual for Blackfin Processors
- VisualDSP++® 5.0 Kernel (VDK) Users Guide
- VisualDSP++® 5.0 Licensing Guide
- VisualDSP++® 5.0 Linker and Utilities Manual
- VisualDSP++® 5.0 Loader and Utilities Manual
- VisualDSP++® 5.0 Product Release Bulletin
- VisualDSP++® 5.0 Quick Installation Reference Card
- VisualDSP++® 5.0 Users Guide

SOFTWARE AND SYSTEMS REQUIREMENTS

- Software and Tools Anomalies Search

TOOLS AND SIMULATIONS

- ADSP-BF561 Blackfin Processor BSDL File 256-Ball CSP BGA Package
- ADSP-BF561 Blackfin Processor BSDL File 256-Ball Sparse CSP_BGA Package
- ADSP-BF561 Blackfin Processor BSDL File 297-Ball PBGA Package
- ADSP-BF561 Blackfin Processor Core B BSDL File All Packages
- Designing with BGA
- Blackfin Processors Software and Tools
- ADSP-BF561 Blackfin Processor IBIS Datafile for 12x12 CSP BGA Package (02/2008)
- ADSP-BF561 Blackfin Processor IBIS Datafile for 17x17 CSP BGA Package (11/2008)
- ADSP-BF561 Blackfin Processor IBIS Datafile for 27x27 PBGA Package (02/2008)

even though the event may be latched in the ILAT register. This register may be read from or written to while in supervisor mode.

Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.

- CEC Interrupt Pending Register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but may be read while in supervisor mode.

The SIC allows further control of event processing by providing six 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 2.

- SIC Interrupt Mask Registers (SIC_IMASKx) – These registers control the masking and unmasking of each peripheral interrupt event. When a bit is set in these registers, that peripheral event is unmasked and will be processed by the system when asserted. A cleared bit in these registers masks the peripheral event, thereby preventing the processor from servicing the event.
- SIC Interrupt Status Registers (SIC_ISRx) – As multiple peripherals can be mapped to a single event, these registers allow the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt; a cleared bit indicates the peripheral is not asserting the event.
- SIC Interrupt Wakeup Enable Registers (SIC_IWRx) – By enabling the corresponding bit in these registers, each peripheral can be configured to wake up the processor, should the processor be in a powered-down mode when the event is generated.

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC will recognize and queue the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the mode of the processor.

DMA CONTROLLERS

The ADSP-BF561 has two independent DMA controllers that support automated data transfers with minimal overhead for the DSP cores. DMA transfers can occur between the ADSP-BF561 internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the SPORTs, SPI port, UART, and PPIs. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The ADSP-BF561 DMA controllers support both 1-dimensional (1-D) and 2-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ± 32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the ADSP-BF561 DMA controllers include:

- A single linear buffer that stops upon completion.
- A circular autorefreshing buffer that interrupts on each full or fractionally full buffer.
- 1-D or 2-D DMA using a linked list of descriptors.
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page.

In addition to the dedicated peripheral DMA channels, each DMA Controller has four memory DMA channels provided for transfers between the various memories of the ADSP-BF561 system. These enable transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

Further, the ADSP-BF561 has a four channel Internal Memory DMA (IMDMA) Controller. The IMDMA Controller allows data transfers between any of the internal L1 and L2 memories.

WATCHDOG TIMER

Each ADSP-BF561 core includes a 32-bit timer, which can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state, via generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the timer control register, which is set only upon a watchdog generated reset.

The timer is clocked by the system clock (SCLK) at a maximum frequency of f_{SCLK}.

TIMERS

There are 14 programmable timer units in the ADSP-BF561.

Each of the 12 general-purpose timer units can be independently programmed as a Pulse Width Modulator (PWM), internally or externally clocked timer, or pulse width counter. The general-purpose timer units can be used in conjunction with the UART to measure the width of the pulses in the data stream to provide an autobaud detect function for a serial channel. The general-purpose timers can generate interrupts to the processor core providing periodic events for synchronization, either to the processor clock or to a count of external signals.

In addition to the 12 general-purpose programmable timers, another timer is also provided for each core. These extra timers are clocked by the internal processor clock (CCLK) and are typically used as a system tick clock for generation of operating system periodic interrupts.

SERIAL PORTS (SPORTs)

The ADSP-BF561 incorporates two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other DSP components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length – Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most significant bit first or least significant bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The DSP can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1,024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

An additional 250 mV of SPORT input hysteresis can be enabled by setting Bit 15 of the PLL_CTL register. When this bit is set, all SPORT input pins have the increased hysteresis.

SERIAL PERIPHERAL INTERFACE (SPI) PORT

The ADSP-BF561 processor has an SPI-compatible port that enables the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (master output-slave input, MOSI, and master input-slave output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin ($\overline{\text{SPISS}}$) lets other SPI devices select the processor, and seven SPI chip select output pins ($\overline{\text{SPISEL7–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured programmable flag pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface which supports both master/slave modes and multimaster environments.

The baud rate and clock phase/polarities for the SPI port are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI DMA controller can only service unidirectional accesses at any given time.

The SPI port clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

Where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORT

The ADSP-BF561 processor provides a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for 5 data bits to 8 data bits, 1 stop bit or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the Blackfin processor family. Third party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

EZ-KIT Lite Evaluation Board

For evaluation of ADSP-BF561 processors, use the ADSP-BF561 EZ-KIT Lite® board available from Analog Devices. Order part number ADDS-BF561-EZLITE. The board comes with on-chip emulation capabilities and is equipped to enable software development. Multiple daughter cards are available.

DESIGNING AN EMULATOR-COMPATIBLE PROCESSOR BOARD

The Analog Devices family of emulators are tools that every system developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on the ADSP-BF561. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the processor is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the processor's JTAG port to the emulator.

For details on target board design issues, including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see *Analog Devices JTAG Emulation Technical Reference (EE-68)* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

RELATED DOCUMENTS

The following publications that describe the ADSP-BF561 processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started With Blackfin Processors*
- *ADSP-BF561 Blackfin Processor Hardware Reference*
- *ADSP-BF53x/BF56x Blackfin Processor Programming Reference*
- ADSP-BF561 *Blackfin Processor Anomaly List*

Table 8. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
PF/SPI/TIMER			
PF0/*SPISS*/*TMR0*	I/O	Programmable Flag/*Slave SPI Select/Timer*	C
PF1/*SPISEL1*/*TMR1*	I/O	Programmable Flag/*SPI Select/Timer*	C
PF2/*SPISEL2*/*TMR2*	I/O	Programmable Flag/*SPI Select/Timer*	C
PF3/*SPISEL3*/*TMR3*	I/O	Programmable Flag/*SPI Select/Timer*	C
PF4/*SPISEL4*/*TMR4*	I/O	Programmable Flag/*SPI Select/Timer*	C
PF5/*SPISEL5*/*TMR5*	I/O	Programmable Flag/*SPI Select/Timer*	C
PF6/*SPISEL6*/*TMR6*	I/O	Programmable Flag/*SPI Select/Timer*	C
PF7/*SPISEL7*/*TMR7*	I/O	Programmable Flag/*SPI Select/Timer*	C
PF8	I/O	Programmable Flag	C
PF9	I/O	Programmable Flag	C
PF10	I/O	Programmable Flag	C
PF11	I/O	Programmable Flag	C
PF12	I/O	Programmable Flag	C
PF13	I/O	Programmable Flag	C
PF14	I/O	Programmable Flag	C
PF15/*EXT CLK*	I/O	Programmable Flag/*External Timer Clock Input*	C
PPI0			
PPI0D15–8/*PF47–40*	I/O	PPI Data/*Programmable Flag Pins*	C
PPI0D7–0	I/O	PPI Data Pins	C
PPI0CLK	I	PPI Clock	
PPI0SYNC1/*TMR8*	I/O	PPI Sync/*Timer*	C
PPI0SYNC2/*TMR9*	I/O	PPI Sync/*Timer*	C
PPI0SYNC3	I/O	PPI Sync	C
PPI1			
PPI1D15–8/*PF39–32*	I/O	PPI Data/*Programmable Flag Pins*	C
PPI1D7–0	I/O	PPI Data Pins	C
PPI1CLK	I	PPI Clock	
PPI1SYNC1/*TMR10*	I/O	PPI Sync/*Timer*	C
PPI1SYNC2/*TMR11*	I/O	PPI Sync/*Timer*	C
PPI1SYNC3	I/O	PPI Sync	C
SPORT0			
RSCLK0/*PF28*	I/O	Sport0 Receive Serial Clock/*Programmable Flag*	D
RFS0/*PF19*	I/O	Sport0 Receive Frame Sync/*Programmable Flag*	C
DR0PRI	I	Sport0 Receive Data Primary	
DR0SEC/*PF20*	I/O	Sport0 Receive Data Secondary/*Programmable Flag*	C
TSCLK0/*PF29*	I/O	Sport0 Transmit Serial Clock/*Programmable Flag*	D
TFS0/*PF16*	I/O	Sport0 Transmit Frame Sync/*Programmable Flag*	C
DT0PRI/*PF18*	I/O	Sport0 Transmit Data Primary/*Programmable Flag*	C
DT0SEC/*PF17*	I/O	Sport0 Transmit Data Secondary/*Programmable Flag*	C

Asynchronous Memory Write Cycle Timing

Table 19. Asynchronous Memory Write Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
Switching Characteristics				
t_{DDAT}	DATA31–0 Disable After CLKOUT		6.0	ns
t_{ENDAT}	DATA31–0 Enable After CLKOUT	1.0		ns
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE3-0}$, ADDR25–2, DATA31–0, $\overline{AOE}$, $\overline{AWE}$.

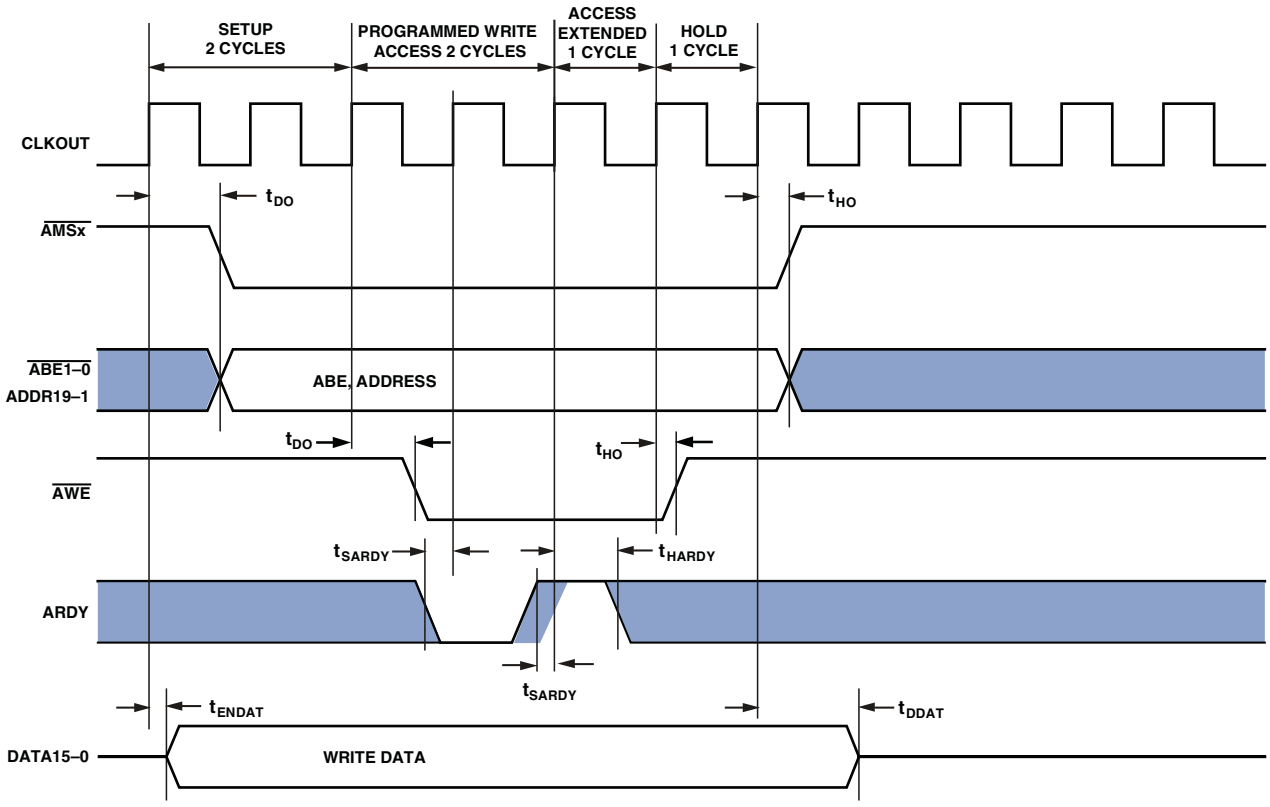

Figure 11. Asynchronous Memory Write Cycle Timing

SDRAM Interface Timing

Table 20. SDRAM Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDAT}	DATA Setup Before CLKOUT	1.5		ns
t_{HSDAT}	DATA Hold After CLKOUT	0.8		ns
Switching Characteristics				
t_{DCAD}	Command, ADDR, Data Delay After CLKOUT[1]		4.0	ns
t_{HCAD}	Command, ADDR, Data Hold After CLKOUT[1]	0.8		ns
t_{DSDAT}	Data Disable After CLKOUT		4.0	ns
t_{ENSDAT}	Data Enable After CLKOUT	1.0		ns
t_{SCLK}	CLKOUT Period	7.5		ns
t_{SCLKH}	CLKOUT Width High	2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		ns

[1] Command pins include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS3–0}$, SA10, SCKE.

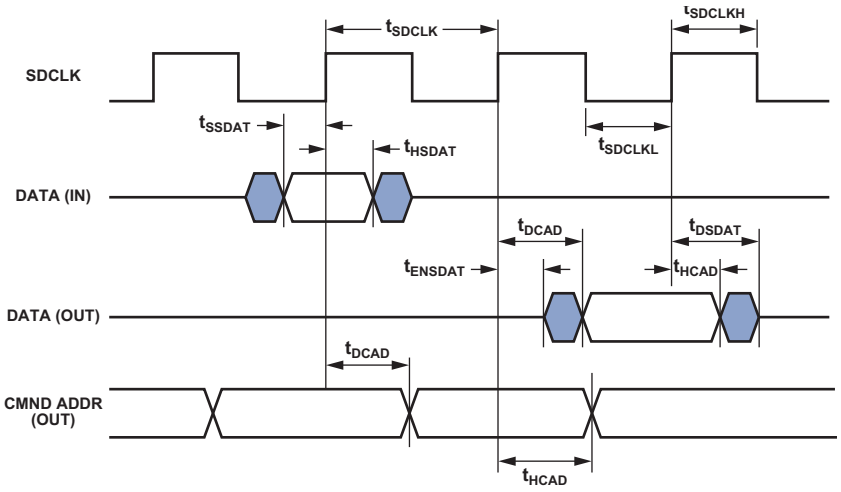

Figure 12. SDRAM Interface Timing

Parallel Peripheral Interface Timing

Table 22, and Figure 14 through Figure 17 on Page 30, describe default Parallel Peripheral Interface operations.

If bit 4 of the PLL_CTL register is set, then Figure 18 on Page 30 and Figure 19 on Page 31 apply.

Table 22. Parallel Peripheral Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	PPIxCLK Width[1]	5.0		ns
t_{PCLK}	PPIxCLK Period[1]	13.3		ns
t_{SFSPE}	External Frame Sync Setup Before PPIxCLK	4.0		ns
t_{HFSPE}	External Frame Sync Hold After PPIxCLK	1.0		ns
t_{SDRPE}	Receive Data Setup Before PPIxCLK	3.5		ns
t_{HDRPE}	Receive Data Hold After PPIxCLK	2.0		ns
Switching Characteristics				
t_{DFSPE}	Internal Frame Sync Delay After PPIxCLK		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPIxCLK	1.7		ns
t_{DDTPE}	Transmit Data Delay After PPIxCLK		8.0	ns
t_{HDTPE}	Transmit Data Hold After PPIxCLK	2.0		ns

[1] For PPI modes that use an internally generated frame sync, the PPIxCLK frequency cannot exceed $f_{SCLK}/2$. For modes with no frame syncs or external frame syncs, PPIxCLK cannot exceed 75 MHz and f_{SCLK} should be equal to or greater than PPIxCLK.

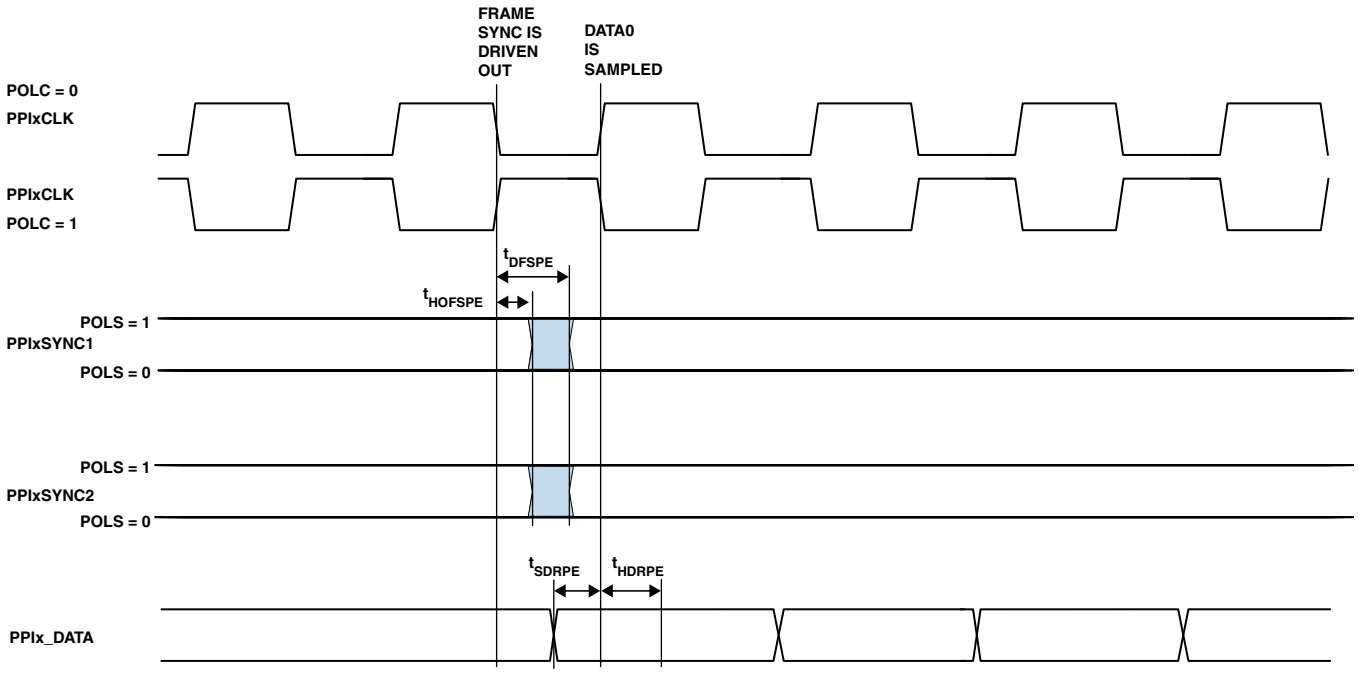

Figure 14. PPI GP Rx Mode with Internal Frame Sync Timing (Default)

Serial Peripheral Interface (SPI) Port— Master Timing

Table 27 and Figure 23 describe SPI port master operations.

Table 27. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	7.5		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		ns
Switching Characteristics				
t_{SDSCIM}	$\overline{SPISELx}$ Low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISELx}$ High	$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)	0	6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1.0	+4.0	ns

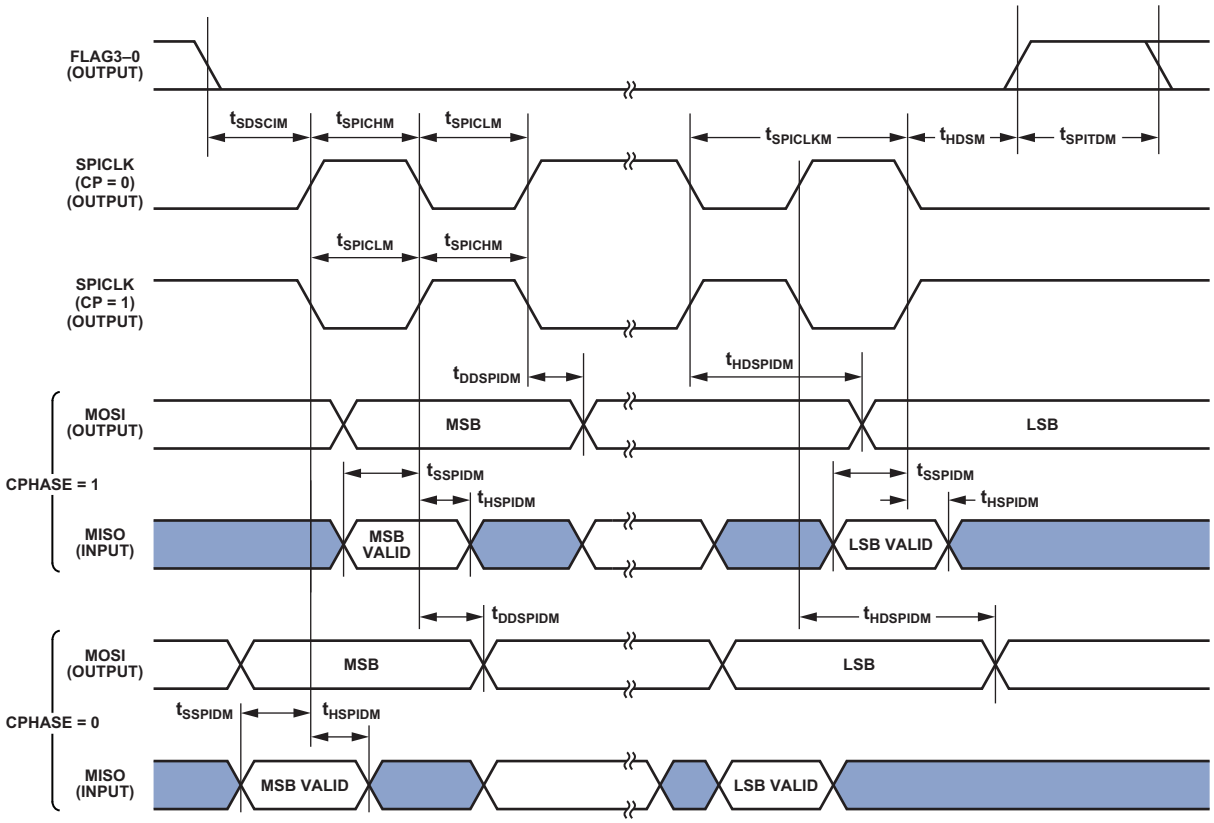

Figure 23. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port— Slave Timing

Table 28 and Figure 24 describe SPI port slave operations.

Table 28. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	8	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0	8	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)	0	10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0	10	ns

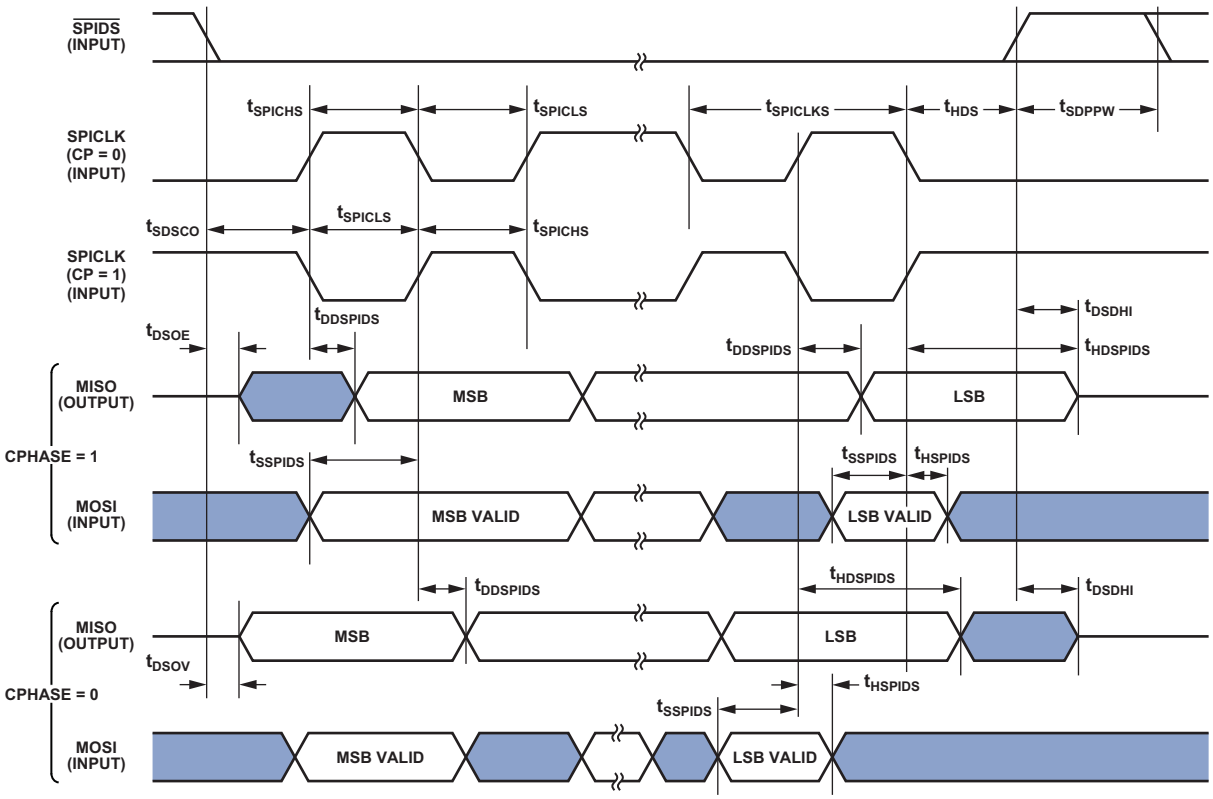

Figure 24. Serial Peripheral Interface (SPI) Port—Slave Timing

JTAG Test and Emulation Port Timing

Table 31 and Figure 28 describe JTAG port operations.

Table 31. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Parameters				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	5		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width[2] (Measured in TCK Cycles)	4		TCK
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	12	ns

[1] System Inputs = DATA31–0, ARDY, PF47–0, PPI0CLK, PPI1CLK, RSCLK0–1, RFS0–1, DR0PRI, DR0SEC, TSCLK0–1, TFS0–1, DR1PRI, DR1SEC, MOSI, MISO, SCK, RX, $\overline{\text{RESET}}$, NMI0, NMI1, BMODE1–0, $\overline{\text{BR}}$, and PPIxD7–0.

[2] 50 MHz maximum

[3] System Outputs = DATA31–0, ADDR25–2, $\overline{\text{ABE3–0}}$, $\overline{\text{AOE}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, $\overline{\text{AMS3–0}}$, $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$, $\overline{\text{SWE}}$, SCKE, CLKOUT, SA10, $\overline{\text{SMS3–0}}$, PF47–0, RSCLK0–1, RFS0–1, TSCLK0–1, TFS0–1, DT0PRI, DT0SEC, DT1PRI, DT1SEC, MOSI, MISO, SCK, TX, $\overline{\text{BG}}$, $\overline{\text{BGH}}$, and PPIxD7–0.

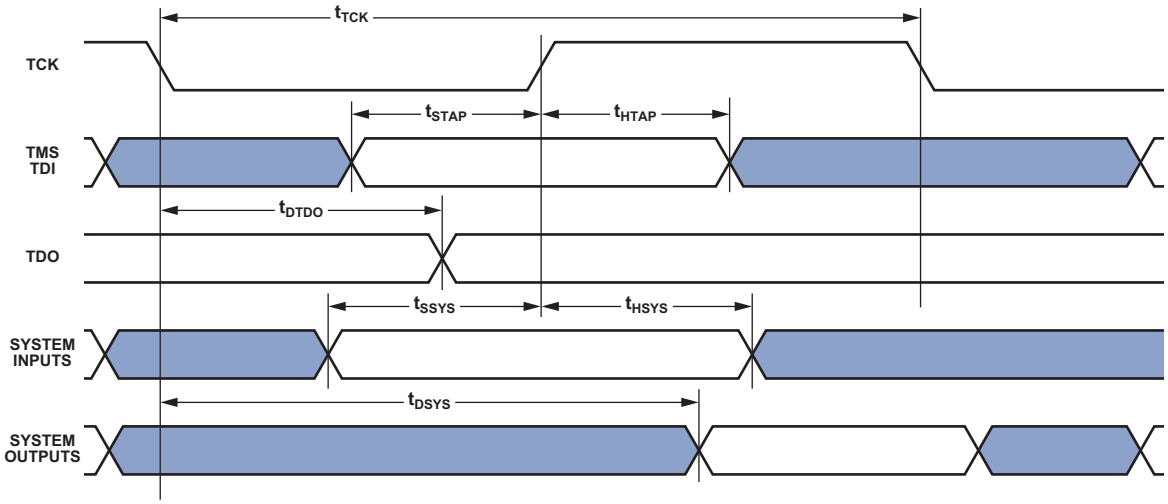

Figure 28. JTAG Port Timing

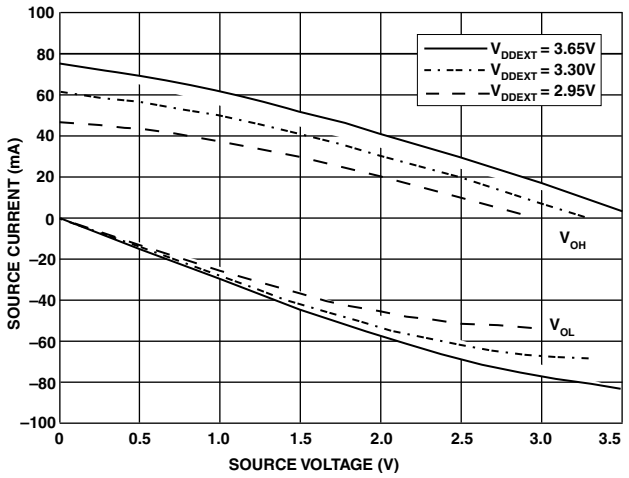

Figure 34. Drive Current C (High V_{DDEXT})

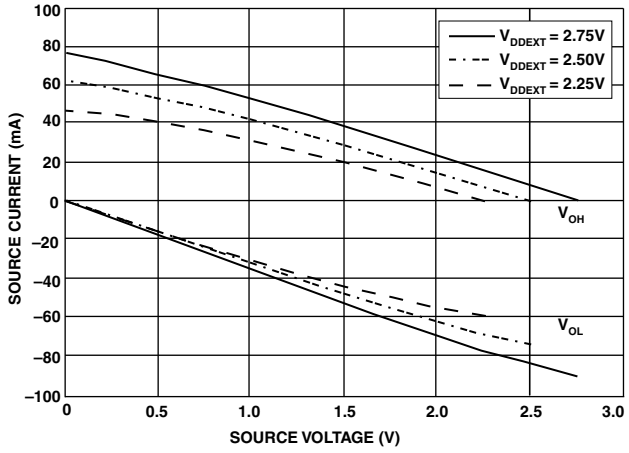

Figure 35. Drive Current D (Low V_{DDEXT})

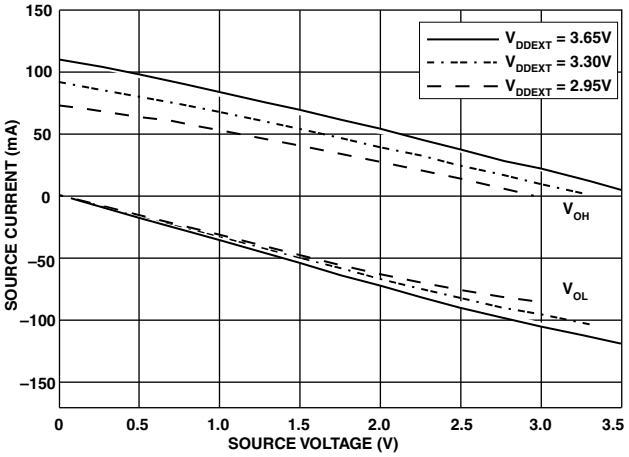

Figure 36. Drive Current D (High V_{DDEXT})

POWER DISSIPATION

Many operating conditions can affect power dissipation. System designers should refer to *Estimating Power for ADSP-BF561 Blackfin Processors (EE-293)* on the Analog Devices website (www.analog.com)—use site search on "EE-293." This document provides detailed information for optimizing your design for lowest power.

See the *ADSP-BF561 Blackfin Processor Hardware Reference Manual* for definitions of the various operating modes and for instructions on how to minimize system power.

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 37 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V.

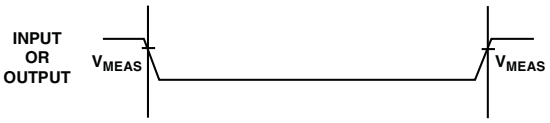

Figure 37. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 38 on Page 43.

The time $t_{ENA\_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches V_{TRIP}(high) or V_{TRIP}(low). V_{TRIP}(high) is 2.0 V and V_{TRIP}(low) is 1.0 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V. Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP}(high) or V_{TRIP}(low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 38 on Page 43.

$$t_{DIS} = t_{DIS\_MEASURED} - t_{DECAY}$$

In Table 32 through Table 34, airflow measurements comply with JEDEC standards JESD51–2 and JESD51–6, and the junction-to-board measurement complies with JESD51–8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Thermal resistance θ_{JA} in Table 32 through Table 34 is the figure of merit relating to performance of the package and board in a convective environment. θ_{JMA} represents the thermal resistance under two conditions of airflow. θ_{JB} represents the heat extracted from the periphery of the board. Ψ_{JT} represents the correlation between T_J and T_{CASE}. Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

Table 32. Thermal Characteristics for BC-256-4 (17 mm × 17 mm) Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	18.1	°C/W
θ_{JMA}	1 Linear m/s Airflow	15.9	°C/W
θ_{JMA}	2 Linear m/s Airflow	15.1	°C/W
θ_{JC}	Not Applicable	3.72	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.11	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.18	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.18	°C/W

Table 33. Thermal Characteristics for BC-256-1 (12 mm × 12 mm) Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	25.6	°C/W
θ_{JMA}	1 Linear m/s Airflow	22.4	°C/W
θ_{JMA}	2 Linear m/s Airflow	21.6	°C/W
θ_{JB}	Not Applicable	18.9	°C/W
θ_{JC}	Not Applicable	4.85	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.15	°C/W
Ψ_{JT}	1 Linear m/s Airflow	n/a	°C/W
Ψ_{JT}	2 Linear m/s Airflow	n/a	°C/W

Table 34. Thermal Characteristics for B-297 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	20.6	°C/W
θ_{JMA}	1 Linear m/s Airflow	17.8	°C/W
θ_{JMA}	2 Linear m/s Airflow	17.4	°C/W
θ_{JB}	Not Applicable	16.3	°C/W
θ_{JC}	Not Applicable	7.15	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.37	°C/W
Ψ_{JT}	1 Linear m/s Airflow	n/a	°C/W
Ψ_{JT}	2 Linear m/s Airflow	n/a	°C/W

Table 35. 256-Ball CSP_BGA (17 mm × 17 mm) Ball Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
N9	GND	P5	PF01	R1	PPI1D12	R13	RSCLK1	T9	TDO
N10	BMODE1	P6	PF06	R2	PPI1D11	R14	TSCLK1	T10	TDI
N11	BMODE0	P7	PF08	R3	PPI1D4	R15	NC	T11	$\overline{\text{EMU}}$
N12	RX	P8	PF15	R4	PPI1D1	R16	TFS0	T12	MISO
N13	DR1SEC	P9	NMI1	R5	PF02	T1	VDDEXT	T13	TX
N14	DT1SEC	P10	TMS	R6	PF07	T2	NC	T14	DR1PRI
N15	RFS0	P11	NMI0	R7	PF11	T3	PPI1D3	T15	DT1PRI
N16	DATA30	P12	SCK	R8	PF14	T4	PPI1D2	T16	VDDEXT
P1	PPI1D13	P13	RFS1	R9	TCK	T5	PF03		
P2	PPI1D8	P14	TFS1	R10	$\overline{\text{TRST}}$	T6	PF05		
P3	PPI1D6	P15	DR0SEC	R11	SLEEP	T7	PF10		
P4	PPI1D0	P16	DT0SEC	R12	MOSI	T8	PF13		

Table 36. 256-Ball CSP_BGA (17 mm × 17 mm) Ball Assignment (Alphabetically by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{ABE0}$	C12	$\overline{BR}$	B11	DT0SEC	P16	GND	M9	PPI0D13	E2
$\overline{ABE1}$	D12	BYPASS	F4	DT1PRI	T15	GND	M11	PPI0D14	E4
$\overline{ABE2}$	A12	CLKIN	F1	DT1SEC	N14	GND	N9	PPI0D15	D1
$\overline{ABE3}$	A13	DATA0	C15	$\overline{EMU}$	T11	MISO	T12	PPI0SYNC1	C1
ADDR02	B15	DATA01	D14	GND	E7	MOSI	R12	PPI0SYNC2	D3
ADDR03	A15	DATA02	D13	GND	E9	NC	L13	PPI0SYNC3	D2
ADDR04	C14	DATA03	D15	GND	E11	NC	R15	PPI1CLK	E5
ADDR05	B14	DATA04	B16	GND	F8	NC	T2	PPI1D0	P4
ADDR06	A14	DATA05	C16	GND	F9	NMI0	P11	PPI1D1	R4
ADDR07	C13	DATA06	E13	GND	G4	NMI1	P9	PPI1D2	T4
ADDR08	B13	DATA07	D16	GND	G5	PF0	N5	PPI1D3	T3
ADDR09	D6	DATA08	F14	GND	G7	PF01	P5	PPI1D4	R3
ADDR10	B6	DATA09	E15	GND	G8	PF02	R5	PPI1D5	N4
ADDR11	A5	DATA10	F15	GND	G9	PF03	T5	PPI1D6	P3
ADDR12	B5	DATA11	F13	GND	G10	PF04	N6	PPI1D7	N3
ADDR13	C6	DATA12	E16	GND	H2	PF05	T6	PPI1D8	P2
ADDR14	A4	DATA13	E14	GND	H3	PF06	P6	PPI1D9	M4
ADDR15	D5	DATA14	G14	GND	H6	PF07	R6	PPI1D10	N2
ADDR16	C5	DATA15	G15	GND	H7	PF08	P7	PPI1D11	R2
ADDR17	B4	DATA16	F16	GND	H8	PF09	N7	PPI1D12	R1
ADDR18	A3	DATA17	G13	GND	H9	PF10	T7	PPI1D13	P1
ADDR19	B3	DATA18	G16	GND	H10	PF11	R7	PPI1D14	M3
ADDR20	C4	DATA19	H15	GND	H11	PF12	N8	PPI1D15	M2
ADDR21	D4	DATA20	J14	GND	H12	PF13	T8	PPI1SYNC1	N1
ADDR22	A2	DATA21	H14	GND	H13	PF14	R8	PPI1SYNC2	M1
ADDR23	B2	DATA22	J15	GND	J5	PF15	P8	PPI1SYNC3	K4
ADDR24	B1	DATA23	H16	GND	J6	PPI0CLK	C3	$\overline{RESET}$	F3
ADDR25	C2	DATA24	J16	GND	J7	PPI0D0	L4	RFS0	N15
$\overline{AMS0}$	A7	DATA25	K15	GND	J8	PPI0D1	L3	RFS1	P13
$\overline{AMS1}$	B7	DATA26	K14	GND	J9	PPI0D2	L2	RSCLK0	M13
$\overline{AMS2}$	C7	DATA27	K16	GND	J10	PPI0D3	L1	RSCLK1	R13
$\overline{AMS3}$	A6	DATA28	L16	GND	J11	PPI0D4	K3	RX	N12
$\overline{AOE}$	B8	DATA29	M16	GND	K7	PPI0D5	K2	SA10	C11
ARDY	A8	DATA30	N16	GND	K8	PPI0D6	K1	$\overline{SCAS}$	D10
$\overline{ARE}$	C8	DATA31	L15	GND	K9	PPI0D7	J3	SCK	P12
$\overline{AWE}$	D7	DR0PRI	M14	GND	K10	PPI0D8	J2	SCKE	B10
$\overline{BG}$	B12	DR0SEC	P15	GND	K12	PPI0D9	J4	SCLK0	A10
$\overline{BGH}$	D11	DR1PRI	T14	GND	K13	PPI0D10	F2	SCLK1	A11
BMODE0	N11	DR1SEC	N13	GND	L9	PPI0D11	E1	SLEEP	R11
BMODE1	N10	DT0PRI	L14	GND	M7	PPI0D12	E3	$\overline{SMS0}$	D8

Table 37. 256-Ball CSP_BGA (12 mm × 12 mm) Ball Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
N09	TDO	P05	GND	R01	PPI1D7	R13	TX/PF26	T09	TCK
N10	BMODE1	P06	PF5	R02	PPI1D6	R14	TSCLK1	T10	TMS
N11	MOSI	P07	PF11	R03	PPI1D2	R15	DT1PRI	T11	SLEEP
N12	GND	P08	PF15	R04	PPI1D0	R16	RFS0	T12	VDDEXT
N13	RFS1	P09	GND	R05	PF4	T01	VDDEXT	T13	RX/PF27
N14	GND	P10	$\overline{\text{TRST}}$	R06	PF8	T02	PPI1D4	T14	DR1SEC
N15	DT0SEC	P11	NMI0	R07	PF10	T03	VDDEXT	T15	DT1SEC
N16	TSCLK0	P12	GND	R08	PF14	T04	PF2	T16	VDDEXT
P01	PPI1D8	P13	RSCLK1	R09	NMI1	T05	PF6		
P02	GND	P14	TFS1	R10	TDI	T06	VDDEXT		
P03	PPI1D5	P15	RSCLK0	R11	$\overline{\text{EMU}}$	T07	PF12		
P04	PF0	P16	DR0SEC	R12	MISO	T08	VDDEXT		

Figure 50 lists the top view of the 256-Ball CSP_BGA (12 mm × 12 mm) ball configuration. Figure 51 lists the bottom view.

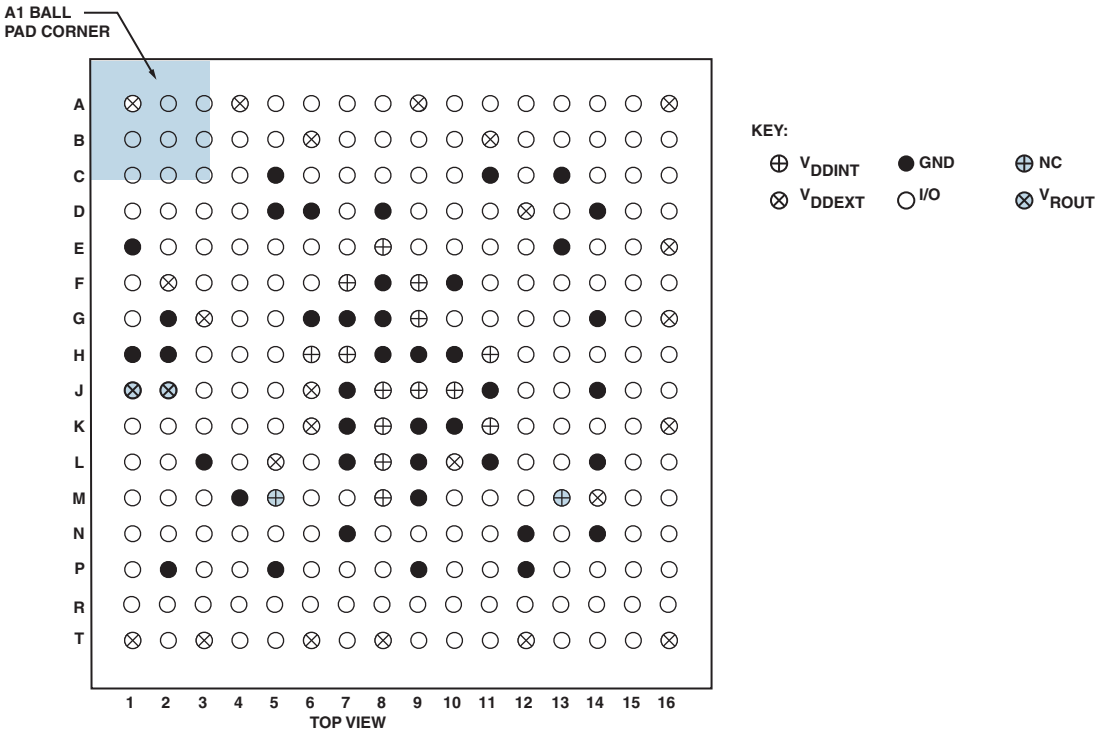

Figure 50. 256-Ball CSP_BGA Ball Configuration (Top View)

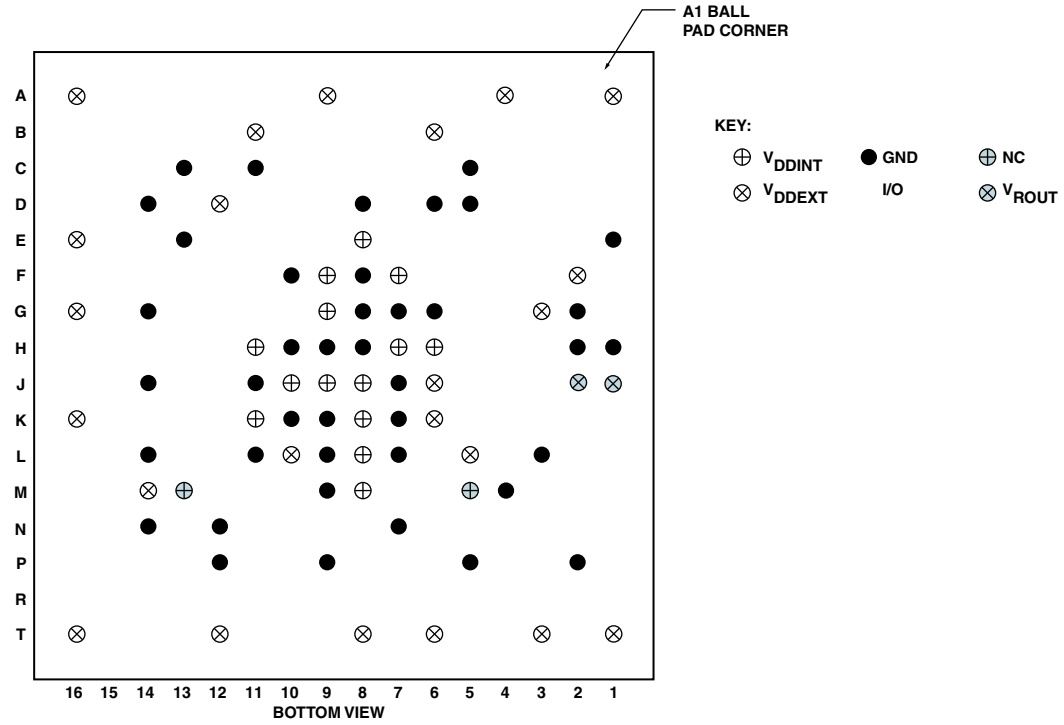

Figure 51. 256-Ball CSP_BGA Ball Configuration (Bottom View)

297-BALL PBGA BALL ASSIGNMENT

Table 39 lists the 297-Ball PBGA ball assignment numerically by ball number. Table 40 on Page 58 lists the ball assignment alphabetically by signal.

Table 39. 297-Ball PBGA Ball Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A01	GND	B15	$\overline{\text{SMS1}}$	G01	PPI0D11	L14	GND
A02	ADDR25	B16	$\overline{\text{SMS3}}$	G02	PPI0D10	L15	GND
A03	ADDR23	B17	SCKE	G25	DATA4	L16	GND
A04	ADDR21	B18	$\overline{\text{SWE}}$	G26	DATA7	L17	GND
A05	ADDR19	B19	SA10	H01	BYPASS	L18	VDDINT
A06	ADDR17	B20	$\overline{\text{BR}}$	H02	$\overline{\text{RESET}}$	L25	DATA12
A07	ADDR15	B21	$\overline{\text{BG}}$	H25	DATA6	L26	DATA15
A08	ADDR13	B22	$\overline{\text{ABE1}}$	H26	DATA9	M01	VROUT0
A09	ADDR11	B23	$\overline{\text{ABE3}}$	J01	CLKIN	M02	GND
A10	ADDR09	B24	ADDR07	J02	GND	M10	VDDEXT
A11	$\overline{\text{AMS3}}$	B25	GND	J10	VDDEXT	M11	GND
A12	$\overline{\text{AMS1}}$	B26	ADDR05	J11	VDDEXT	M12	GND
A13	$\overline{\text{AWE}}$	C01	PPI0SYNC3	J12	VDDEXT	M13	GND
A14	$\overline{\text{ARE}}$	C02	PPI0CLK	J13	VDDEXT	M14	GND
A15	$\overline{\text{SMS0}}$	C03	GND	J14	VDDEXT	M15	GND
A16	$\overline{\text{SMS2}}$	C04	GND	J15	VDDEXT	M16	GND
A17	$\overline{\text{SRAS}}$	C05	GND	J16	VDDINT	M17	GND
A18	$\overline{\text{SCAS}}$	C22	GND	J17	VDDINT	M18	VDDINT
A19	SCLK0	C23	GND	J18	VDDINT	M25	DATA14
A20	SCLK1	C24	GND	J25	DATA8	M26	DATA17
A21	$\overline{\text{BGH}}$	C25	ADDR04	J26	DATA11	N01	VROUT1
A22	$\overline{\text{ABE0}}$	C26	ADDR03	K01	XTAL	N02	PPI0D9
A23	$\overline{\text{ABE2}}$	D01	PPI0SYNC1	K02	NC	N10	VDDEXT
A24	ADDR08	D02	PPI0SYNC2	K10	VDDEXT	N11	GND
A25	ADDR06	D03	GND	K11	VDDEXT	N12	GND
A26	GND	D04	GND	K12	VDDEXT	N13	GND
B01	PPI1CLK	D23	GND	K13	VDDEXT	N14	GND
B02	GND	D24	GND	K14	VDDEXT	N15	GND
B03	ADDR24	D25	ADDR02	K15	VDDEXT	N16	GND
B04	ADDR22	D26	DATA1	K16	VDDINT	N17	GND
B05	ADDR20	E01	PPI0D15	K17	VDDINT	N18	VDDINT
B06	ADDR18	E02	PPI0D14	K18	VDDINT	N25	DATA16
B07	ADDR16	E03	GND	K25	DATA10	N26	DATA19
B08	ADDR14	E24	GND	K26	DATA13	P01	PPI0D7
B09	ADDR12	E25	DATA0	L01	NC	P02	PPI0D8
B10	ADDR10	E26	DATA3	L02	NC	P10	VDDEXT
B11	$\overline{\text{AMS2}}$	F01	PPI0D13	L10	VDDEXT	P11	GND
B12	$\overline{\text{AMS0}}$	F02	PPI0D12	L11	GND	P12	GND
B13	$\overline{\text{AOE}}$	F25	DATA2	L12	GND	P13	GND
B14	ARDY	F26	DATA5	L13	GND	P14	GND

Table 40. 297-Ball PBGA Ball Assignment (Alphabetically by Signal) (Continued)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
GND	AF26	PPI0D7	P01	RSCLK0	AD26	VDDEXT	K13
MISO	AE19	PPI0D8	P02	RSCLK1	AF21	VDDEXT	K14
MOSI	AE20	PPI0D9	N02	RX	AE21	VDDEXT	K15
NC	K02	PPI0D10	G02	SA10	B19	VDDEXT	L10
NC	L01	PPI0D11	G01	$\overline{\text{SCAS}}$	A18	VDDEXT	M10
NC	L02	PPI0D12	F02	SCK	AF19	VDDEXT	N10
NC	AD25	PPI0D13	F01	SCKE	B17	VDDEXT	P10
NC	AE13	PPI0D14	E02	SCLK0	A19	VDDEXT	R10
NC	AE26	PPI0D15	E01	SCLK1	A20	VDDEXT	T10
NMI0	AF18	PPI0SYNC1	D01	SLEEP	AF17	VDDEXT	U10
NMI1	AF13	PPI0SYNC2	D02	$\overline{\text{SMS0}}$	A15	VDDEXT	U11
PF0	AE05	PPI0SYNC3	C01	$\overline{\text{SMS1}}$	B15	VDDEXT	U12
PF1	AF05	PPI1CLK	B01	$\overline{\text{SMS2}}$	A16	VDDEXT	U13
PF2	AE06	PPI1D0	AF04	$\overline{\text{SMS3}}$	B16	VDDINT	J16
PF3	AF06	PPI1D1	AE04	$\overline{\text{SRAS}}$	A17	VDDINT	J17
PF4	AE07	PPI1D2	AF03	$\overline{\text{SWE}}$	B18	VDDINT	J18
PF5	AF07	PPI1D3	AE03	TCK	AF14	VDDINT	K16
PF6	AE08	PPI1D4	AF02	TDI	AF15	VDDINT	K17
PF7	AF08	PPI1D5	AE01	TDO	AE14	VDDINT	K18
PF8	AE09	PPI1D6	AD02	TFS0	AB25	VDDINT	L18
PF9	AF09	PPI1D7	AD01	TFS1	AE24	VDDINT	M18
PF10	AE10	PPI1D8	AC02	TMS	AF16	VDDINT	N18
PF11	AF10	PPI1D9	AC01	$\overline{\text{TRST}}$	AE15	VDDINT	P18
PF12	AE11	PPI1D10	AB02	TSCLK0	AA26	VDDINT	R18
PF13	AF11	PPI1D11	AB01	TSCLK1	AF23	VDDINT	T18
PF14	AE12	PPI1D12	AA02	TX/PF26	AF20	VDDINT	U15
PF15	AF12	PPI1D13	AA01	VDDEXT	J10	VDDINT	U16
PPI0CLK	C02	PPI1D14	Y02	VDDEXT	J11	VDDINT	U17
PPI0D0	V02	PPI1D15	Y01	VDDEXT	J12	VDDINT	U18
PPI0D1	U01	PPI1SYNC1	W01	VDDEXT	J13	VROUT0	M01
PPI0D2	U02	PPI1SYNC2	W02	VDDEXT	J14	VROUT1	N01
PPI0D3	T01	PPI1SYNC3	V01	VDDEXT	J15	XTAL	K01
PPI0D4	T02	$\overline{\text{RESET}}$	H02	VDDEXT	K10		
PPI0D5	R01	RFS0	AC26	VDDEXT	K11		
PPI0D6	R02	RFS1	AE22	VDDEXT	K12		

OUTLINE DIMENSIONS

Dimensions in the outline dimension figures are shown in millimeters.

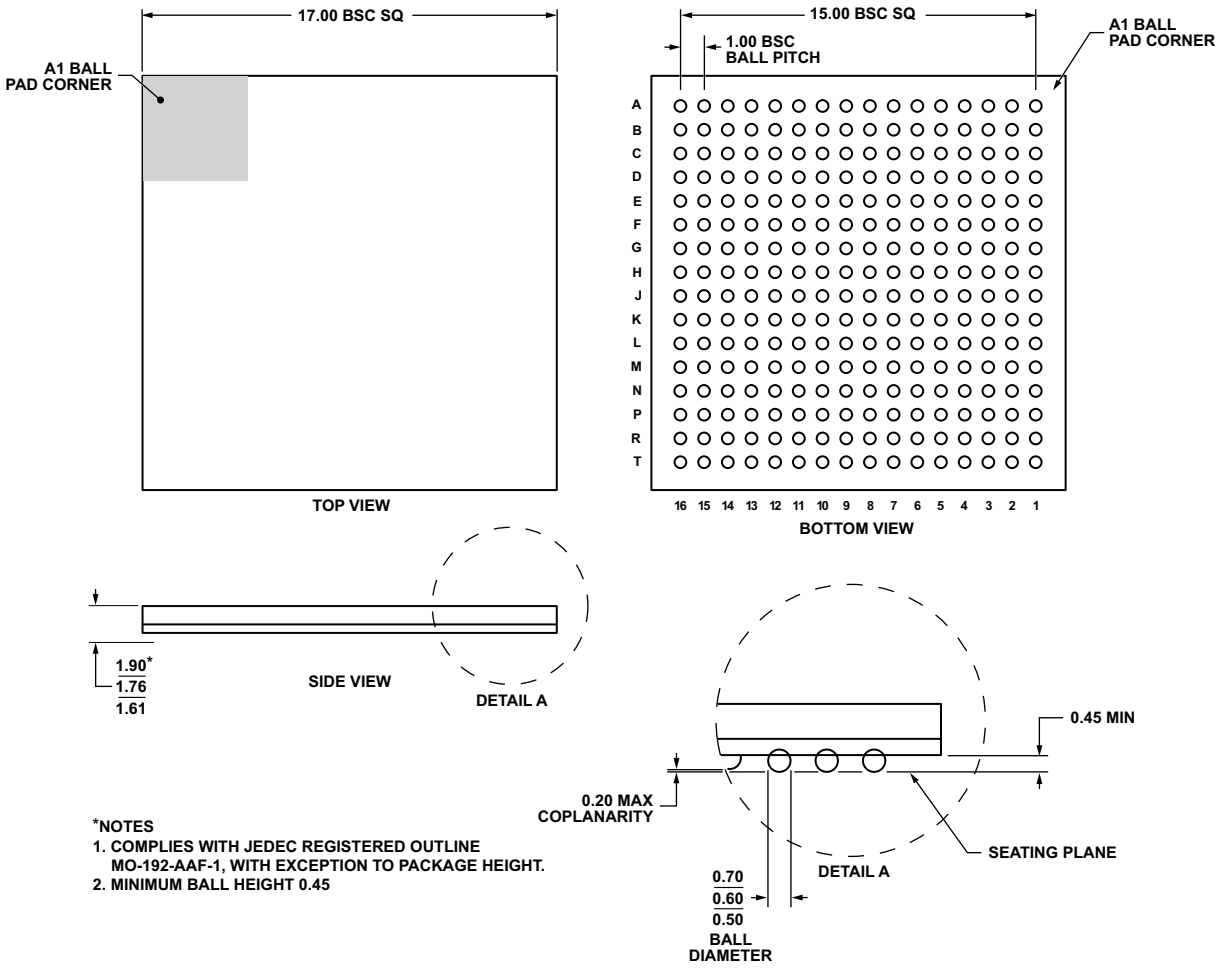

Figure 54. 256-Ball Chip Scale Package Ball Grid Array (CSP_BGA) (BC-256-4)