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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	500MHz
Non-Volatile Memory	External
On-Chip RAM	328kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	297-BGA
Supplier Device Package	297-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf561sbb500

- ADSP-BF561: Blackfin Embedded Symmetric Multiprocessor Data Sheet

Emulator Manuals

- HPUSB, USB, and HPPCI Emulator User's Guide
- ICE-1000/ICE-2000 Emulator User's Guide
- ICE-100B Emulator User's Guide

Evaluation Kit Manuals

- ADSP-BF561 EZ-KIT Lite® Evaluation System Manual
- Blackfin® A-V EZ-Extender® Manual
- Blackfin® EZ-Extender® Manual
- Blackfin® FPGA EZ-Extender® Manual
- Blackfin®/SHARC® USB EZ-Extender® Manual

Integrated Circuit Anomalies

- ADSP-BF561 Blackfin Anomaly List for Revisions 0.3, 0.5

Processor Manuals

- ADSP-BF561 Blackfin ® Processor Hardware Reference
- ADSP-BF5xx/ADSP-BF60x Blackfin® Processor Programming Reference
- Blackfin Processors: Manuals

Product Highlight

- ADSP-BF561 Blackfin Dual-Core Embedded Processor
- Blackfin Processor Family Product Highlight
- EZ-KIT Lite for Analog Devices ADSP-BF561 Blackfin Processor

Software Manuals

- CrossCore® Embedded Studio 2.5.0 Assembler and Preprocessor Manual
- CrossCore® Embedded Studio 2.5.0 C/C++ Compiler and Library Manual for Blackfin Processors
- CrossCore® Embedded Studio 2.5.0 Linker and Utilities Manual
- CrossCore® Embedded Studio 2.5.0 Loader and Utilities Manual
- CrossCore® Software Licensing Guide
- lwIP for CrossCore® Embedded Studio 1.0.0 User's Guide
- VisualDSP++® 5.0 Assembler and Preprocessor Manual
- VisualDSP++® 5.0 C/C++ Compiler and Library Manual for Blackfin Processors
- VisualDSP++® 5.0 Device Drivers and System Services Manual for Blackfin Processors
- VisualDSP++® 5.0 Kernel (VDK) Users Guide
- VisualDSP++® 5.0 Licensing Guide
- VisualDSP++® 5.0 Linker and Utilities Manual
- VisualDSP++® 5.0 Loader and Utilities Manual
- VisualDSP++® 5.0 Product Release Bulletin
- VisualDSP++® 5.0 Quick Installation Reference Card
- VisualDSP++® 5.0 Users Guide

SOFTWARE AND SYSTEMS REQUIREMENTS

- Software and Tools Anomalies Search

TOOLS AND SIMULATIONS

- ADSP-BF561 Blackfin Processor BSDL File 256-Ball CSP BGA Package
- ADSP-BF561 Blackfin Processor BSDL File 256-Ball Sparse CSP_BGA Package
- ADSP-BF561 Blackfin Processor BSDL File 297-Ball PBGA Package
- ADSP-BF561 Blackfin Processor Core B BSDL File All Packages
- Designing with BGA
- Blackfin Processors Software and Tools
- ADSP-BF561 Blackfin Processor IBIS Datafile for 12x12 CSP BGA Package (02/2008)
- ADSP-BF561 Blackfin Processor IBIS Datafile for 17x17 CSP BGA Package (11/2008)
- ADSP-BF561 Blackfin Processor IBIS Datafile for 27x27 PBGA Package (02/2008)

GENERAL DESCRIPTION

The ADSP-BF561 processor is a high performance member of the Blackfin® family of products targeting a variety of multimedia, industrial, and telecommunications applications. At the heart of this device are two independent Analog Devices Blackfin processors. These Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantage of a clean, orthogonal RISC-like microprocessor instruction set, and single instruction, multiple data (SIMD) multimedia capabilities in a single instruction set architecture.

The ADSP-BF561 processor has 328K bytes of on-chip memory. Each Blackfin core includes:

- 16K bytes of instruction SRAM/cache
- 16K bytes of instruction SRAM
- 32K bytes of data SRAM/cache
- 32K bytes of data SRAM
- 4K bytes of scratchpad SRAM

Additional on-chip memory peripherals include:

- 128K bytes of low latency on-chip L2 SRAM
- Four-channel internal memory DMA controller
- External memory controller with glueless support for SDRAM, mobile SDRAM, SRAM, and flash.

PORTABLE LOW POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. Blackfin processors are designed in a low power and low voltage design methodology and feature dynamic power management, the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. Varying the voltage and frequency can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This translates into longer battery life for portable appliances.

BLACKFIN PROCESSOR CORE

As shown in Figure 2, each Blackfin core contains two multiplier/accumulators (MACs), two 40-bit ALUs, four video ALUs, and a single shifter. The computational units process 8-bit, 16-bit, or 32-bit data from the register file.

Each MAC performs a 16-bit by 16-bit multiply in every cycle, with accumulation to a 40-bit result, providing eight bits of extended precision. The ALUs perform a standard set of arithmetic and logical operations. With two ALUs capable of operating on 16-bit or 32-bit data, the flexibility of the computation units covers the signal processing requirements of a varied set of application needs.

Each of the two 32-bit input registers can be regarded as two 16-bit halves, so each ALU can accomplish very flexible single 16-bit arithmetic operations. By viewing the registers as pairs of 16-bit operands, dual 16-bit or single 32-bit operations can be accomplished in a single cycle. By further taking advantage of the second ALU, quad 16-bit operations can be accomplished simply, accelerating the per cycle throughput.

The powerful 40-bit shifter has extensive capabilities for performing shifting, rotating, normalization, extraction, and depositing of data. The data for the computational units is found in a multiported register file of sixteen 16-bit entries or eight 32-bit entries.

A powerful program sequencer controls the flow of instruction execution, including instruction alignment and decoding. The sequencer supports conditional jumps and subroutine calls, as well as zero overhead looping. A loop buffer stores instructions locally, eliminating instruction memory accesses for tight looped code.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches from memory. The DAGs share a register file containing four sets of 32-bit Index, Modify, Length, and Base registers. Eight additional 32-bit registers provide pointers for general indexing of variables and stack locations.

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. Level 2 (L2) memories are other memories, on-chip or off-chip, that may take multiple processor cycles to access. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information. At the L2 level, there is a single unified memory space, holding both instructions and data.

In addition, half of L1 instruction memory and half of L1 data memory may be configured as either Static RAMs (SRAMs) or caches. The Memory Management Unit (MMU) provides memory protection for individual tasks that may be operating on the core and may protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin instruction set has been optimized so that 16-bit op-codes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit op-codes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the VisualDSP C/C++ compiler, resulting in fast and efficient software implementations.

writing the appropriate values into the Interrupt Assignment Registers (SIC_IAR7–0). Table 2 describes the inputs into the SIC and the default mappings into the CEC.

Table 2. System Interrupt Controller (SIC)

Peripheral Interrupt Event	Default Mapping
PLL Wakeup	IVG7
DMA1 Error (Generic)	IVG7
DMA2 Error (Generic)	IVG7
IMDMA Error	IVG7
PPI0 Error	IVG7
PPI1 Error	IVG7
SPORT0 Error	IVG7
SPORT1 Error	IVG7
SPI Error	IVG7
UART Error	IVG7
Reserved	IVG7
DMA1 Channel 0 Interrupt (PPI0)	IVG8
DMA1 Channel 1 Interrupt (PPI1)	IVG8
DMA1 Channel 2 Interrupt	IVG8
DMA1 Channel 3 Interrupt	IVG8
DMA1 Channel 4 Interrupt	IVG8
DMA1 Channel 5 Interrupt	IVG8
DMA1 Channel 6 Interrupt	IVG8
DMA1 Channel 7 Interrupt	IVG8
DMA1 Channel 8 Interrupt	IVG8
DMA1 Channel 9 Interrupt	IVG8
DMA1 Channel 10 Interrupt	IVG8
DMA1 Channel 11 Interrupt	IVG8
DMA2 Channel 0 Interrupt (SPORT0 Rx)	IVG9
DMA2 Channel 1 Interrupt (SPORT0 Tx)	IVG9
DMA2 Channel 2 Interrupt (SPORT1 Rx)	IVG9
DMA2 Channel 3 Interrupt (SPORT1 Tx)	IVG9
DMA2 Channel 4 Interrupt (SPI)	IVG9
DMA2 Channel 5 Interrupt (UART Rx)	IVG9
DMA2 Channel 6 Interrupt (UART Tx)	IVG9
DMA2 Channel 7 Interrupt	IVG9
DMA2 Channel 8 Interrupt	IVG9
DMA2 Channel 9 Interrupt	IVG9
DMA2 Channel 10 Interrupt	IVG9
DMA2 Channel 11 Interrupt	IVG9
Timer0 Interrupt	IVG10
Timer1 Interrupt	IVG10
Timer2 Interrupt	IVG10
Timer3 Interrupt	IVG10
Timer4 Interrupt	IVG10
Timer5 Interrupt	IVG10
Timer6 Interrupt	IVG10
Timer7 Interrupt	IVG10
Timer8 Interrupt	IVG10
Timer9 Interrupt	IVG10
Timer10 Interrupt	IVG10
Timer11 Interrupt	IVG10
Programmable Flags 15–0 Interrupt A	IVG11
Programmable Flags 15–0 Interrupt B	IVG11
Programmable Flags 31–16 Interrupt A	IVG11
Programmable Flags 31–16 Interrupt B	IVG11
Programmable Flags 47–32 Interrupt A	IVG11
Programmable Flags 47–32 Interrupt B	IVG11
DMA1 Channel 12/13 Interrupt (Memory DMA/Stream 0)	IVG8
DMA1 Channel 14/15 Interrupt (Memory DMA/Stream 1)	IVG8
DMA2 Channel 12/13 Interrupt (Memory DMA/Stream 0)	IVG9
DMA2 Channel 14/15 Interrupt (Memory DMA/Stream 1)	IVG9
IMDMA Stream 0 Interrupt	IVG12
IMDMA Stream 1 Interrupt	IVG12
Watchdog Timer Interrupt	IVG13
Reserved	IVG7
Reserved	IVG7
Supplemental Interrupt 0	IVG7
Supplemental Interrupt 1	IVG7

Event Control

The ADSP-BF561 provides the user with a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each of the registers is 16 bits wide, while each bit represents a particular event class.

- CEC Interrupt Latch Register (ILAT) – The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but may also be written to clear (cancel) latched events. This register may be read while in supervisor mode and may only be written while in supervisor mode when the corresponding IMASK bit is cleared.
- CEC Interrupt Mask Register (IMASK) – The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and will be processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, thereby preventing the processor from servicing the event

- All registers, I/O, and memory are mapped into a unified 4G byte memory space providing a simplified programming model.
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data types; and separate user and kernel stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded as 16-bits.

DEVELOPMENT TOOLS

The ADSP-BF561 is supported with a complete set of CROSSCORE®† software and hardware development tools, including Analog Devices emulators and the VisualDSP++®‡ development environment. The same emulator hardware that supports other Analog Devices processors also fully emulates the ADSP-BF561.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler that is based on an algebraic syntax, an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ runtime library that includes DSP and mathematical functions. A key point for these tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to Blackfin assembly. The Blackfin processor has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to nonintrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information).
- Insert breakpoints.
- Set conditional breakpoints on registers, memory, and stacks.
- Trace instruction execution.
- Perform linear or statistical profiling of program execution.
- Fill, dump, and graphically plot the contents of memory.
- Perform source level debugging.
- Create custom debugger windows.

The VisualDSP++ IDE lets programmers define and manage software development. Its dialog boxes and property pages let programmers configure and manage all development tools, including color syntax highlighting in the VisualDSP++ editor. These capabilities permit programmers to:

- Control how the development tools process inputs and generate outputs.
- Maintain a one-to-one correspondence with the tool's command line switches.

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of embedded, real-time programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, pre-emptive, cooperative, and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used with standard command line tools. When the VDK is used, the development environment assists the developer with many error prone tasks and assists in managing system resources, automating the generation of various VDK-based objects, and visualizing the system state when debugging an application that uses the VDK.

The Expert Linker can be used to visually manipulate the placement of code and data in the embedded system. Memory utilization can be viewed in a color-coded graphical form. Code and data can be easily moved to different areas of the processor or external memory with the drag of the mouse. Runtime stack and heap usage can be examined. The Expert Linker is fully compatible with existing Linker Definition File (LDF), allowing the developer to move between the graphical and textual environments.

Analog Devices emulators use the IEEE 1149.1 JTAG test access port of the ADSP-BF561 to monitor and control the target board processor during emulation. The emulator provides full-speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect the loading or timing of the target system.

† CROSSCORE is a registered trademark of Analog Devices, Inc.
‡ VisualDSP++ is a registered trademark of Analog Devices, Inc.

Asynchronous Memory Read Cycle Timing

Table 18. Asynchronous Memory Read Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA31–0 Setup Before CLKOUT	2.1		ns
t_{HDAT}	DATA31–0 Hold After CLKOUT	0.8		ns
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE3-0}$, ADDR25–2, $\overline{AOE}$, $\overline{ARE}$.

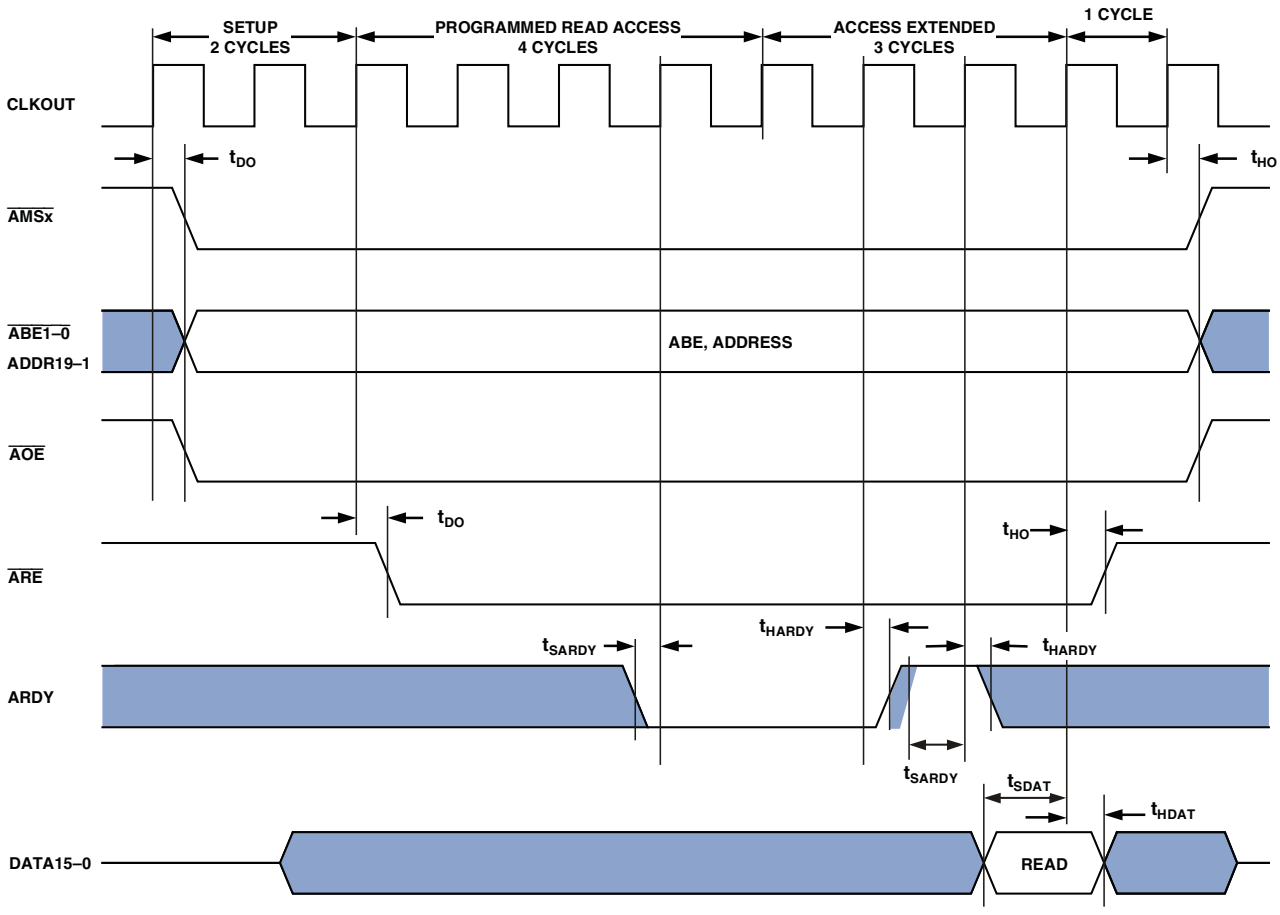


Figure 10. Asynchronous Memory Read Cycle Timing

SDRAM Interface Timing

Table 20. SDRAM Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDAT}	DATA Setup Before CLKOUT	1.5		ns
t_{HSDAT}	DATA Hold After CLKOUT	0.8		ns
Switching Characteristics				
t_{DCAD}	Command, ADDR, Data Delay After CLKOUT[1]		4.0	ns
t_{HCAD}	Command, ADDR, Data Hold After CLKOUT[1]	0.8		ns
t_{DSDAT}	Data Disable After CLKOUT		4.0	ns
t_{ENSDAT}	Data Enable After CLKOUT	1.0		ns
t_{SCLK}	CLKOUT Period	7.5		ns
t_{SCLKH}	CLKOUT Width High	2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		ns

[1] Command pins include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS3–0}$, SA10, SCKE.

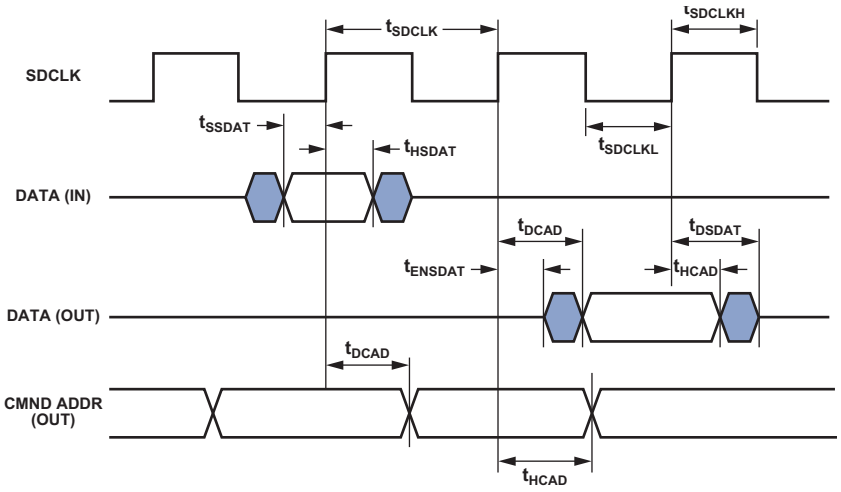


Figure 12. SDRAM Interface Timing

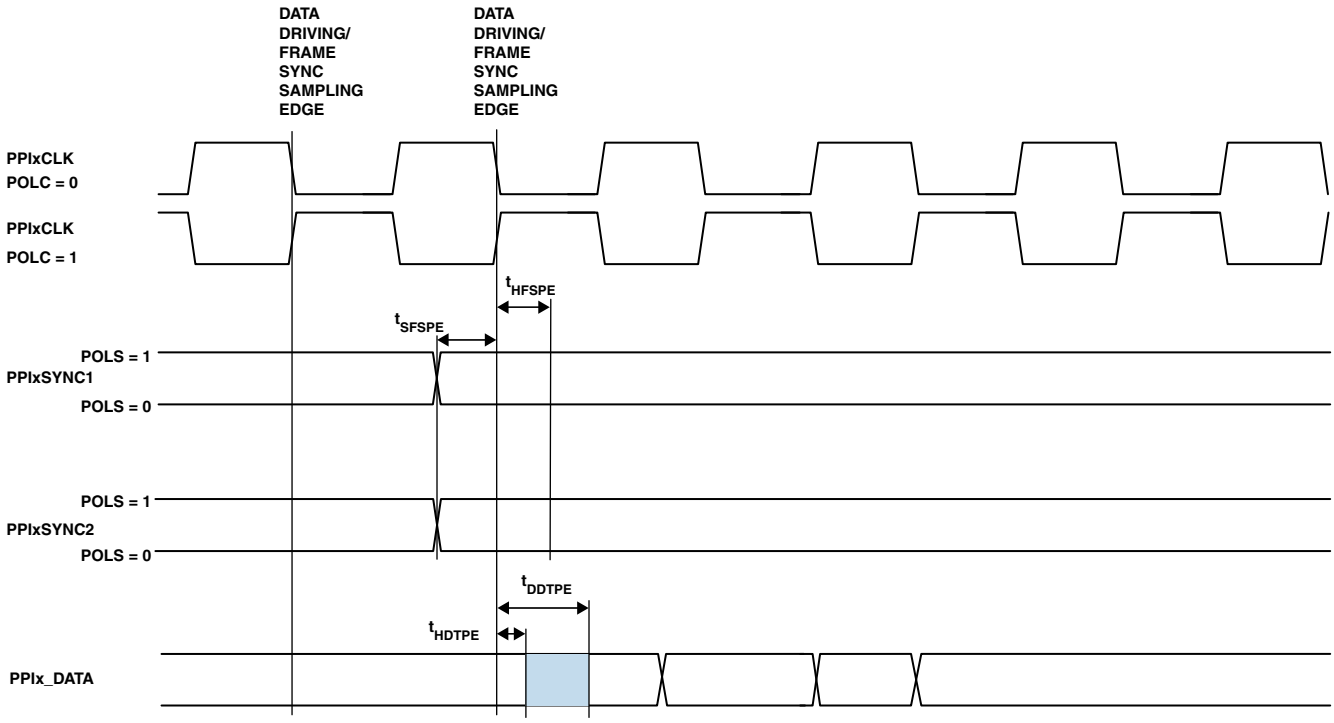


Figure 19. PPI GP Tx Mode with External Frame Sync Timing (Bit 4 of PLL_CTL Set)

Serial Ports

Table 23 through Table 26 on Page 34 and Figure 20 on Page 33 through Figure 22 on Page 34 describe Serial Port operations.

Table 23. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	3.0		ns
t_{HFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	3.0		ns
t_{SDRE}	Receive Data Setup Before RSCLKx[1]	3.0		ns
t_{HDRE}	Receive Data Hold After RSCLKx[1]	3.0		ns
t_{SCLKW}	TSCLKx/RSCLKx Width	4.5		ns
t_{SCLK}	TSCLKx/RSCLKx Period	15.0		ns
t_{SUDTE}	Start-Up Delay From SPORT Enable To First External TFSx	4.0		TSCLKx
t_{SUDRE}	Start-Up Delay From SPORT Enable To First External RFSx	4.0		RSCLKx
Switching Characteristics				
t_{DFSE}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]		10.0	ns
t_{HOFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]	0.0		ns
t_{DDTE}	Transmit Data Delay After TSCLKx[2]		10.0	ns
t_{HDTE}	Transmit Data Hold After TSCLKx[2]	0.0		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 24. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	8.0		ns
t_{HFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	–2.0		ns
t_{SDRI}	Receive Data Setup Before RSCLKx[1]	6.0		ns
t_{HDRI}	Receive Data Hold After RSCLKx[1]	0.0		ns
t_{SCLKW}	TSCLKx/RSCLKx Width	4.5		ns
t_{SCLK}	TSCLKx/RSCLKx Period	15.0		ns
Switching Characteristics				
t_{DFSI}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]		3.0	ns
t_{HOFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]	–1.0		ns
t_{DDTI}	Transmit Data Delay After TSCLKx[2]		3.0	ns
t_{HDTI}	Transmit Data Hold After TSCLKx[2]	–2.0		ns
t_{SCLKIW}	TSCLKx/RSCLKx Width	4.5		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 25. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1]		10.0	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	–2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1]		3.0	ns

[1] Referenced to drive edge.

Table 26. External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFSx or External RFSx with MCMEN = 1, MFD = 0[1, 2]		10.0	ns
$t_{DTENLFS}$	Data Enable from Late FS or MCMEN = 1, MFD = 0[1, 2]	0		ns

[1] MCMEN = 1, TFSx enable and TFSx valid follow $t_{DTENLFS}$ and $t_{DDTLFSE}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$, then $t_{DDTTE/I}$ and $t_{DTENE/I}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

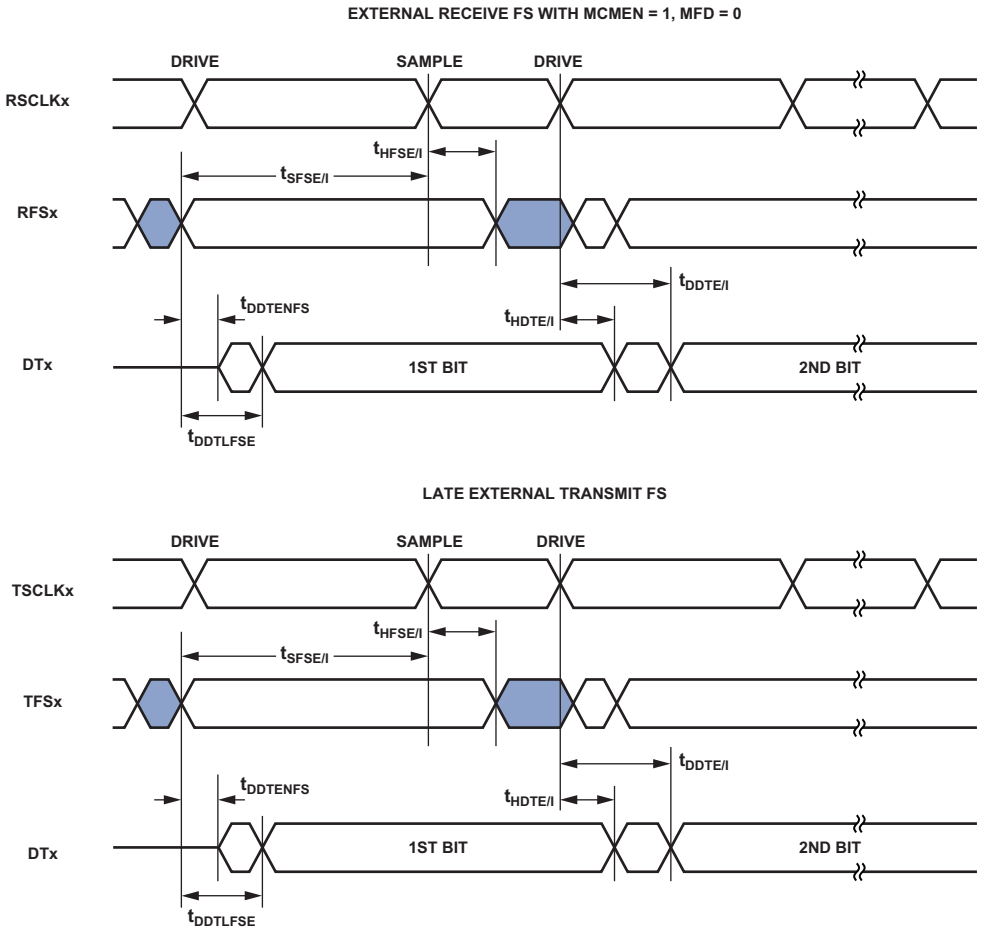


Figure 22. External Late Frame Sync

Universal Asynchronous Receiver Transmitter (UART) Port—Receive and Transmit Timing

Figure 25 describes UART port receive and transmit operations. The maximum baud rate is SCLK/16. As shown in Figure 25, there is some latency between the generation internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART.

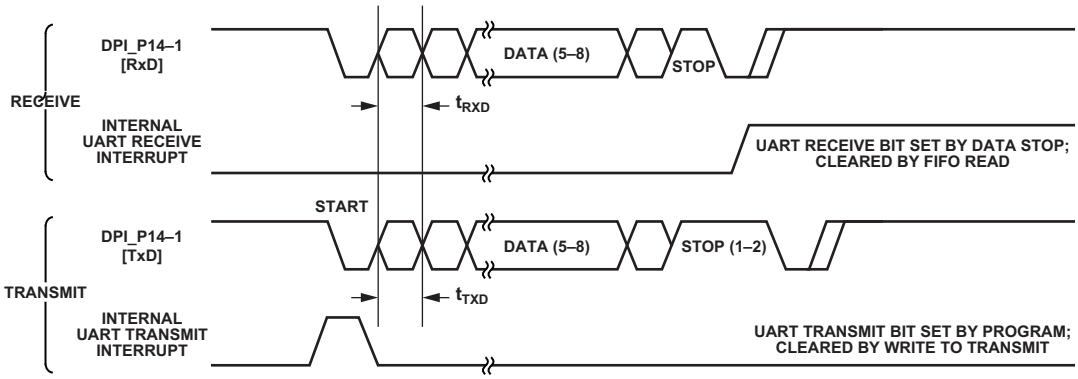


Figure 25. UART Port—Receive and Transmit Timing

JTAG Test and Emulation Port Timing

Table 31 and Figure 28 describe JTAG port operations.

Table 31. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Parameters				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	5		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width[2] (Measured in TCK Cycles)	4		TCK
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	12	ns

[1] System Inputs = DATA31–0, ARDY, PF47–0, PPI0CLK, PPI1CLK, RSCLK0–1, RFS0–1, DR0PRI, DR0SEC, TSCLK0–1, TFS0–1, DR1PRI, DR1SEC, MOSI, MISO, SCK, RX, $\overline{\text{RESET}}$, NMI0, NMI1, BMODE1–0, $\overline{\text{BR}}$, and PPIxD7–0.

[2] 50 MHz maximum

[3] System Outputs = DATA31–0, ADDR25–2, $\overline{\text{ABE3–0}}$, $\overline{\text{AOE}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, $\overline{\text{AMS3–0}}$, $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$, $\overline{\text{SWE}}$, SCKE, CLKOUT, SA10, $\overline{\text{SMS3–0}}$, PF47–0, RSCLK0–1, RFS0–1, TSCLK0–1, TFS0–1, DT0PRI, DT0SEC, DT1PRI, DT1SEC, MOSI, MISO, SCK, TX, $\overline{\text{BG}}$, $\overline{\text{BGH}}$, and PPIxD7–0.

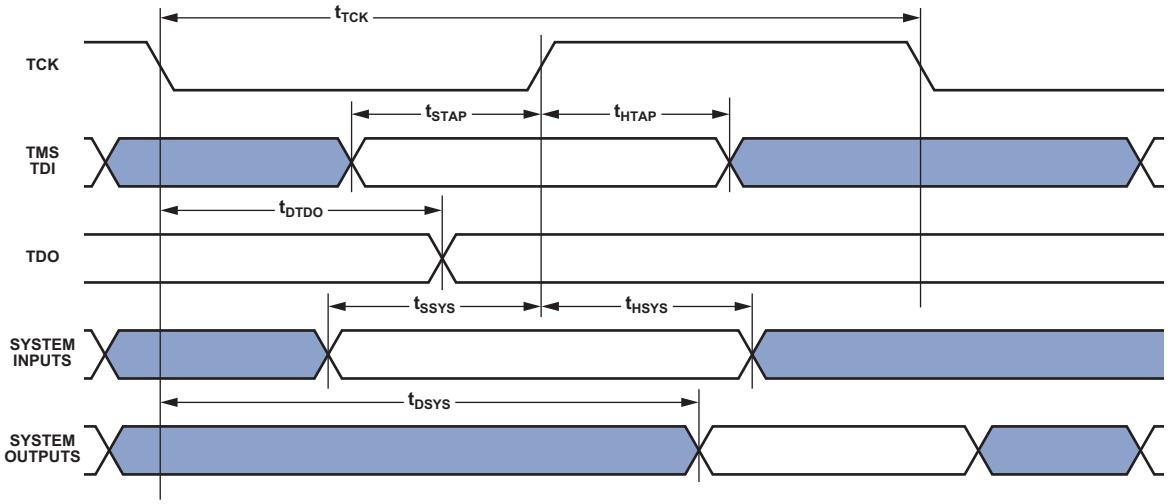


Figure 28. JTAG Port Timing

OUTPUT DRIVE CURRENTS

Figure 29 through Figure 36 on Page 42 show typical current voltage characteristics for the output drivers of the ADSP-BF561 processor. The curves represent the current drive capability of the output drivers as a function of output voltage. Refer to Table 8 on Page 17 to identify the driver type for a pin.

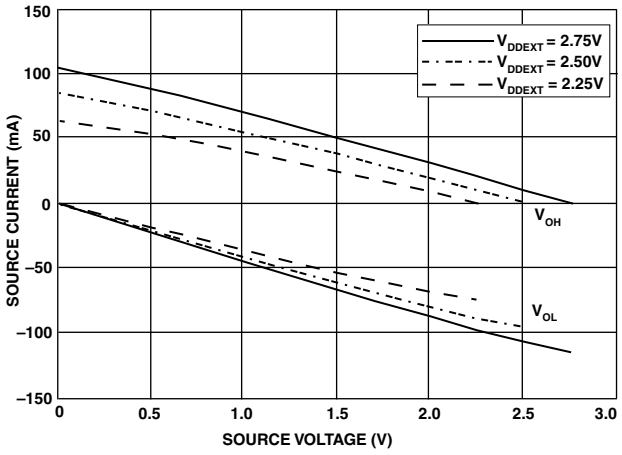


Figure 29. Drive Current A (Low V_{DDEXT})

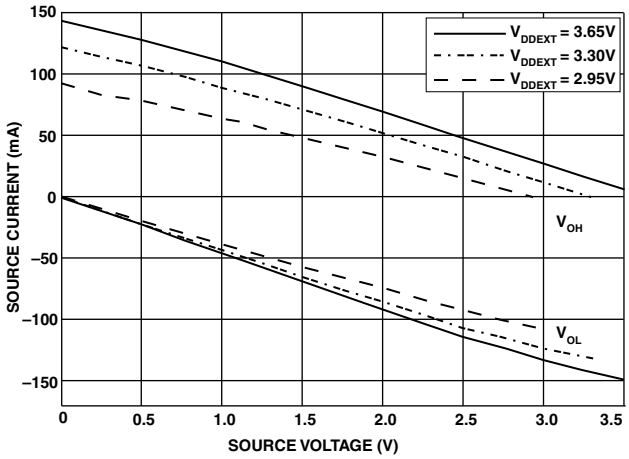


Figure 30. Drive Current A (High V_{DDEXT})

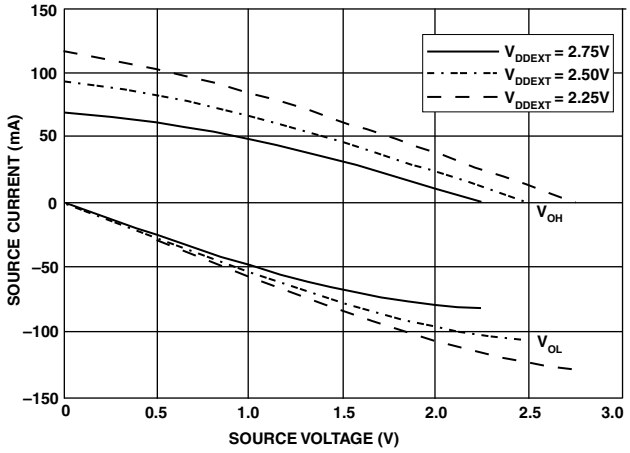


Figure 31. Drive Current B (Low V_{DDEXT})

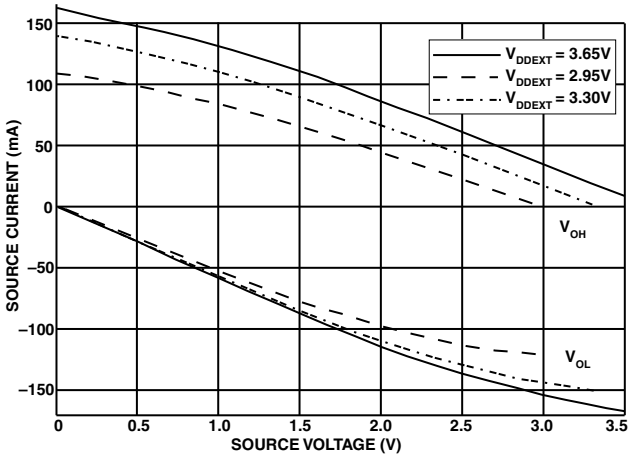


Figure 32. Drive Current B (High V_{DDEXT})

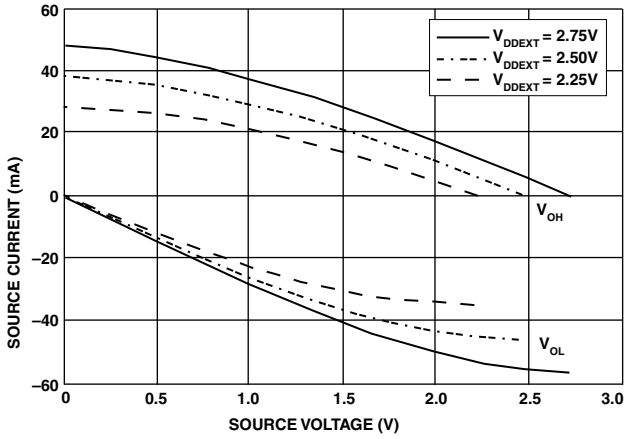


Figure 33. Drive Current C (Low V_{DDEXT})

In Table 32 through Table 34, airflow measurements comply with JEDEC standards JESD51–2 and JESD51–6, and the junction-to-board measurement complies with JESD51–8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Thermal resistance θ_{JA} in Table 32 through Table 34 is the figure of merit relating to performance of the package and board in a convective environment. θ_{JMA} represents the thermal resistance under two conditions of airflow. θ_{JB} represents the heat extracted from the periphery of the board. Ψ_{JT} represents the correlation between T_J and T_{CASE}. Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

Table 32. Thermal Characteristics for BC-256-4 (17 mm × 17 mm) Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	18.1	°C/W
θ_{JMA}	1 Linear m/s Airflow	15.9	°C/W
θ_{JMA}	2 Linear m/s Airflow	15.1	°C/W
θ_{JC}	Not Applicable	3.72	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.11	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.18	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.18	°C/W

Table 33. Thermal Characteristics for BC-256-1 (12 mm × 12 mm) Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	25.6	°C/W
θ_{JMA}	1 Linear m/s Airflow	22.4	°C/W
θ_{JMA}	2 Linear m/s Airflow	21.6	°C/W
θ_{JB}	Not Applicable	18.9	°C/W
θ_{JC}	Not Applicable	4.85	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.15	°C/W
Ψ_{JT}	1 Linear m/s Airflow	n/a	°C/W
Ψ_{JT}	2 Linear m/s Airflow	n/a	°C/W

Table 34. Thermal Characteristics for B-297 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	20.6	°C/W
θ_{JMA}	1 Linear m/s Airflow	17.8	°C/W
θ_{JMA}	2 Linear m/s Airflow	17.4	°C/W
θ_{JB}	Not Applicable	16.3	°C/W
θ_{JC}	Not Applicable	7.15	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.37	°C/W
Ψ_{JT}	1 Linear m/s Airflow	n/a	°C/W
Ψ_{JT}	2 Linear m/s Airflow	n/a	°C/W

256-BALL CSP_BGA (17 mm) BALL ASSIGNMENT

Table 35 lists the 256-Ball CSP_BGA (17 mm × 17 mm) ball assignment by ball number. Table 36 on Page 48 lists the ball assignment alphabetically by signal.

Table 35. 256-Ball CSP_BGA (17 mm × 17 mm) Ball Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	VDDEXT	C9	$\overline{\text{SMS3}}$	F1	CLKIN	H9	GND	L1	PPI0D3
A2	ADDR22	C10	$\overline{\text{SWE}}$	F2	PPI0D10	H10	GND	L2	PPI0D2
A3	ADDR18	C11	SA10	F3	$\overline{\text{RESET}}$	H11	GND	L3	PPI0D1
A4	ADDR14	C12	$\overline{\text{ABE0}}$	F4	BYPASS	H12	GND	L4	PPI0D0
A5	ADDR11	C13	ADDR07	F5	VDDEXT	H13	GND	L5	VDDEXT
A6	$\overline{\text{AMS3}}$	C14	ADDR04	F6	VDDEXT	H14	DATA21	L6	VDDEXT
A7	$\overline{\text{AMS0}}$	C15	DATA0	F7	VDDEXT	H15	DATA19	L7	VDDEXT
A8	ARDY	C16	DATA05	F8	GND	H16	DATA23	L8	VDDEXT
A9	$\overline{\text{SMS2}}$	D1	PPI0D15	F9	GND	J1	VROUT1	L9	GND
A10	SCLK0	D2	PPI0SYNC3	F10	VDDEXT	J2	PPI0D8	L10	VDDEXT
A11	SCLK1	D3	PPI0SYNC2	F11	VDDEXT	J3	PPI0D7	L11	VDDEXT
A12	$\overline{\text{ABE2}}$	D4	ADDR21	F12	VDDEXT	J4	PPI0D9	L12	VDDEXT
A13	$\overline{\text{ABE3}}$	D5	ADDR15	F13	DATA11	J5	GND	L13	NC
A14	ADDR06	D6	ADDR09	F14	DATA08	J6	GND	L14	DT0PRI
A15	ADDR03	D7	$\overline{\text{AWE}}$	F15	DATA10	J7	GND	L15	DATA31
A16	VDDEXT	D8	$\overline{\text{SMS0}}$	F16	DATA16	J8	GND	L16	DATA28
B1	ADDR24	D9	$\overline{\text{SRAS}}$	G1	XTAL	J9	GND	M1	PPI1SYNC2
B2	ADDR23	D10	$\overline{\text{SCAS}}$	G2	VDDEXT	J10	GND	M2	PPI1D15
B3	ADDR19	D11	$\overline{\text{BGH}}$	G3	VDDEXT	J11	GND	M3	PPI1D14
B4	ADDR17	D12	$\overline{\text{ABE1}}$	G4	GND	J12	VDDINT	M4	PPI1D9
B5	ADDR12	D13	DATA02	G5	GND	J13	VDDINT	M5	VDDINT
B6	ADDR10	D14	DATA01	G6	VDDEXT	J14	DATA20	M6	VDDINT
B7	$\overline{\text{AMS1}}$	D15	DATA03	G7	GND	J15	DATA22	M7	GND
B8	$\overline{\text{AOE}}$	D16	DATA07	G8	GND	J16	DATA24	M8	VDDINT
B9	$\overline{\text{SMS1}}$	E1	PPI0D11	G9	GND	K1	PPI0D6	M9	GND
B10	SCKE	E2	PPI0D13	G10	GND	K2	PPI0D5	M10	VDDINT
B11	$\overline{\text{BR}}$	E3	PPI0D12	G11	VDDEXT	K3	PPI0D4	M11	GND
B12	$\overline{\text{BG}}$	E4	PPI0D14	G12	VDDEXT	K4	PPI1SYNC3	M12	VDDINT
B13	ADDR08	E5	PPI1CLK	G13	DATA17	K5	VDDEXT	M13	RSCLK0
B14	ADDR05	E6	VDDINT	G14	DATA14	K6	VDDEXT	M14	DR0PRI
B15	ADDR02	E7	GND	G15	DATA15	K7	GND	M15	TSCLK0
B16	DATA04	E8	VDDINT	G16	DATA18	K8	GND	M16	DATA29
C1	PPI0SYNC1	E9	GND	H1	VROUT0	K9	GND	N1	PPI1SYNC1
C2	ADDR25	E10	VDDINT	H2	GND	K10	GND	N2	PPI1D10
C3	PPI0CLK	E11	GND	H3	GND	K11	VDDEXT	N3	PPI1D7
C4	ADDR20	E12	VDDINT	H4	VDDINT	K12	GND	N4	PPI1D5
C5	ADDR16	E13	DATA06	H5	VDDINT	K13	GND	N5	PF0
C6	ADDR13	E14	DATA13	H6	GND	K14	DATA26	N6	PF04
C7	$\overline{\text{AMS2}}$	E15	DATA09	H7	GND	K15	DATA25	N7	PF09
C8	$\overline{\text{ARE}}$	E16	DATA12	H8	GND	K16	DATA27	N8	PF12

256-BALL CSP_BGA (12 mm) BALL ASSIGNMENT

Table 37 lists the 256-Ball CSP_BGA (12 mm × 12 mm) ball assignment by ball number. Table 38 on Page 53 lists the ball assignment alphabetically by signal.

Table 37. 256-Ball CSP_BGA (12 mm × 12 mm) Ball Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A01	VDDEXT	C09	$\overline{\text{SMS2}}$	F01	CLKIN	H09	GND	L01	PPI0D0
A02	ADDR24	C10	$\overline{\text{SRAS}}$	F02	VDDEXT	H10	GND	L02	PPI1SYNC2
A03	ADDR20	C11	GND	F03	$\overline{\text{RESET}}$	H11	VDDINT	L03	GND
A04	VDDEXT	C12	$\overline{\text{BGH}}$	F04	PPI0D10	H12	DATA16	L04	PPI1SYNC3
A05	ADDR14	C13	GND	F05	ADDR21	H13	DATA18	L05	VDDEXT
A06	ADDR10	C14	ADDR07	F06	ADDR17	H14	DATA20	L06	PPI1D11
A07	$\overline{\text{AMS3}}$	C15	DATA1	F07	VDDINT	H15	DATA17	L07	GND
A08	$\overline{\text{AWE}}$	C16	DATA3	F08	GND	H16	DATA19	L08	VDDINT
A09	VDDEXT	D01	PPI0D13	F09	VDDINT	J01	VROUT0	L09	GND
A10	$\overline{\text{SMS3}}$	D02	PPI0D15	F10	GND	J02	VROUT1	L10	VDDEXT
A11	SCLK0	D03	PPI0SYNC3	F11	ADDR08	J03	PPI0D2	L11	GND
A12	SCLK1	D04	ADDR23	F12	DATA10	J04	PPI0D3	L12	DR0PRI
A13	$\overline{\text{BG}}$	D05	GND	F13	DATA8	J05	PPI0D1	L13	TFS0
A14	$\overline{\text{ABE2}}$	D06	GND	F14	DATA12	J06	VDDEXT	L14	GND
A15	$\overline{\text{ABE3}}$	D07	ADDR09	F15	DATA9	J07	GND	L15	DATA27
A16	VDDEXT	D08	GND	F16	DATA11	J08	VDDINT	L16	DATA29
B01	PPI1CLK	D09	ARDY	G01	XTAL	J09	VDDINT	M01	PPI1D15
B02	ADDR22	D10	$\overline{\text{SCAS}}$	G02	GND	J10	VDDINT	M02	PPI1D13
B03	ADDR18	D11	SA10	G03	VDDEXT	J11	GND	M03	PPI1D9
B04	ADDR16	D12	VDDEXT	G04	BYPASS	J12	DATA30	M04	GND
B05	ADDR12	D13	ADDR02	G05	PPI0D14	J13	DATA22	M05	NC
B06	VDDEXT	D14	GND	G06	GND	J14	GND	M06	PF3
B07	$\overline{\text{AMS1}}$	D15	DATA5	G07	GND	J15	DATA21	M07	PF7
B08	$\overline{\text{ARE}}$	D16	DATA6	G08	GND	J16	DATA23	M08	VDDINT
B09	$\overline{\text{SMS1}}$	E01	GND	G09	VDDINT	K01	PPI0D6	M09	GND
B10	SCKE	E02	PPI0D11	G10	ADDR05	K02	PPI0D4	M10	BMODE0
B11	VDDEXT	E03	PPI0D12	G11	ADDR03	K03	PPI0D8	M11	SCK
B12	$\overline{\text{BR}}$	E04	PPI0SYNC1	G12	DATA15	K04	PPI1SYNC1	M12	DR1PRI
B13	$\overline{\text{ABE1}}$	E05	ADDR15	G13	DATA14	K05	PPI1D14	M13	NC
B14	ADDR06	E06	ADDR13	G14	GND	K06	VDDEXT	M14	VDDEXT
B15	ADDR04	E07	$\overline{\text{AMS2}}$	G15	DATA13	K07	GND	M15	DATA31
B16	DATA0	E08	VDDINT	G16	VDDEXT	K08	VDDINT	M16	DT0PRI
C01	PPI0SYNC2	E09	$\overline{\text{SMS0}}$	H01	GND	K09	GND	N01	PPI1D12
C02	PPI0CLK	E10	$\overline{\text{SWE}}$	H02	GND	K10	GND	N02	PPI1D10
C03	ADDR25	E11	$\overline{\text{ABE0}}$	H03	PPI0D9	K11	VDDINT	N03	PPI1D3
C04	ADDR19	E12	DATA2	H04	PPI0D7	K12	DATA28	N04	PPI1D1
C05	GND	E13	GND	H05	PPI0D5	K13	DATA26	N05	PF1
C06	ADDR11	E14	DATA4	H06	VDDINT	K14	DATA24	N06	PF9
C07	$\overline{\text{AOE}}$	E15	DATA7	H07	VDDINT	K15	DATA25	N07	GND
C08	$\overline{\text{AMS0}}$	E16	VDDEXT	H08	GND	K16	VDDEXT	N08	PF13

Figure 50 lists the top view of the 256-Ball CSP_BGA (12 mm × 12 mm) ball configuration. Figure 51 lists the bottom view.

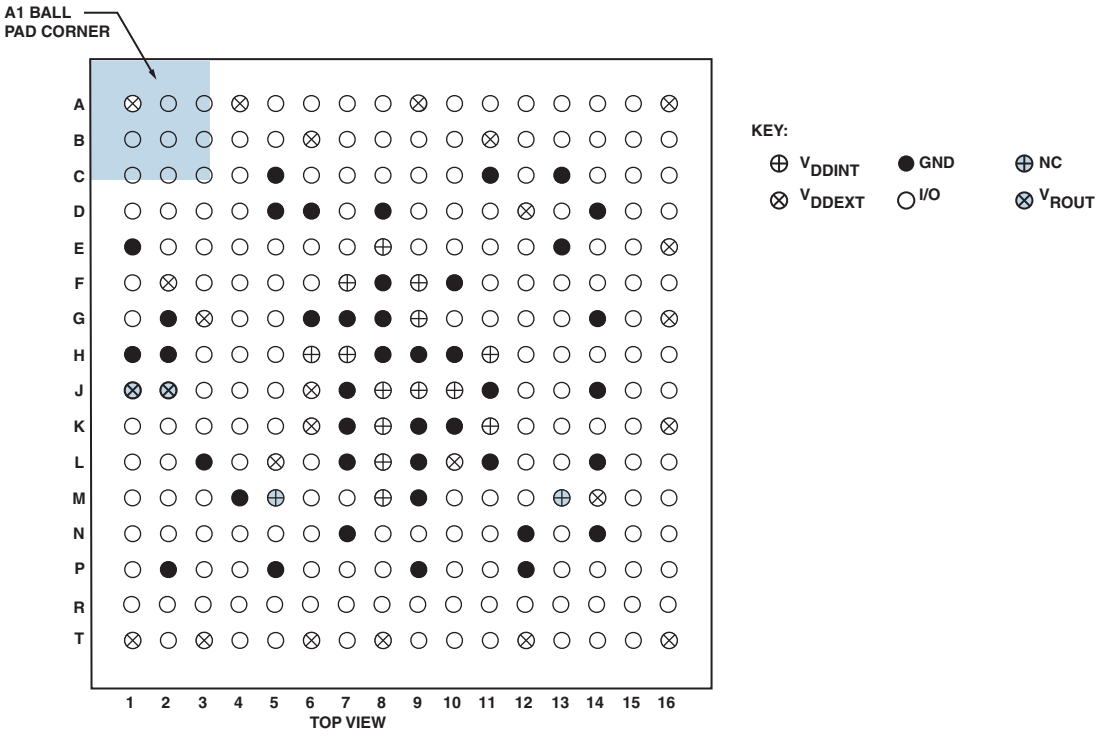


Figure 50. 256-Ball CSP_BGA Ball Configuration (Top View)

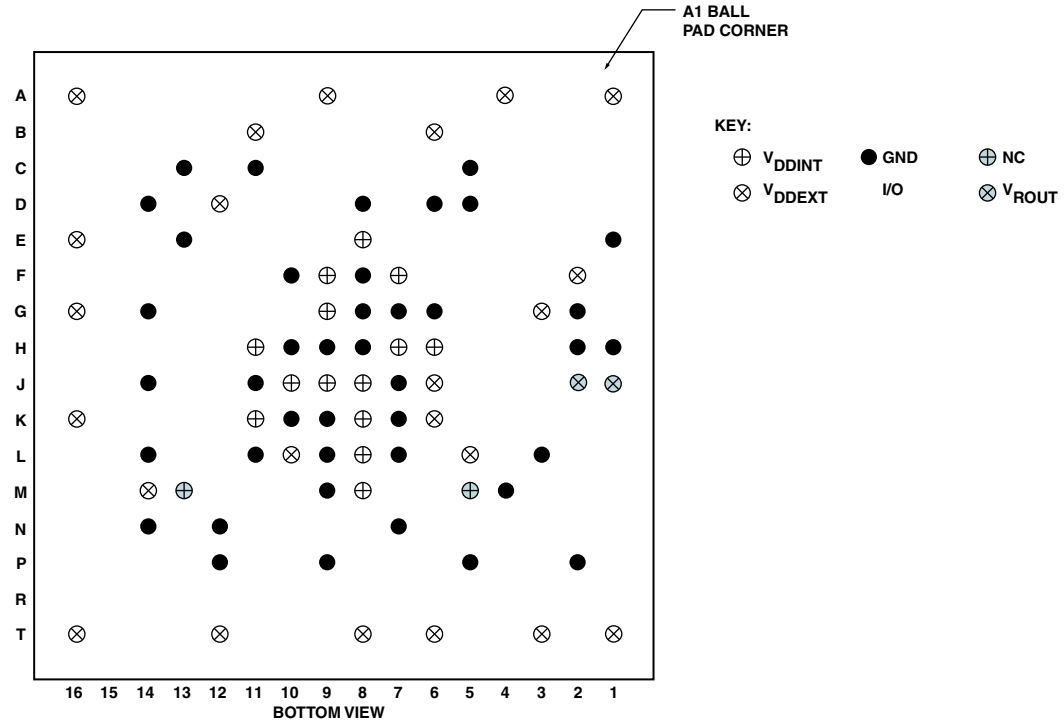


Figure 51. 256-Ball CSP_BGA Ball Configuration (Bottom View)

297-BALL PBGA BALL ASSIGNMENT

Table 39 lists the 297-Ball PBGA ball assignment numerically by ball number. Table 40 on Page 58 lists the ball assignment alphabetically by signal.

Table 39. 297-Ball PBGA Ball Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A01	GND	B15	$\overline{\text{SMS1}}$	G01	PPI0D11	L14	GND
A02	ADDR25	B16	$\overline{\text{SMS3}}$	G02	PPI0D10	L15	GND
A03	ADDR23	B17	SCKE	G25	DATA4	L16	GND
A04	ADDR21	B18	$\overline{\text{SWE}}$	G26	DATA7	L17	GND
A05	ADDR19	B19	SA10	H01	BYPASS	L18	VDDINT
A06	ADDR17	B20	$\overline{\text{BR}}$	H02	$\overline{\text{RESET}}$	L25	DATA12
A07	ADDR15	B21	$\overline{\text{BG}}$	H25	DATA6	L26	DATA15
A08	ADDR13	B22	$\overline{\text{ABE1}}$	H26	DATA9	M01	VROUT0
A09	ADDR11	B23	$\overline{\text{ABE3}}$	J01	CLKIN	M02	GND
A10	ADDR09	B24	ADDR07	J02	GND	M10	VDDEXT
A11	$\overline{\text{AMS3}}$	B25	GND	J10	VDDEXT	M11	GND
A12	$\overline{\text{AMS1}}$	B26	ADDR05	J11	VDDEXT	M12	GND
A13	$\overline{\text{AWE}}$	C01	PPI0SYNC3	J12	VDDEXT	M13	GND
A14	$\overline{\text{ARE}}$	C02	PPI0CLK	J13	VDDEXT	M14	GND
A15	$\overline{\text{SMS0}}$	C03	GND	J14	VDDEXT	M15	GND
A16	$\overline{\text{SMS2}}$	C04	GND	J15	VDDEXT	M16	GND
A17	$\overline{\text{SRAS}}$	C05	GND	J16	VDDINT	M17	GND
A18	$\overline{\text{SCAS}}$	C22	GND	J17	VDDINT	M18	VDDINT
A19	SCLK0	C23	GND	J18	VDDINT	M25	DATA14
A20	SCLK1	C24	GND	J25	DATA8	M26	DATA17
A21	$\overline{\text{BGH}}$	C25	ADDR04	J26	DATA11	N01	VROUT1
A22	$\overline{\text{ABE0}}$	C26	ADDR03	K01	XTAL	N02	PPI0D9
A23	$\overline{\text{ABE2}}$	D01	PPI0SYNC1	K02	NC	N10	VDDEXT
A24	ADDR08	D02	PPI0SYNC2	K10	VDDEXT	N11	GND
A25	ADDR06	D03	GND	K11	VDDEXT	N12	GND
A26	GND	D04	GND	K12	VDDEXT	N13	GND
B01	PPI1CLK	D23	GND	K13	VDDEXT	N14	GND
B02	GND	D24	GND	K14	VDDEXT	N15	GND
B03	ADDR24	D25	ADDR02	K15	VDDEXT	N16	GND
B04	ADDR22	D26	DATA1	K16	VDDINT	N17	GND
B05	ADDR20	E01	PPI0D15	K17	VDDINT	N18	VDDINT
B06	ADDR18	E02	PPI0D14	K18	VDDINT	N25	DATA16
B07	ADDR16	E03	GND	K25	DATA10	N26	DATA19
B08	ADDR14	E24	GND	K26	DATA13	P01	PPI0D7
B09	ADDR12	E25	DATA0	L01	NC	P02	PPI0D8
B10	ADDR10	E26	DATA3	L02	NC	P10	VDDEXT
B11	$\overline{\text{AMS2}}$	F01	PPI0D13	L10	VDDEXT	P11	GND
B12	$\overline{\text{AMS0}}$	F02	PPI0D12	L11	GND	P12	GND
B13	$\overline{\text{AOE}}$	F25	DATA2	L12	GND	P13	GND
B14	ARDY	F26	DATA5	L13	GND	P14	GND

OUTLINE DIMENSIONS

Dimensions in the outline dimension figures are shown in millimeters.

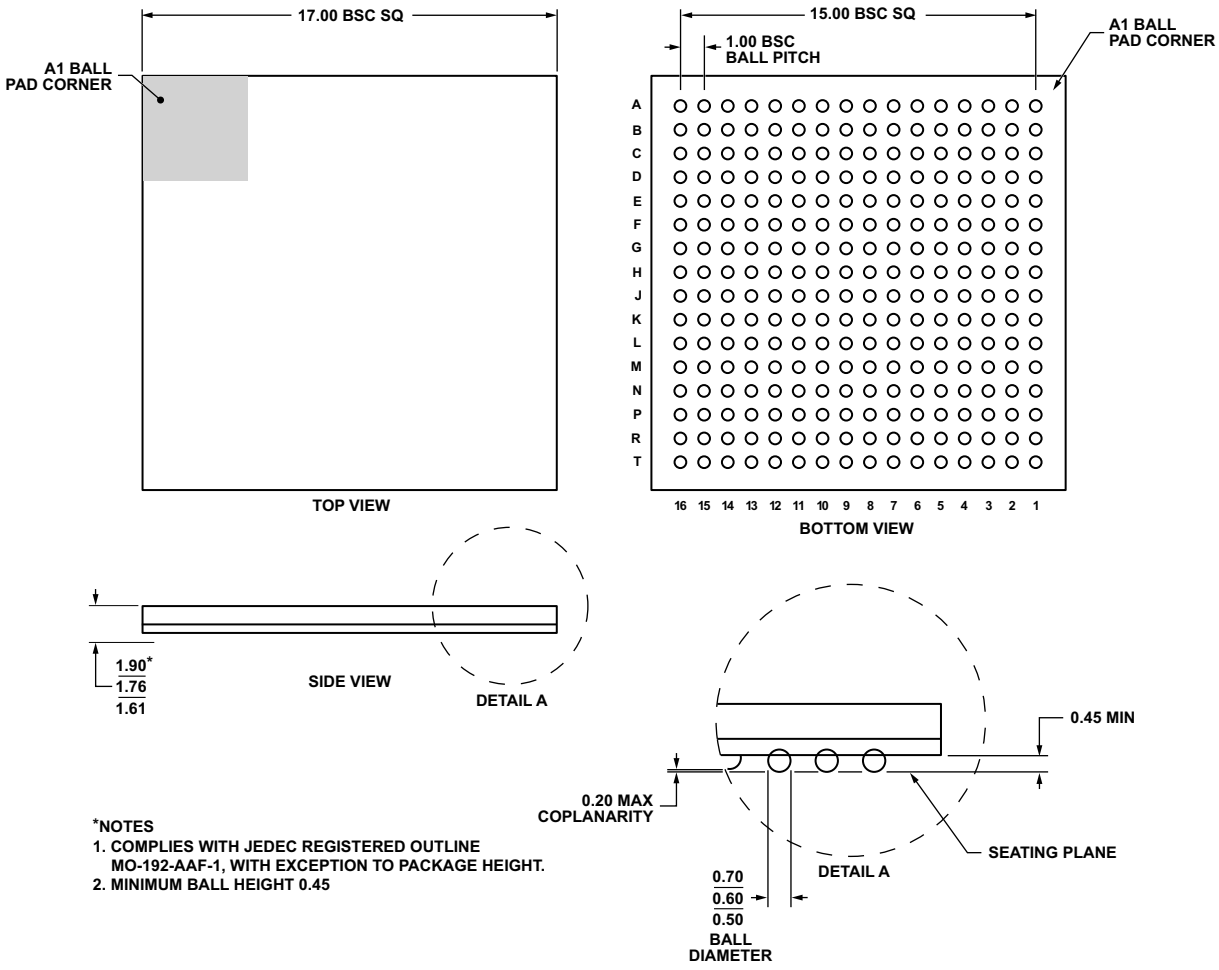
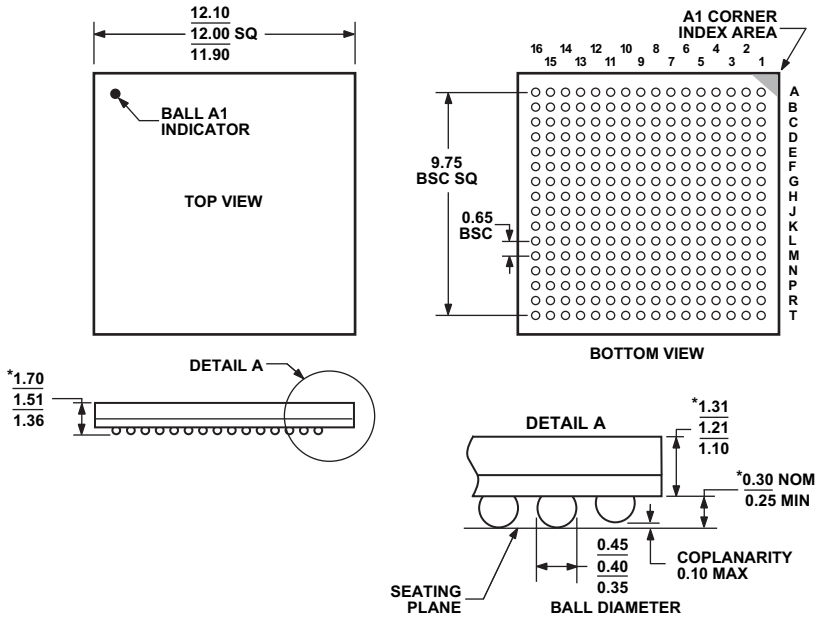
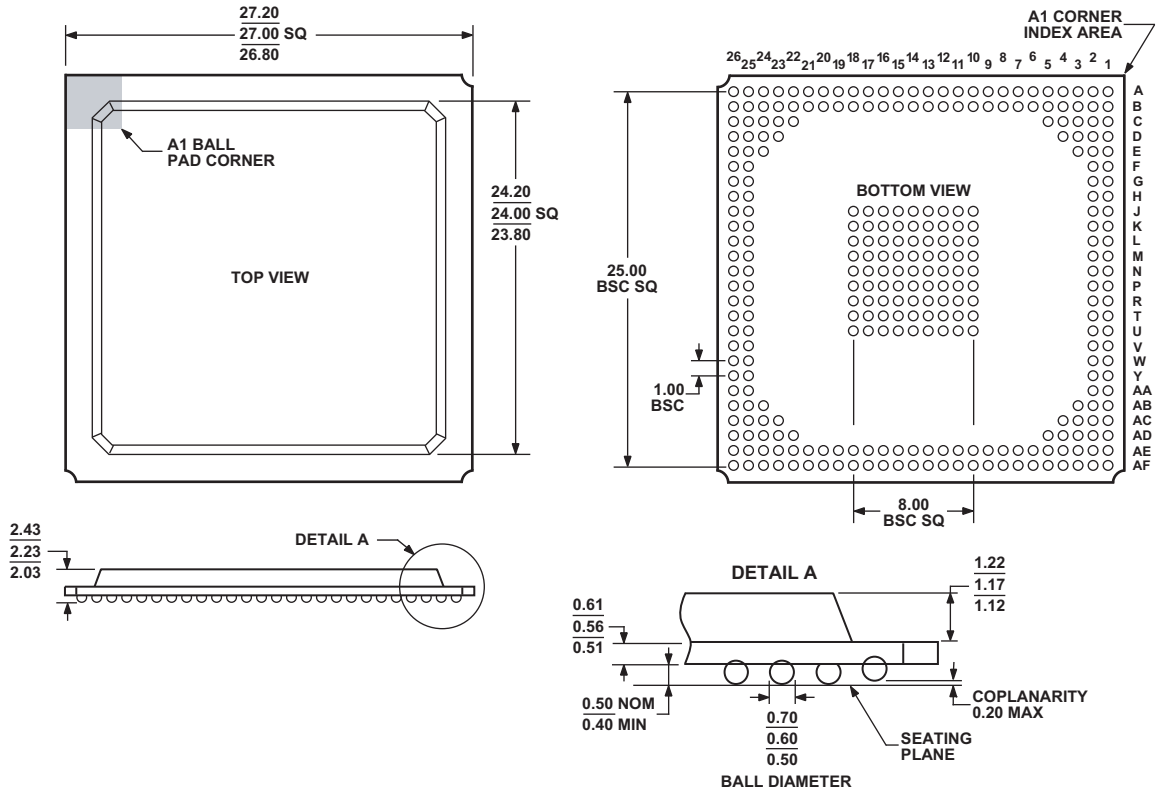


Figure 54. 256-Ball Chip Scale Package Ball Grid Array (CSP_BGA) (BC-256-4)



*COMPLIANT TO JEDEC STANDARDS MO-225 WITH EXCEPTION TO DIMENSIONS INDICATED BY AN ASTERISK.

Figure 55. 256-Ball Chip Scale Package Ball Grid Array (CSP_BGA) (BC-256-1)



COMPLIANT TO JEDEC STANDARDS MS-034-AAL-1

Figure 56. 297-Ball Plastic Ball Grid Array (PBGA) (B-297)

SURFACE-MOUNT DESIGN

Table 41 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Table 41. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
256-Ball CSP_BGA (BC-256-1)	Solder Mask Defined	0.30 mm diameter	0.43 mm diameter
256-Ball CSP_BGA (BC-256-4)	Solder Mask Defined	0.43 mm diameter	0.55 mm diameter
297-Ball PBGA (B-297)	Solder Mask Defined	0.43 mm diameter	0.58 mm diameter

AUTOMOTIVE PRODUCTS

Some ADSP-BF561 models are available for automotive applications with controlled manufacturing. Note that these special models may have specifications that differ from the general release models.

The automotive grade products shown in Table 42 are available for use in automotive applications. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

Table 42. Automotive Products

Product Family[1]	Temperature Range[2]	Speed Grade (Max)[3]	Package Description	Package Option
ADBF561WBBZ5xx	–40°C to +85°C	533 MHz	297-Ball PBGA	B-297
ADBF561WBBCZ5xx	–40°C to +85°C	533 MHz	256-Ball CSP_BGA	BC-256-4

[1] xx denotes silicon revision.
[2] Referenced temperature is ambient temperature.
[3] The internal voltage regulation feature is not available. External voltage regulation is required to ensure correct operation.

ORDERING GUIDE

Model	Temperature Range[1]	Speed Grade (Max)	Package Description	Package Option
ADSP-BF561SKBCZ-6V[2]	0°C to +70°C	600 MHz	256-Ball CSP_BGA	BC-256-1
ADSP-BF561SKBCZ-5V[2]	0°C to +70°C	533 MHz	256-Ball CSP_BGA	BC-256-1
ADSP-BF561SKBCZ500[2]	0°C to +70°C	500 MHz	256-Ball CSP_BGA	BC-256-1
ADSP-BF561SKB500	0°C to +70°C	500 MHz	297-Ball PBGA	B-297
ADSP-BF561SKB600	0°C to +70°C	600 MHz	297-Ball PBGA	B-297
ADSP-BF561SKBZ500[2]	0°C to +70°C	500 MHz	297-Ball PBGA	B-297
ADSP-BF561SKBZ600[2]	0°C to +70°C	600 MHz	297-Ball PBGA	B-297
ADSP-BF561SBB600	–40°C to +85°C	600 MHz	297-Ball PBGA	B-297
ADSP-BF561SBB500	–40°C to +85°C	500 MHz	297-Ball PBGA	B-297
ADSP-BF561SBBZ600[2]	–40°C to +85°C	600 MHz	297-Ball PBGA	B-297
ADSP-BF561SBBZ500[2]	–40°C to +85°C	500 MHz	297-Ball PBGA	B-297
ADSP-BF561SKBCZ-6A[2]	0°C to +70°C	600 MHz	256-Ball CSP_BGA	BC-256-4
ADSP-BF561SKBCZ-5A[2]	0°C to +70°C	500 MHz	256-Ball CSP_BGA	BC-256-4
ADSP-BF561SBBCZ-5A[2]	–40°C to +85°C	500 MHz	256-Ball CSP_BGA	BC-256-4

[1] Referenced temperature is ambient temperature.
[2] Z = RoHS compliant part.