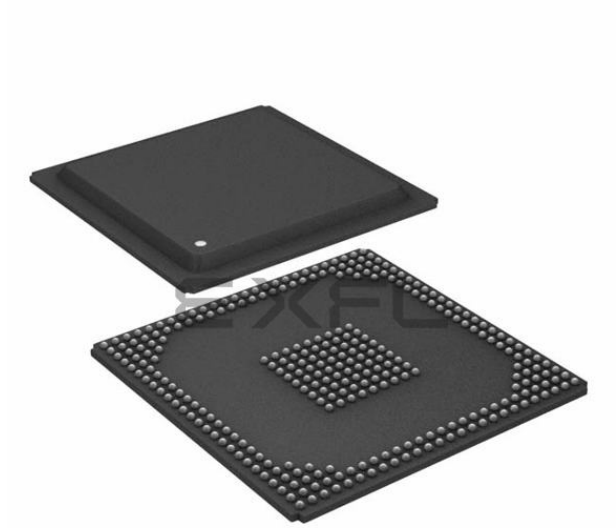

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	500MHz
Non-Volatile Memory	External
On-Chip RAM	328kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.25V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	297-BGA
Supplier Device Package	297-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf561skb500

GENERAL DESCRIPTION

The ADSP-BF561 processor is a high performance member of the Blackfin® family of products targeting a variety of multimedia, industrial, and telecommunications applications. At the heart of this device are two independent Analog Devices Blackfin processors. These Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantage of a clean, orthogonal RISC-like microprocessor instruction set, and single instruction, multiple data (SIMD) multimedia capabilities in a single instruction set architecture.

The ADSP-BF561 processor has 328K bytes of on-chip memory. Each Blackfin core includes:

- 16K bytes of instruction SRAM/cache
- 16K bytes of instruction SRAM
- 32K bytes of data SRAM/cache
- 32K bytes of data SRAM
- 4K bytes of scratchpad SRAM

Additional on-chip memory peripherals include:

- 128K bytes of low latency on-chip L2 SRAM
- Four-channel internal memory DMA controller
- External memory controller with glueless support for SDRAM, mobile SDRAM, SRAM, and flash.

PORTABLE LOW POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. Blackfin processors are designed in a low power and low voltage design methodology and feature dynamic power management, the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. Varying the voltage and frequency can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This translates into longer battery life for portable appliances.

BLACKFIN PROCESSOR CORE

As shown in Figure 2, each Blackfin core contains two multiplier/accumulators (MACs), two 40-bit ALUs, four video ALUs, and a single shifter. The computational units process 8-bit, 16-bit, or 32-bit data from the register file.

Each MAC performs a 16-bit by 16-bit multiply in every cycle, with accumulation to a 40-bit result, providing eight bits of extended precision. The ALUs perform a standard set of arithmetic and logical operations. With two ALUs capable of operating on 16-bit or 32-bit data, the flexibility of the computation units covers the signal processing requirements of a varied set of application needs.

Each of the two 32-bit input registers can be regarded as two 16-bit halves, so each ALU can accomplish very flexible single 16-bit arithmetic operations. By viewing the registers as pairs of 16-bit operands, dual 16-bit or single 32-bit operations can be accomplished in a single cycle. By further taking advantage of the second ALU, quad 16-bit operations can be accomplished simply, accelerating the per cycle throughput.

The powerful 40-bit shifter has extensive capabilities for performing shifting, rotating, normalization, extraction, and depositing of data. The data for the computational units is found in a multiported register file of sixteen 16-bit entries or eight 32-bit entries.

A powerful program sequencer controls the flow of instruction execution, including instruction alignment and decoding. The sequencer supports conditional jumps and subroutine calls, as well as zero overhead looping. A loop buffer stores instructions locally, eliminating instruction memory accesses for tight looped code.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches from memory. The DAGs share a register file containing four sets of 32-bit Index, Modify, Length, and Base registers. Eight additional 32-bit registers provide pointers for general indexing of variables and stack locations.

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. Level 2 (L2) memories are other memories, on-chip or off-chip, that may take multiple processor cycles to access. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information. At the L2 level, there is a single unified memory space, holding both instructions and data.

In addition, half of L1 instruction memory and half of L1 data memory may be configured as either Static RAMs (SRAMs) or caches. The Memory Management Unit (MMU) provides memory protection for individual tasks that may be operating on the core and may protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin instruction set has been optimized so that 16-bit op-codes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit op-codes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the VisualDSP C/C++ compiler, resulting in fast and efficient software implementations.

writing the appropriate values into the Interrupt Assignment Registers (SIC_IAR7–0). Table 2 describes the inputs into the SIC and the default mappings into the CEC.

Table 2. System Interrupt Controller (SIC)

Peripheral Interrupt Event	Default Mapping
PLL Wakeup	IVG7
DMA1 Error (Generic)	IVG7
DMA2 Error (Generic)	IVG7
IMDMA Error	IVG7
PPI0 Error	IVG7
PPI1 Error	IVG7
SPORT0 Error	IVG7
SPORT1 Error	IVG7
SPI Error	IVG7
UART Error	IVG7
Reserved	IVG7
DMA1 Channel 0 Interrupt (PPI0)	IVG8
DMA1 Channel 1 Interrupt (PPI1)	IVG8
DMA1 Channel 2 Interrupt	IVG8
DMA1 Channel 3 Interrupt	IVG8
DMA1 Channel 4 Interrupt	IVG8
DMA1 Channel 5 Interrupt	IVG8
DMA1 Channel 6 Interrupt	IVG8
DMA1 Channel 7 Interrupt	IVG8
DMA1 Channel 8 Interrupt	IVG8
DMA1 Channel 9 Interrupt	IVG8
DMA1 Channel 10 Interrupt	IVG8
DMA1 Channel 11 Interrupt	IVG8
DMA2 Channel 0 Interrupt (SPORT0 Rx)	IVG9
DMA2 Channel 1 Interrupt (SPORT0 Tx)	IVG9
DMA2 Channel 2 Interrupt (SPORT1 Rx)	IVG9
DMA2 Channel 3 Interrupt (SPORT1 Tx)	IVG9
DMA2 Channel 4 Interrupt (SPI)	IVG9
DMA2 Channel 5 Interrupt (UART Rx)	IVG9
DMA2 Channel 6 Interrupt (UART Tx)	IVG9
DMA2 Channel 7 Interrupt	IVG9
DMA2 Channel 8 Interrupt	IVG9
DMA2 Channel 9 Interrupt	IVG9
DMA2 Channel 10 Interrupt	IVG9
DMA2 Channel 11 Interrupt	IVG9
Timer0 Interrupt	IVG10
Timer1 Interrupt	IVG10
Timer2 Interrupt	IVG10
Timer3 Interrupt	IVG10
Timer4 Interrupt	IVG10
Timer5 Interrupt	IVG10
Timer6 Interrupt	IVG10
Timer7 Interrupt	IVG10
Timer8 Interrupt	IVG10
Timer9 Interrupt	IVG10
Timer10 Interrupt	IVG10
Timer11 Interrupt	IVG10
Programmable Flags 15–0 Interrupt A	IVG11
Programmable Flags 15–0 Interrupt B	IVG11
Programmable Flags 31–16 Interrupt A	IVG11
Programmable Flags 31–16 Interrupt B	IVG11
Programmable Flags 47–32 Interrupt A	IVG11
Programmable Flags 47–32 Interrupt B	IVG11
DMA1 Channel 12/13 Interrupt (Memory DMA/Stream 0)	IVG8
DMA1 Channel 14/15 Interrupt (Memory DMA/Stream 1)	IVG8
DMA2 Channel 12/13 Interrupt (Memory DMA/Stream 0)	IVG9
DMA2 Channel 14/15 Interrupt (Memory DMA/Stream 1)	IVG9
IMDMA Stream 0 Interrupt	IVG12
IMDMA Stream 1 Interrupt	IVG12
Watchdog Timer Interrupt	IVG13
Reserved	IVG7
Reserved	IVG7
Supplemental Interrupt 0	IVG7
Supplemental Interrupt 1	IVG7

Event Control

The ADSP-BF561 provides the user with a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each of the registers is 16 bits wide, while each bit represents a particular event class.

- CEC Interrupt Latch Register (ILAT) – The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but may also be written to clear (cancel) latched events. This register may be read while in supervisor mode and may only be written while in supervisor mode when the corresponding IMASK bit is cleared.
- CEC Interrupt Mask Register (IMASK) – The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and will be processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, thereby preventing the processor from servicing the event

PIN DESCRIPTIONS

ADSP-BF561 pin definitions are listed in Table 8. In order to maintain maximum function and reduce package size and pin count, some pins have multiple functions. In cases where pin function is reconfigurable, the default state is shown in plain text, while alternate functionality is shown in italics.

All pins are three-stated during and immediately after reset, except the external memory interface, asynchronous memory control, and synchronous memory control pins. These pins are all driven high, with the exception of CLKOUT, which toggles at the system clock rate. However if $\overline{BR}$ is active, the memory pins are also three-stated.

All I/O pins have their input buffers disabled, with the exception of the pins that need pull-ups or pull-downs if unused, as noted in Table 8.

Table 8. Pin Descriptions

Pin Name	Type	Function	Driver Type[1]
EBIU			
ADDR25–2	O	Address Bus for Async/Sync Access	A
DATA31–0	I/O	Data Bus for Async/Sync Access	A
$\overline{ABE3–0}$/SDQM3–0	O	Byte Enables/Data Masks for Async/Sync Access	A
$\overline{BR}$	I	Bus Request (This pin should be pulled HIGH if not used.)	
$\overline{BG}$	O	Bus Grant	A
$\overline{BGH}$	O	Bus Grant Hang	A
EBIU (ASYNC)			
$\overline{AMS3–0}$	O	Bank Select	A
ARDY	I	Hardware Ready Control (This pin should be pulled HIGH if not used.)	
$\overline{AOE}$	O	Output Enable	A
$\overline{AWE}$	O	Write Enable	A
$\overline{ARE}$	O	Read Enable	A
EBIU (SDRAM)			
$\overline{SRAS}$	O	Row Address Strobe	A
$\overline{SCAS}$	O	Column Address Strobe	A
$\overline{SWE}$	O	Write Enable	A
SCKE	O	Clock Enable	A
SCLK0/CLKOUT	O	Clock Output Pin 0	B
SCLK1	O	Clock Output Pin 1	B
SA10	O	SDRAM A10 Pin	A
$\overline{SMS3–0}$	O	Bank Select	A

SPECIFICATIONS

Component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage[1]	Non automotive 500 MHz and 533 MHz speed grade models[2]	0.8	1.25	1.375	V
V_{DDINT}	Internal Supply Voltage[3]	600 MHz speed grade models[2]	0.8	1.35	1.4185	V
V_{DDINT}	Internal Supply Voltage[3]	Automotive grade models[2]	0.95	1.25	1.375	V
V_{DDEXT}	External Supply Voltage	Non automotive grade models[2]	2.25	2.5, or 3.3	3.6	V
V_{DDEXT}	External Supply Voltage	Automotive grade models[2]	2.7	3.3	3.6	V
V_{IH}	High Level Input Voltage[4, 5]		2.0		3.6	V
V_{IL}	Low Level Input Voltage[5]		–0.3		+0.6	V
T_J	Junction Temperature	256-Ball CSP_BGA (12 mm × 12 mm) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+105	°C
T_J	Junction Temperature	256-Ball CSP_BGA (17 mm × 17 mm) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
T_J	Junction Temperature	256-Ball CSP_BGA (17 mm × 17 mm) @ $T_{AMBIENT}$ =–40°C to +85°C	–40		+115	°C
T_J	Junction Temperature	297-Ball PBGA @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
T_J	Junction Temperature	297-Ball PBGA @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+115	°C

[1] Internal voltage (V_{DDINT}) regulator tolerance is –5% to +10% for all models.
[2] See Ordering Guide on Page 63.
[3] The internal voltage regulation feature is not available. External voltage regulation is required to ensure correct operation.
[4] The ADSP-BF561 is 3.3 V tolerant (always accepts up to 3.6 V maximum V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}, because V_{OH} (maximum) approximately equals V_{DDEXT} (maximum). This 3.3 V tolerance applies to bidirectional and input only pins.
[5] Applies to all signal pins.

Table 9 and Table 10 describe the timing requirements for the ADSP-BF561 clocks ($t_{CCLK} = 1/f_{CCLK}$). Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock, system clock, and Voltage Controlled Oscillator (VCO) operating frequencies, as described in Absolute Maximum Ratings on Page 22. Table 11 describes phase-locked loop operating conditions.

Table 9. Core Clock (CCLK) Requirements—500 MHz and 533 MHz Speed Grade Models[1]

Parameter		Max	Unit
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.235 Vminimum)[2]	533	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.1875 Vminimum)	500	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.045 Vminimum)	444	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.95 Vminimum)	350	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.855 Vminimum)[3]	300	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.8 V minimum)[3]	250	MHz

[1] See Ordering Guide on Page 63.
[2] External Voltage regulation is required on automotive grade models (see Ordering Guide on Page 63) to ensure correct operation.
[3] Not applicable to automotive grade models. See Ordering Guide on Page 63.

Table 10. Core Clock (CCLK) Requirements—600 MHz Speed Grade Models[1]

Parameter		Max	Unit
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.2825 V minimum)[2]	600	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.235 V minimum)	533	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.1875 V minimum)	500	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 1.045 V minimum)	444	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.95 V minimum)	350	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.855 V minimum)	300	MHz
f_{CCLK}	CCLK Frequency (V_{DDINT} = 0.8 V minimum)	250	MHz

[1] See Ordering Guide on Page 63.
[2] External voltage regulator required to ensure proper operation at 600 MHz.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 13 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 13. Absolute Maximum Ratings

Parameter	Value
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.42 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.5 V to +3.8 V
Input Voltage[1]	–0.5 V to +3.8 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance[2]	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature Under Bias	125°C

[1] Applies to 100% transient duty cycle. For other duty cycles see Table 14.
[2] For proper SDRAM controller operation, the maximum load capacitance is 50 pF (at 3.3 V) or 30 pF (at 2.5 V) for ADDR19–1, DATA15–0, ABE1–0/SDQM1–0, CLKOUT, SCKE, SA10, SRAS, SCAS, SWE, and SMS.

Table 14. Maximum Duty Cycle for Input Transient Voltage[1]

V_{IN} Min (V)	V_{IN} Max (V)[2]	Maximum Duty Cycle
–0.50	3.80	100%
–0.70	4.00	40%
–0.80	4.10	25%
–0.90	4.20	15%
–1.00	4.30	10%

[1] Applies to all signal pins with the exception of CLKIN, XTAL, VROUT1–0.
[2] Only one of the listed options can apply to a particular design.

PACKAGE INFORMATION

The information presented in Figure 7 and Table 15 provides details about the package branding for the Blackfin processors. For a complete listing of product availability, see the Ordering Guide on Page 63.

Figure 7. Product Information on Package

Table 15. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

Clock and Reset Timing

Table 16 and Figure 8 describe clock and reset operations. Per Absolute Maximum Ratings on Page 22, combinations of CLKIN and clock multipliers must not result in core/system clocks exceeding the maximum limits allowed for the processor, including system clock restrictions related to supply voltage.

Table 16. Clock and Normal Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN (to PLL) Period[1, 2, 3]	25.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse	10.0		ns
t_{CKINH}	CLKIN High Pulse	10.0		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[4]	$11 \times t_{CKIN}$		ns

[1] If DF bit in PLL_CTL register is set t_{CLKIN} is divided by two before going to PLL, then the t_{CLKIN} maximum period is 50 ns and the t_{CLKIN} minimum period is 12.5 ns.
[2] Applies to PLL bypass mode and PLL nonbypass mode.
[3] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 9 on Page 20 through Table 12 on Page 21.
[4] Applies after power-up sequence is complete. See Table 17 and Figure 9 for power-up reset timing.

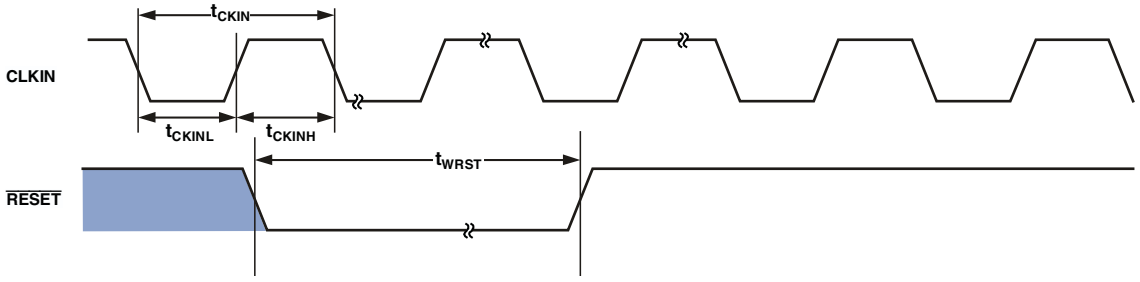


Figure 8. Clock and Normal Reset Timing

Table 17. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted after the V_{DDINT}, V_{DDEXT}, and CLKIN Pins are Stable and Within Specification	$3500 \times t_{CKIN}$		µs

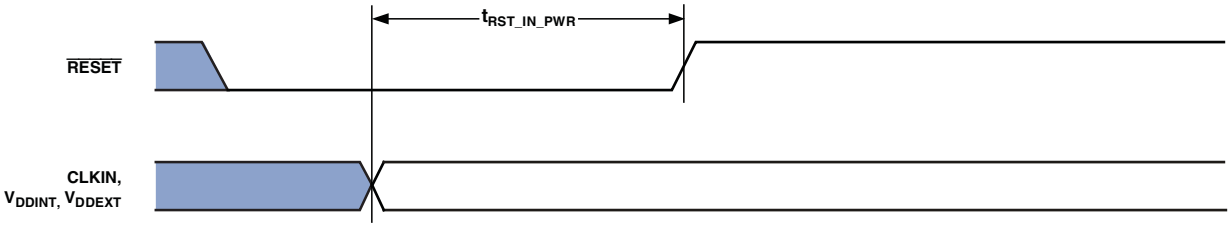


Figure 9. Power-Up Reset Timing

Asynchronous Memory Write Cycle Timing

Table 19. Asynchronous Memory Write Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
Switching Characteristics				
t_{DDAT}	DATA31–0 Disable After CLKOUT		6.0	ns
t_{ENDAT}	DATA31–0 Enable After CLKOUT	1.0		ns
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE3-0}$, ADDR25–2, DATA31–0, $\overline{AOE}$, $\overline{AWE}$.

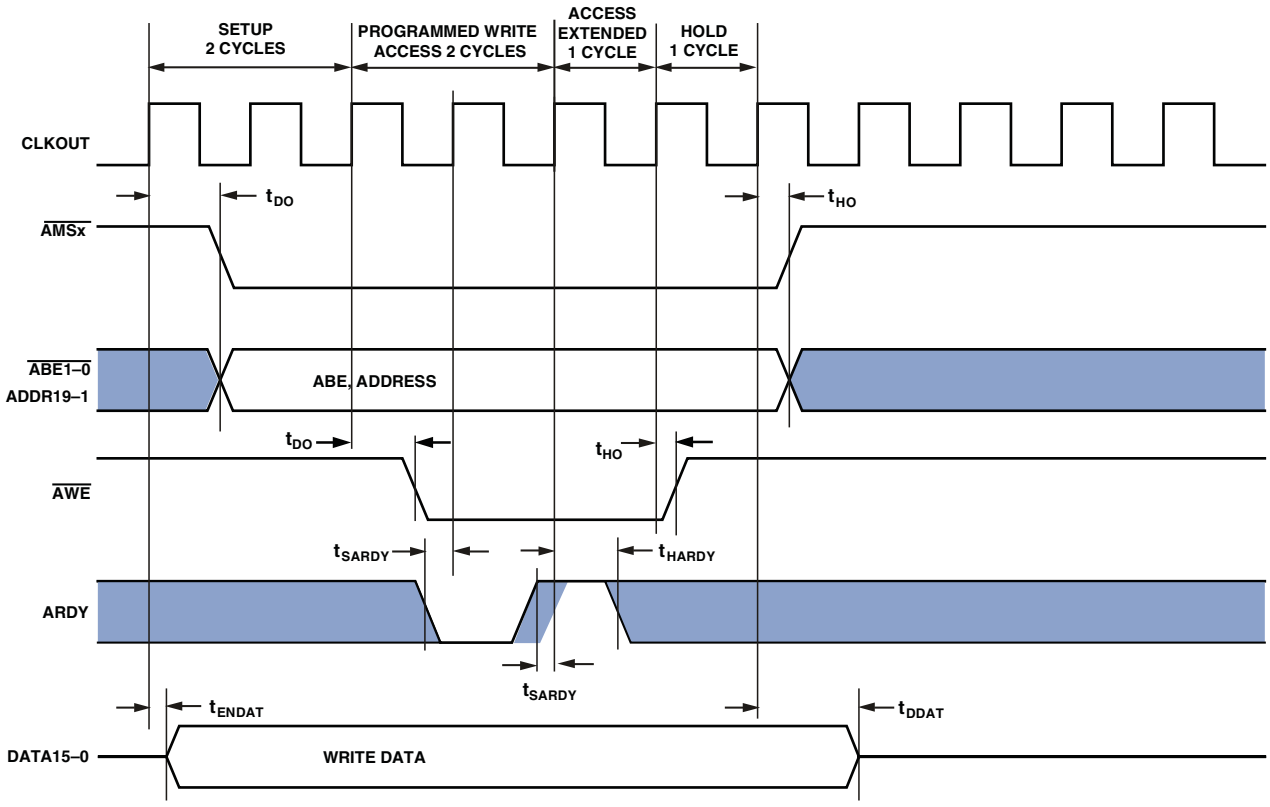


Figure 11. Asynchronous Memory Write Cycle Timing

Parallel Peripheral Interface Timing

Table 22, and Figure 14 through Figure 17 on Page 30, describe default Parallel Peripheral Interface operations.

If bit 4 of the PLL_CTL register is set, then Figure 18 on Page 30 and Figure 19 on Page 31 apply.

Table 22. Parallel Peripheral Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	PPIxCLK Width[1]	5.0		ns
t_{PCLK}	PPIxCLK Period[1]	13.3		ns
t_{SFSPE}	External Frame Sync Setup Before PPIxCLK	4.0		ns
t_{HFSPE}	External Frame Sync Hold After PPIxCLK	1.0		ns
t_{SDRPE}	Receive Data Setup Before PPIxCLK	3.5		ns
t_{HDRPE}	Receive Data Hold After PPIxCLK	2.0		ns
Switching Characteristics				
t_{DFSPE}	Internal Frame Sync Delay After PPIxCLK		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPIxCLK	1.7		ns
t_{DDTPE}	Transmit Data Delay After PPIxCLK		8.0	ns
t_{HDTPE}	Transmit Data Hold After PPIxCLK	2.0		ns

[1] For PPI modes that use an internally generated frame sync, the PPIxCLK frequency cannot exceed $f_{SCLK}/2$. For modes with no frame syncs or external frame syncs, PPIxCLK cannot exceed 75 MHz and f_{SCLK} should be equal to or greater than PPIxCLK.

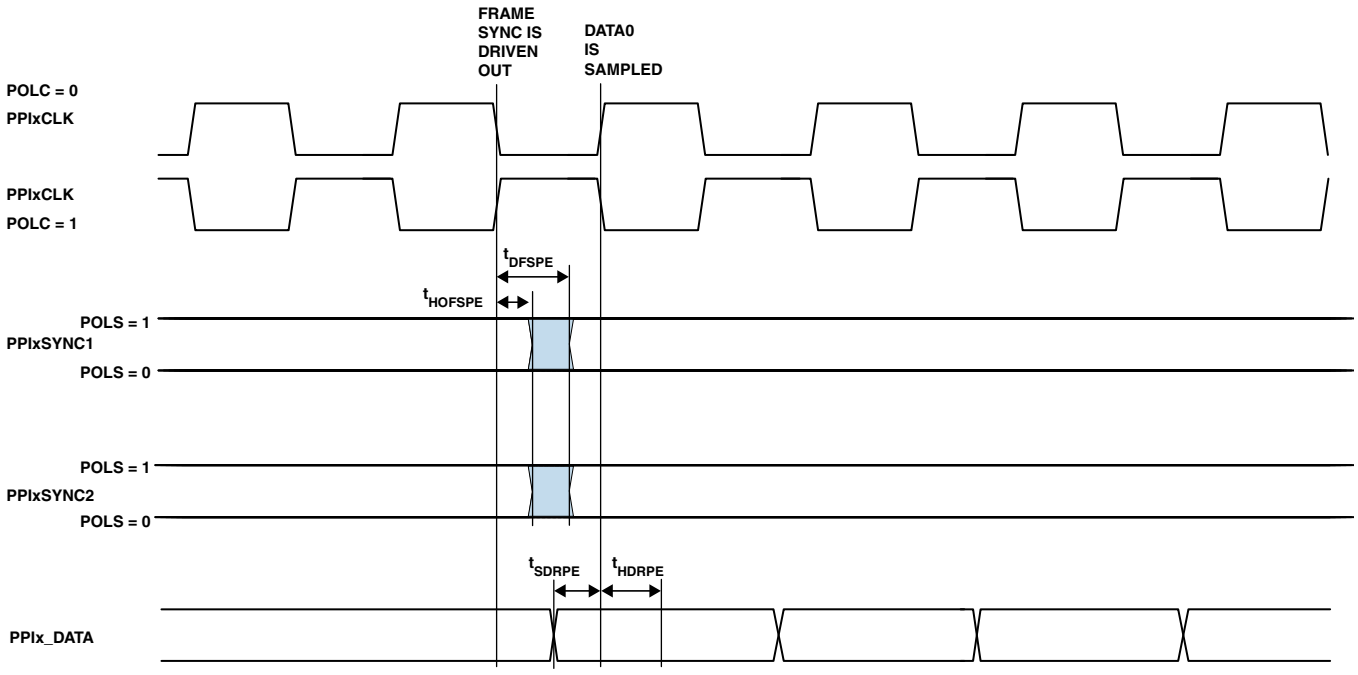


Figure 14. PPI GP Rx Mode with Internal Frame Sync Timing (Default)

Table 25. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1]		10.0	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	–2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1]		3.0	ns

[1] Referenced to drive edge.

Table 26. External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFSx or External RFSx with MCMEN = 1, MFD = 0[1, 2]		10.0	ns
$t_{DTENLFS}$	Data Enable from Late FS or MCMEN = 1, MFD = 0[1, 2]	0		ns

[1] MCMEN = 1, TFSx enable and TFSx valid follow $t_{DTENLFS}$ and $t_{DDTLFSE}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$, then $t_{DDTTE/I}$ and $t_{DTENE/I}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

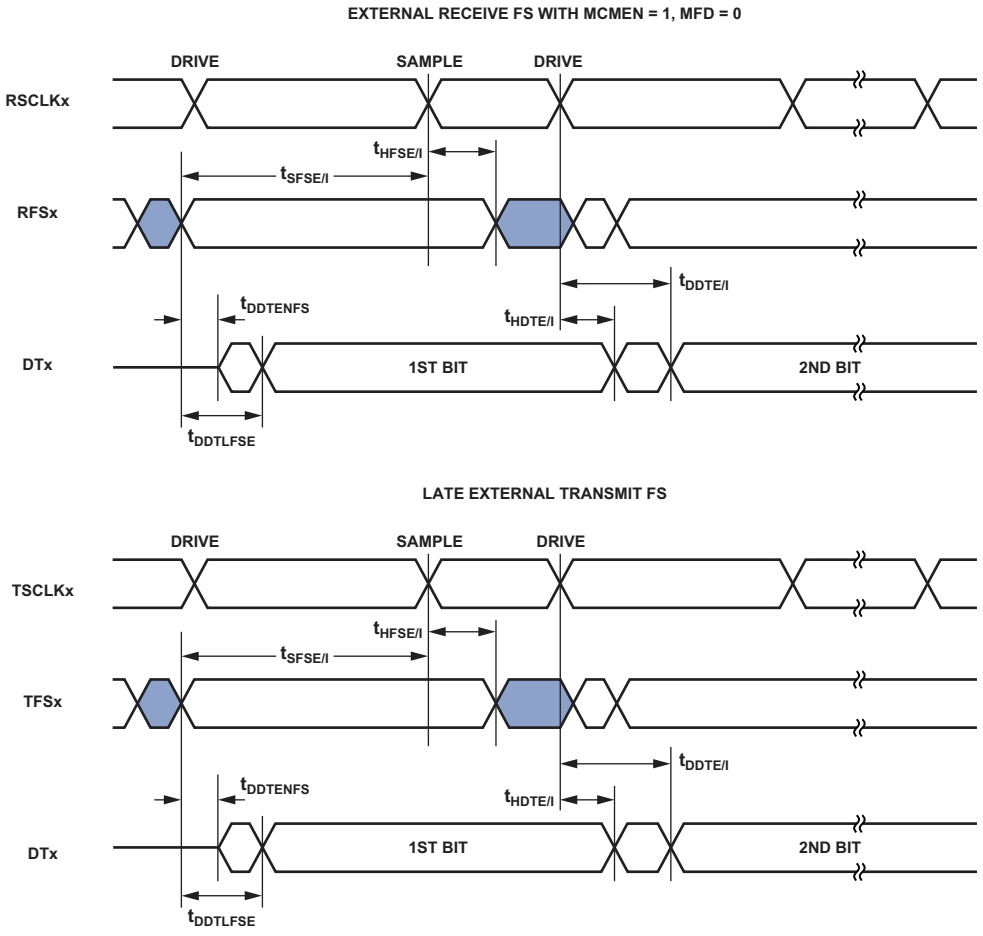


Figure 22. External Late Frame Sync

Serial Peripheral Interface (SPI) Port— Master Timing

Table 27 and Figure 23 describe SPI port master operations.

Table 27. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	7.5		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		ns
Switching Characteristics				
t_{SDSCIM}	$\overline{SPISELx}$ Low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISELx}$ High	$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)	0	6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1.0	+4.0	ns

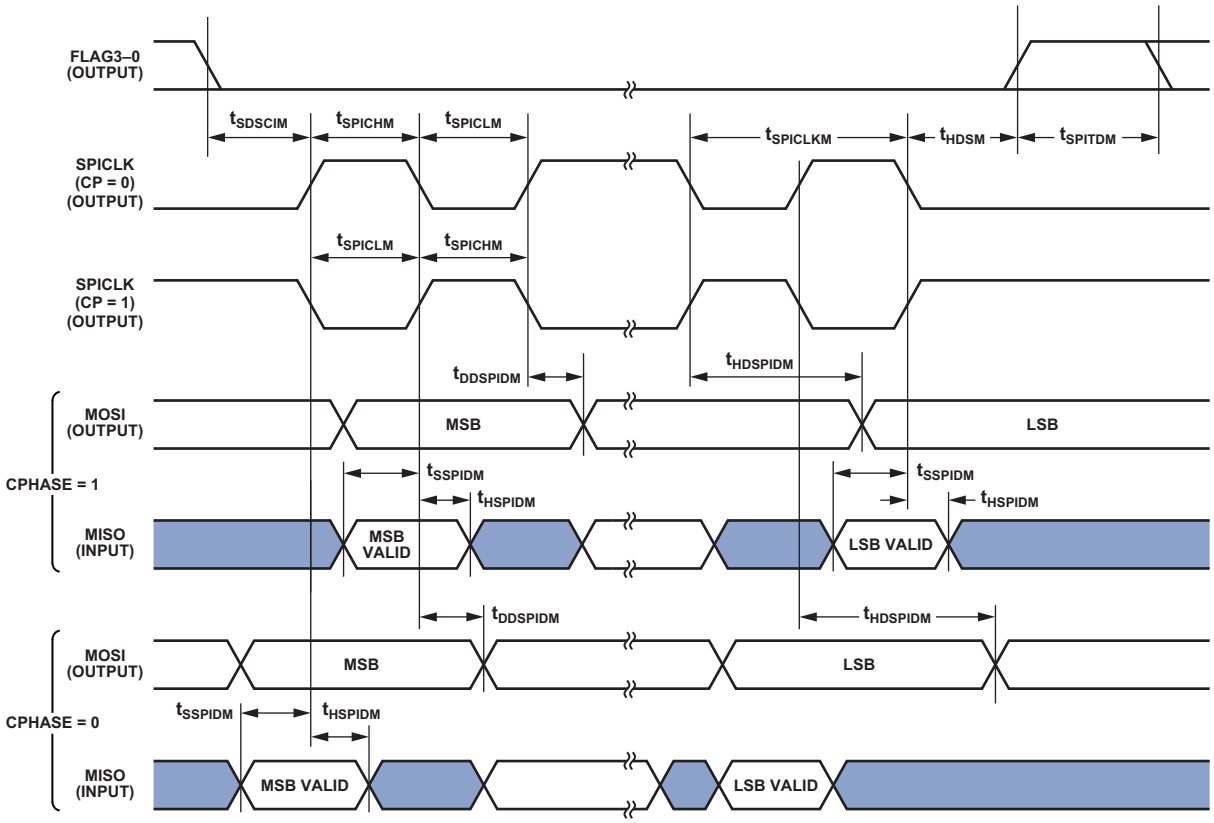


Figure 23. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port— Slave Timing

Table 28 and Figure 24 describe SPI port slave operations.

Table 28. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	8	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0	8	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)	0	10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0	10	ns

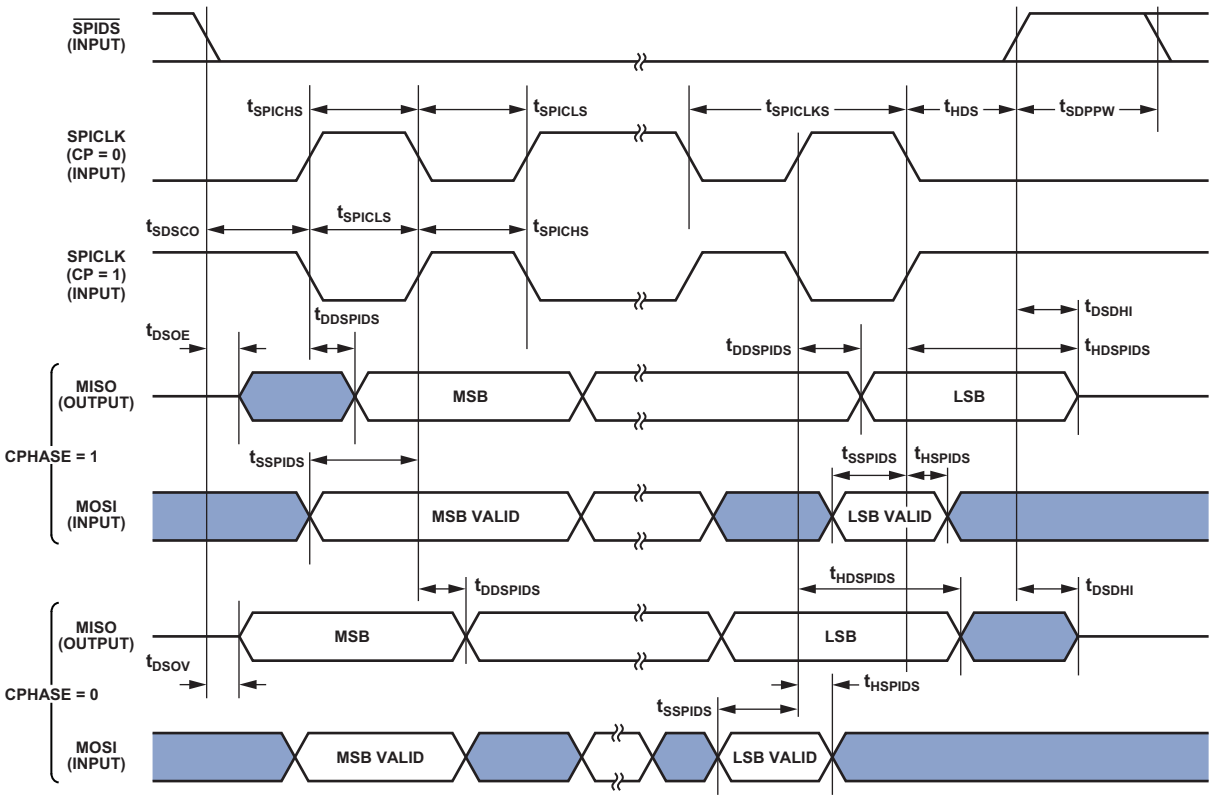


Figure 24. Serial Peripheral Interface (SPI) Port—Slave Timing

Universal Asynchronous Receiver Transmitter (UART) Port—Receive and Transmit Timing

Figure 25 describes UART port receive and transmit operations. The maximum baud rate is SCLK/16. As shown in Figure 25, there is some latency between the generation internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART.

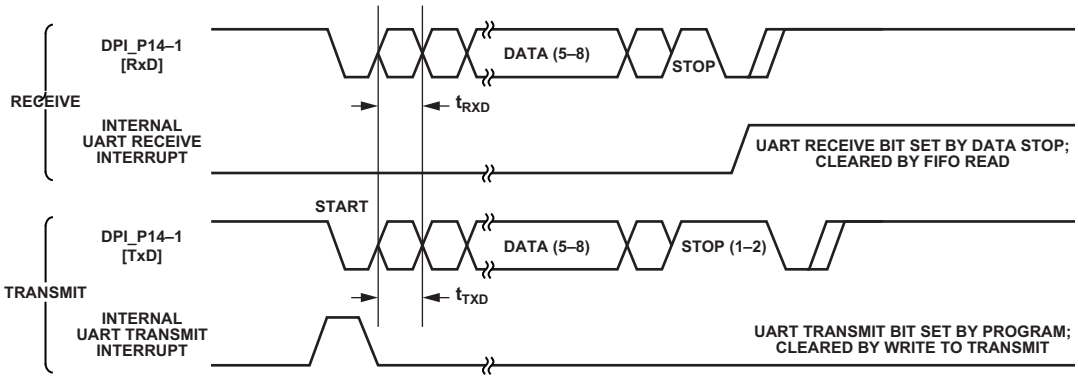


Figure 25. UART Port—Receive and Transmit Timing

The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load C_L and the load current I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V.

The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches, to when the output voltage decays ΔV from the measured output high or output low voltage.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-BF561 processor's output voltage and the input threshold for the device requiring the hold time. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the various output disable times as specified in the Timing Specifications on Page 23 (for example t_{DSDAT} for an SDRAM write cycle as shown in SDRAM Interface Timing on Page 26).

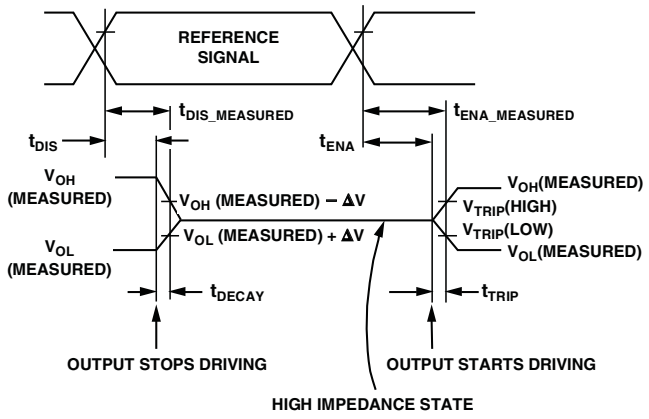


Figure 38. Output Enable/Disable

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 39). V_{LOAD} is 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V. Figure 40 through Figure 47 on Page 44 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.

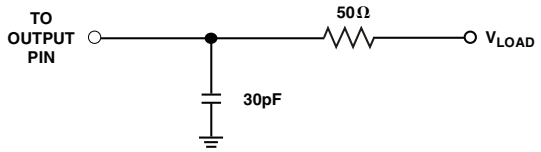


Figure 39. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

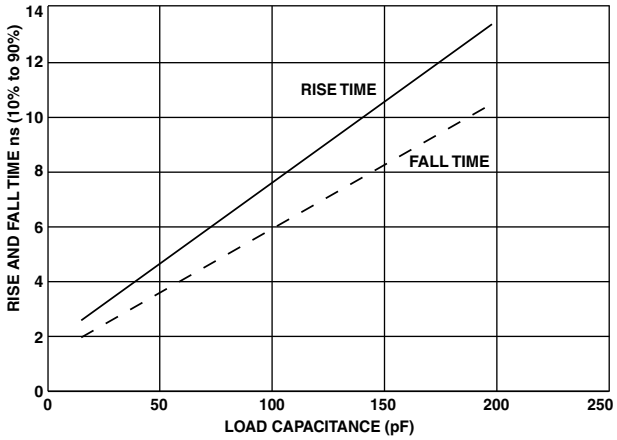


Figure 40. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver A at V_{DDEXT} (min)

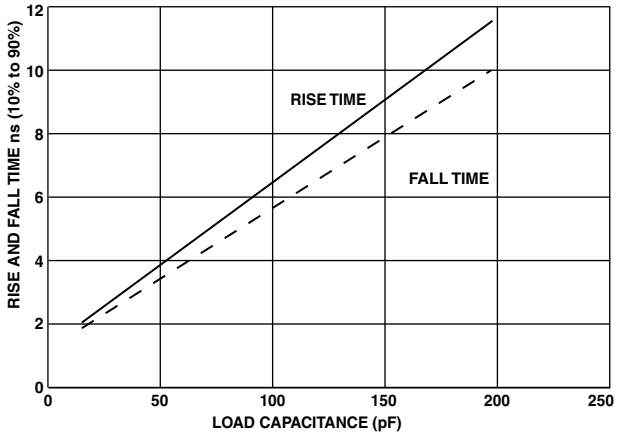


Figure 41. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver A at V_{DDEXT} (max)

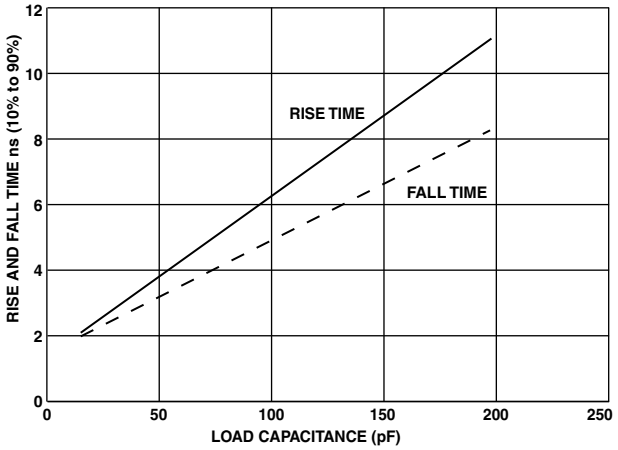


Figure 42. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver B at V_{DDEXT} (min)

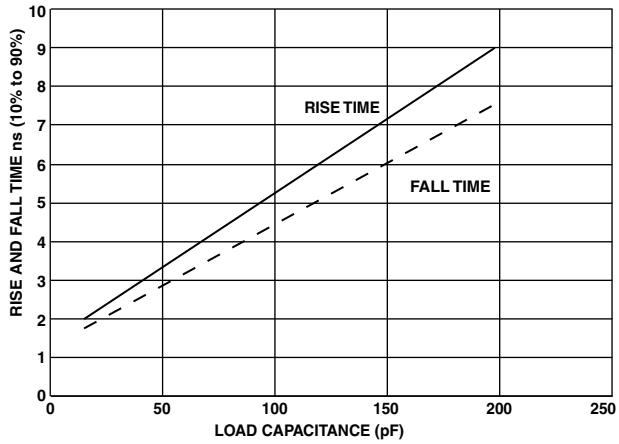


Figure 43. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver B at V_{DDEXT} (max)

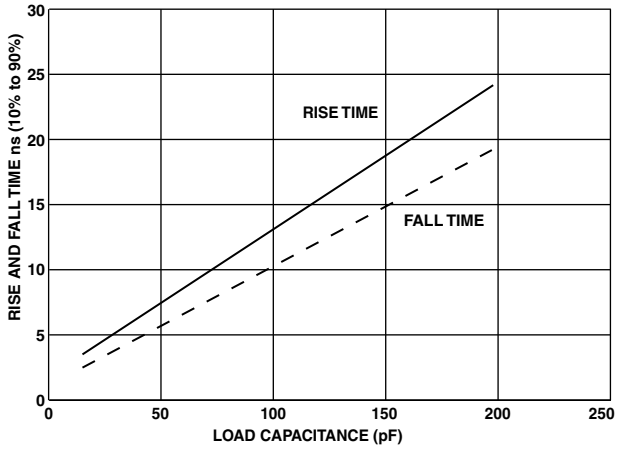


Figure 44. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver C at V_{DDEXT} (min)

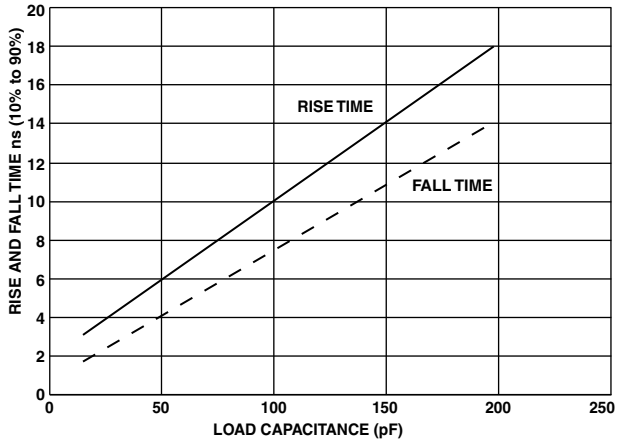


Figure 45. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver C at V_{DDEXT} (max)

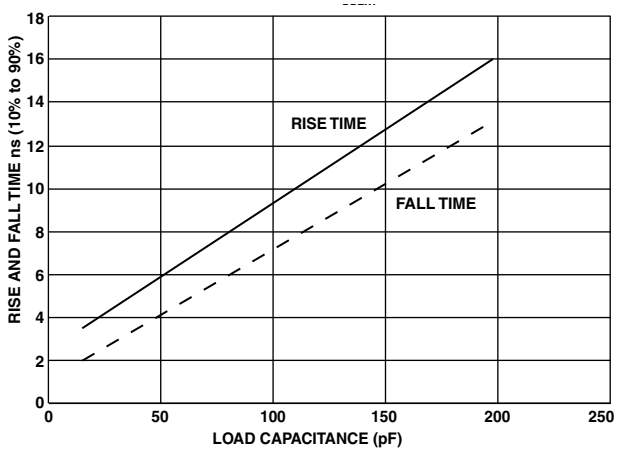


Figure 46. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver D at V_{DDEXT} (min)

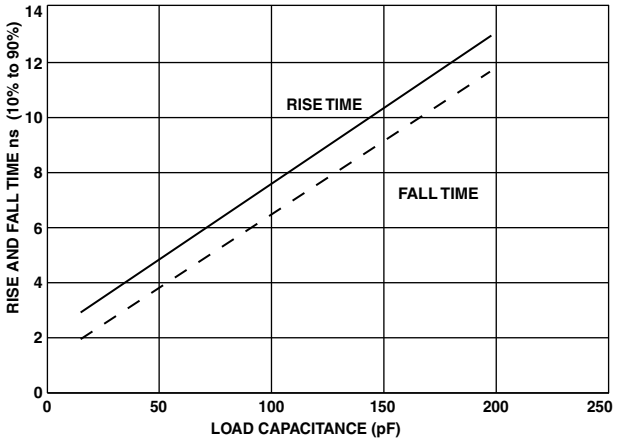


Figure 47. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver D at V_{DDEXT} (max)

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:
T_J = junction temperature (°C).

T_{CASE} = case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = from Table 32 on Page 45 through Table 34 on Page 45.

P_D = power dissipation (see Power Dissipation on Page 42 for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:
T_A = ambient temperature (°C).

256-BALL CSP_BGA (17 mm) BALL ASSIGNMENT

Table 35 lists the 256-Ball CSP_BGA (17 mm × 17 mm) ball assignment by ball number. Table 36 on Page 48 lists the ball assignment alphabetically by signal.

Table 35. 256-Ball CSP_BGA (17 mm × 17 mm) Ball Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	VDDEXT	C9	$\overline{\text{SMS3}}$	F1	CLKIN	H9	GND	L1	PPI0D3
A2	ADDR22	C10	$\overline{\text{SWE}}$	F2	PPI0D10	H10	GND	L2	PPI0D2
A3	ADDR18	C11	SA10	F3	$\overline{\text{RESET}}$	H11	GND	L3	PPI0D1
A4	ADDR14	C12	$\overline{\text{ABE0}}$	F4	BYPASS	H12	GND	L4	PPI0D0
A5	ADDR11	C13	ADDR07	F5	VDDEXT	H13	GND	L5	VDDEXT
A6	$\overline{\text{AMS3}}$	C14	ADDR04	F6	VDDEXT	H14	DATA21	L6	VDDEXT
A7	$\overline{\text{AMS0}}$	C15	DATA0	F7	VDDEXT	H15	DATA19	L7	VDDEXT
A8	ARDY	C16	DATA05	F8	GND	H16	DATA23	L8	VDDEXT
A9	$\overline{\text{SMS2}}$	D1	PPI0D15	F9	GND	J1	VROUT1	L9	GND
A10	SCLK0	D2	PPI0SYNC3	F10	VDDEXT	J2	PPI0D8	L10	VDDEXT
A11	SCLK1	D3	PPI0SYNC2	F11	VDDEXT	J3	PPI0D7	L11	VDDEXT
A12	$\overline{\text{ABE2}}$	D4	ADDR21	F12	VDDEXT	J4	PPI0D9	L12	VDDEXT
A13	$\overline{\text{ABE3}}$	D5	ADDR15	F13	DATA11	J5	GND	L13	NC
A14	ADDR06	D6	ADDR09	F14	DATA08	J6	GND	L14	DT0PRI
A15	ADDR03	D7	$\overline{\text{AWE}}$	F15	DATA10	J7	GND	L15	DATA31
A16	VDDEXT	D8	$\overline{\text{SMS0}}$	F16	DATA16	J8	GND	L16	DATA28
B1	ADDR24	D9	$\overline{\text{SRAS}}$	G1	XTAL	J9	GND	M1	PPI1SYNC2
B2	ADDR23	D10	$\overline{\text{SCAS}}$	G2	VDDEXT	J10	GND	M2	PPI1D15
B3	ADDR19	D11	$\overline{\text{BGH}}$	G3	VDDEXT	J11	GND	M3	PPI1D14
B4	ADDR17	D12	$\overline{\text{ABE1}}$	G4	GND	J12	VDDINT	M4	PPI1D9
B5	ADDR12	D13	DATA02	G5	GND	J13	VDDINT	M5	VDDINT
B6	ADDR10	D14	DATA01	G6	VDDEXT	J14	DATA20	M6	VDDINT
B7	$\overline{\text{AMS1}}$	D15	DATA03	G7	GND	J15	DATA22	M7	GND
B8	$\overline{\text{AOE}}$	D16	DATA07	G8	GND	J16	DATA24	M8	VDDINT
B9	$\overline{\text{SMS1}}$	E1	PPI0D11	G9	GND	K1	PPI0D6	M9	GND
B10	SCKE	E2	PPI0D13	G10	GND	K2	PPI0D5	M10	VDDINT
B11	$\overline{\text{BR}}$	E3	PPI0D12	G11	VDDEXT	K3	PPI0D4	M11	GND
B12	$\overline{\text{BG}}$	E4	PPI0D14	G12	VDDEXT	K4	PPI1SYNC3	M12	VDDINT
B13	ADDR08	E5	PPI1CLK	G13	DATA17	K5	VDDEXT	M13	RSCLK0
B14	ADDR05	E6	VDDINT	G14	DATA14	K6	VDDEXT	M14	DR0PRI
B15	ADDR02	E7	GND	G15	DATA15	K7	GND	M15	TSCLK0
B16	DATA04	E8	VDDINT	G16	DATA18	K8	GND	M16	DATA29
C1	PPI0SYNC1	E9	GND	H1	VROUT0	K9	GND	N1	PPI1SYNC1
C2	ADDR25	E10	VDDINT	H2	GND	K10	GND	N2	PPI1D10
C3	PPI0CLK	E11	GND	H3	GND	K11	VDDEXT	N3	PPI1D7
C4	ADDR20	E12	VDDINT	H4	VDDINT	K12	GND	N4	PPI1D5
C5	ADDR16	E13	DATA06	H5	VDDINT	K13	GND	N5	PF0
C6	ADDR13	E14	DATA13	H6	GND	K14	DATA26	N6	PF04
C7	$\overline{\text{AMS2}}$	E15	DATA09	H7	GND	K15	DATA25	N7	PF09
C8	$\overline{\text{ARE}}$	E16	DATA12	H8	GND	K16	DATA27	N8	PF12

Table 37. 256-Ball CSP_BGA (12 mm × 12 mm) Ball Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
N09	TDO	P05	GND	R01	PPI1D7	R13	TX/PF26	T09	TCK
N10	BMODE1	P06	PF5	R02	PPI1D6	R14	TSCLK1	T10	TMS
N11	MOSI	P07	PF11	R03	PPI1D2	R15	DT1PRI	T11	SLEEP
N12	GND	P08	PF15	R04	PPI1D0	R16	RFS0	T12	VDDEXT
N13	RFS1	P09	GND	R05	PF4	T01	VDDEXT	T13	RX/PF27
N14	GND	P10	$\overline{\text{TRST}}$	R06	PF8	T02	PPI1D4	T14	DR1SEC
N15	DT0SEC	P11	NMI0	R07	PF10	T03	VDDEXT	T15	DT1SEC
N16	TSCLK0	P12	GND	R08	PF14	T04	PF2	T16	VDDEXT
P01	PPI1D8	P13	RSCLK1	R09	NMI1	T05	PF6		
P02	GND	P14	TFS1	R10	TDI	T06	VDDEXT		
P03	PPI1D5	P15	RSCLK0	R11	$\overline{\text{EMU}}$	T07	PF12		
P04	PF0	P16	DR0SEC	R12	MISO	T08	VDDEXT		

Figure 52 lists the top view of the 297-Ball PBGA ball configuration. Figure 53 lists the bottom view.

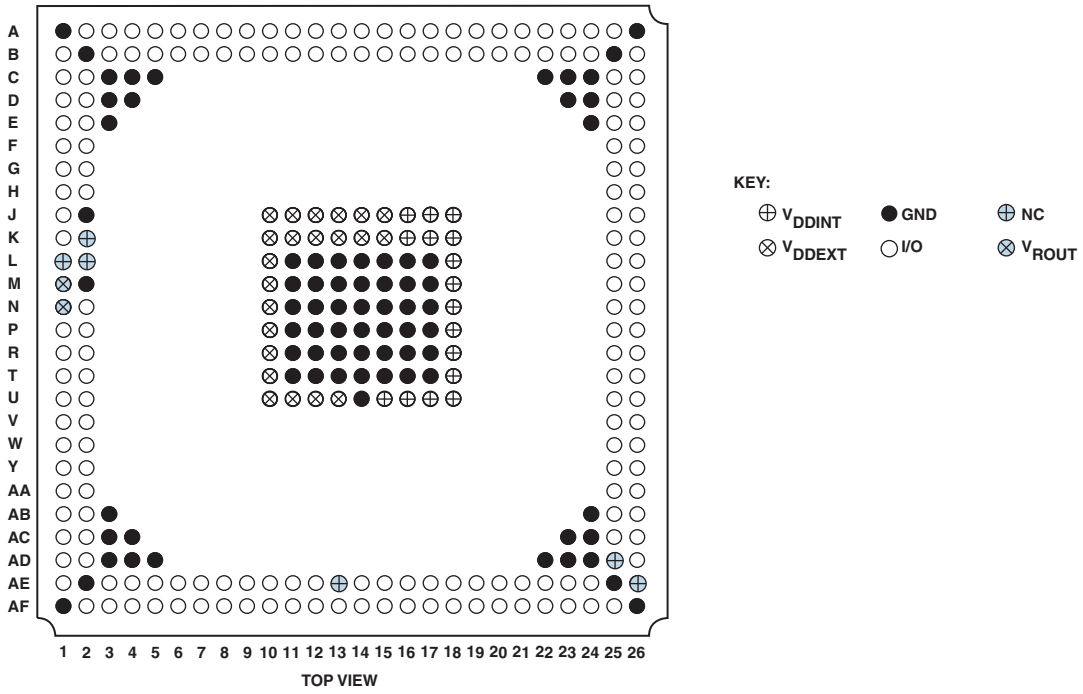


Figure 52. 297-Ball PBGA Ball Configuration (Top View)

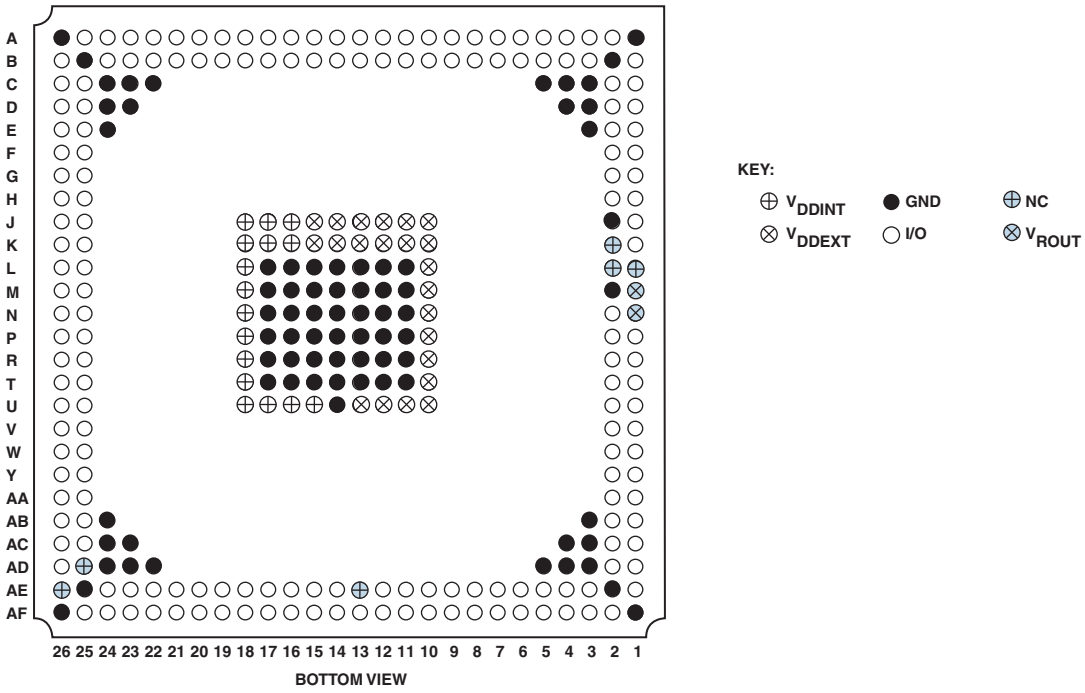
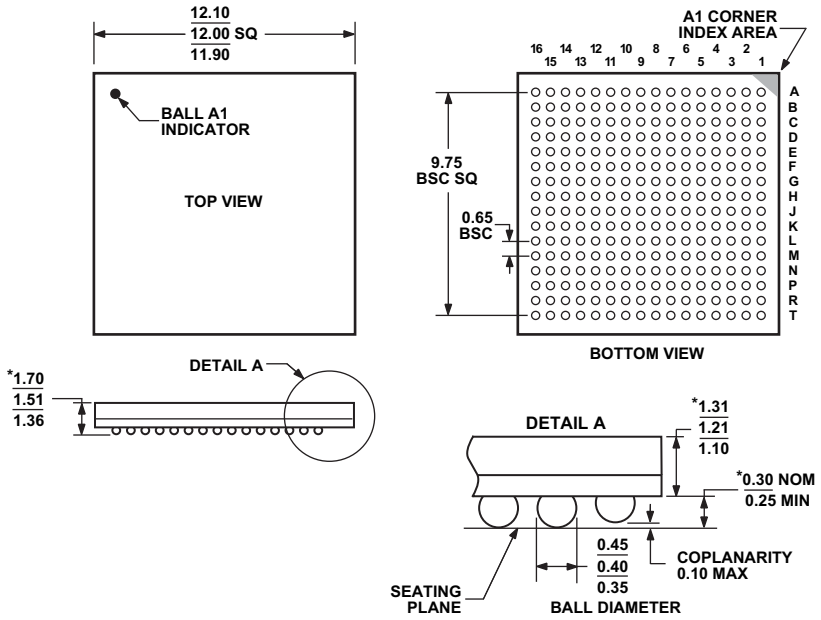
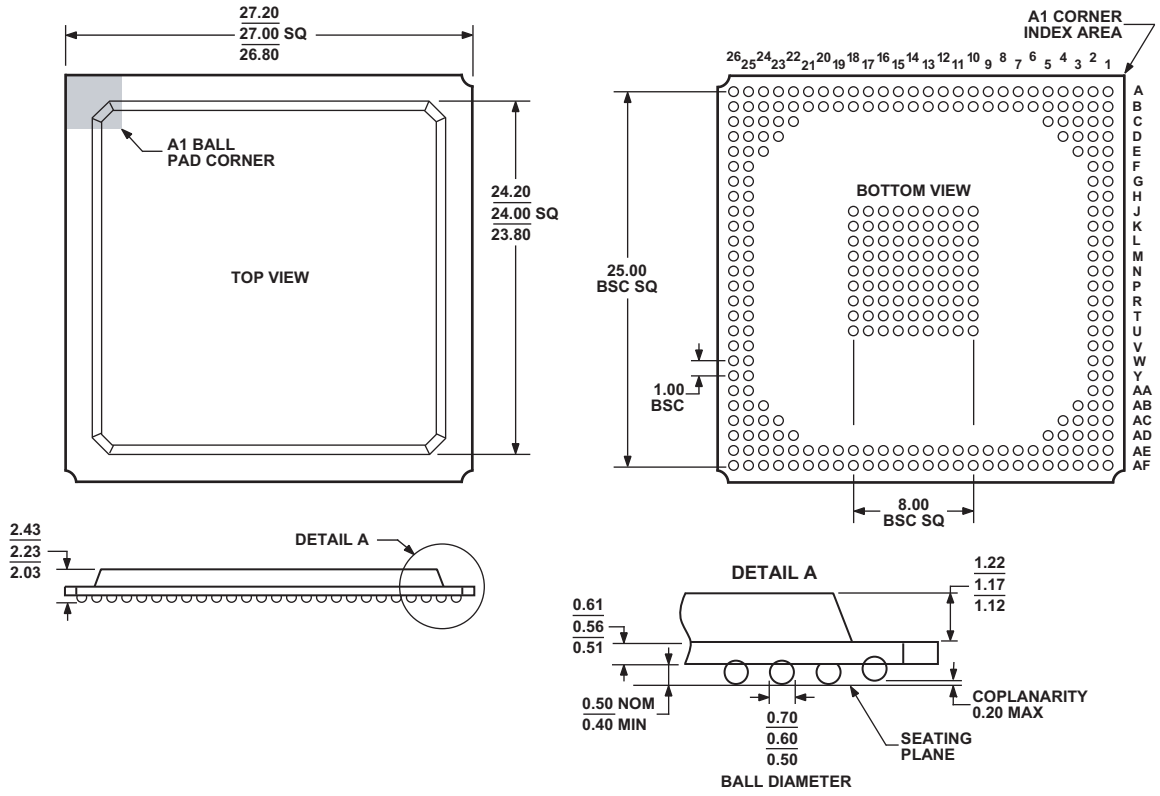


Figure 53. 297-Ball PBGA Ball Configuration (Bottom View)



*COMPLIANT TO JEDEC STANDARDS MO-225 WITH EXCEPTION TO DIMENSIONS INDICATED BY AN ASTERISK.

Figure 55. 256-Ball Chip Scale Package Ball Grid Array (CSP_BGA) (BC-256-1)



COMPLIANT TO JEDEC STANDARDS MS-034-AAL-1

Figure 56. 297-Ball Plastic Ball Grid Array (PBGA) (B-297)

SURFACE-MOUNT DESIGN

Table 41 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Table 41. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
256-Ball CSP_BGA (BC-256-1)	Solder Mask Defined	0.30 mm diameter	0.43 mm diameter
256-Ball CSP_BGA (BC-256-4)	Solder Mask Defined	0.43 mm diameter	0.55 mm diameter
297-Ball PBGA (B-297)	Solder Mask Defined	0.43 mm diameter	0.58 mm diameter

AUTOMOTIVE PRODUCTS

Some ADSP-BF561 models are available for automotive applications with controlled manufacturing. Note that these special models may have specifications that differ from the general release models.

The automotive grade products shown in Table 42 are available for use in automotive applications. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

Table 42. Automotive Products

Product Family[1]	Temperature Range[2]	Speed Grade (Max)[3]	Package Description	Package Option
ADBF561WBBZ5xx	–40°C to +85°C	533 MHz	297-Ball PBGA	B-297
ADBF561WBBCZ5xx	–40°C to +85°C	533 MHz	256-Ball CSP_BGA	BC-256-4

[1] xx denotes silicon revision.
[2] Referenced temperature is ambient temperature.
[3] The internal voltage regulation feature is not available. External voltage regulation is required to ensure correct operation.

ORDERING GUIDE

Model	Temperature Range[1]	Speed Grade (Max)	Package Description	Package Option
ADSP-BF561SKBCZ-6V[2]	0°C to +70°C	600 MHz	256-Ball CSP_BGA	BC-256-1
ADSP-BF561SKBCZ-5V[2]	0°C to +70°C	533 MHz	256-Ball CSP_BGA	BC-256-1
ADSP-BF561SKBCZ500[2]	0°C to +70°C	500 MHz	256-Ball CSP_BGA	BC-256-1
ADSP-BF561SKB500	0°C to +70°C	500 MHz	297-Ball PBGA	B-297
ADSP-BF561SKB600	0°C to +70°C	600 MHz	297-Ball PBGA	B-297
ADSP-BF561SKBZ500[2]	0°C to +70°C	500 MHz	297-Ball PBGA	B-297
ADSP-BF561SKBZ600[2]	0°C to +70°C	600 MHz	297-Ball PBGA	B-297
ADSP-BF561SBB600	–40°C to +85°C	600 MHz	297-Ball PBGA	B-297
ADSP-BF561SBB500	–40°C to +85°C	500 MHz	297-Ball PBGA	B-297
ADSP-BF561SBBZ600[2]	–40°C to +85°C	600 MHz	297-Ball PBGA	B-297
ADSP-BF561SBBZ500[2]	–40°C to +85°C	500 MHz	297-Ball PBGA	B-297
ADSP-BF561SKBCZ-6A[2]	0°C to +70°C	600 MHz	256-Ball CSP_BGA	BC-256-4
ADSP-BF561SKBCZ-5A[2]	0°C to +70°C	500 MHz	256-Ball CSP_BGA	BC-256-4
ADSP-BF561SBBCZ-5A[2]	–40°C to +85°C	500 MHz	256-Ball CSP_BGA	BC-256-4

[1] Referenced temperature is ambient temperature.
[2] Z = RoHS compliant part.

D04696-0-9/09(E)