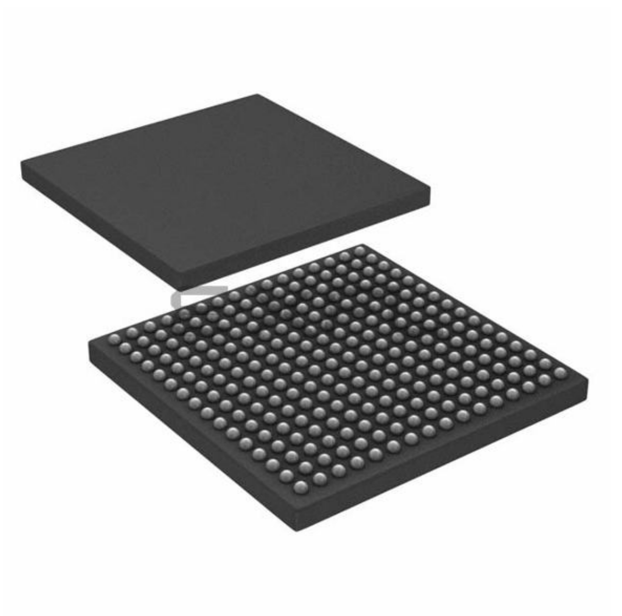

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	533MHz
Non-Volatile Memory	External
On-Chip RAM	328kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.25V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LFBGA, CSPBGA
Supplier Device Package	256-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf561skbcz-5v

ADSP-BF561* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- Low Cost ICE-1000 and High Performance ICE-2000 USB-based JTAG Emulators
- Multimedia Starter Kit
- The ADSP-BF561 EZ-Kit Lite evaluation hardware provides a low-cost hardware solution for evaluating the ADSP-BF561 Blackfin processor.
- USB-Based Emulator and High Performance USB-Based Emulator

DOCUMENTATION

Application Notes

- AN-813: Interfacing the ADSP-BF533/ADSP-BF561 Blackfin®; Processors to High Speed Parallel ADCs
- EE-120: Interfacing Assembly Language Programs to C
- EE-126: The ABCs of SDRAMemories
- EE-175: Emulator and Evaluation Hardware Troubleshooting Guide for VisualDSP++ Users
- EE-183: Rational Sample Rate Conversion with Blackfin® Processors
- EE-185: Fast Floating-Point Arithmetic Emulation on Blackfin® Processors
- EE-228: Switching Regulator Design Considerations for ADSP-BF533 Blackfin® Processors
- EE-261: Understanding Jitter Requirements of PLL-Based Processors
- EE-269: A Beginner's Guide to Ethernet 802.3
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- EE-323: Implementing Dynamically Loaded Software Modules
- EE-326: Blackfin® Processor and SDRAM Technology
- EE-330: Windows Vista Compatibility in VisualDSP++ 5.0 Development Tools
- EE-332: Cycle Counting and Profiling
- EE-336: Putting ADSP-BF54x Blackfin® Processor Booting into Practice
- EE-339: Using External Switching Regulators with Blackfin® Processors
- EE-340: Connecting SHARC® and Blackfin® Processors over SPI
- EE-356: Emulator and Evaluation Hardware Troubleshooting Guide for CCES Users

Data Sheet

REFERENCE MATERIALS

Customer Case Studies

- Dahua Case Study
- UTAS Medical Equipment Ensures High Quality Patient Care with Help from Analog Devices

Technical Articles

- An Efficient Asynchronous Sampling-rate Conversion Algorithm for Multi-channel Audio Applications
- Blackfin Processor Targets Digital Media Open Source Applications
- Blackfin Processor's Parallel Peripheral Interface Simplifies LCD Connection in Portable Multimedia
- Designing IPTV Set-top Boxes Without Getting Boxed In
- Enhance Processor Performance in Open-Source Applications
- High Performance DSPs for Portable Applications
- Is it Really Possible to Play DVD Quality Media While Executing Linux Applications?
- Understanding Advanced Processor Features Promotes Efficient Coding
- Video Filtering Considerations for Media Processors

White Papers

- A BDTI Analysis of the Analog Devices ADSP-BF5xx
- Blackfin Car Telematics Platform Brings Low Cost Telematics to the Mass Market
- Device-Based Social Networking
- LabVIEW 1000m Below the Waves: Synchronized Sampling of Autonomous Units Through Sound
- Secure, Field Upgradeable OS Architecture for Blackfin
- Security Without Compromise
- Unifying Microarchitecture for Embedded Media Processing

DESIGN RESOURCES

- ADSP-BF561 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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writing the appropriate values into the Interrupt Assignment Registers (SIC_IAR7–0). Table 2 describes the inputs into the SIC and the default mappings into the CEC.

Table 2. System Interrupt Controller (SIC)

Peripheral Interrupt Event	Default Mapping
PLL Wakeup	IVG7
DMA1 Error (Generic)	IVG7
DMA2 Error (Generic)	IVG7
IMDMA Error	IVG7
PPI0 Error	IVG7
PPI1 Error	IVG7
SPORT0 Error	IVG7
SPORT1 Error	IVG7
SPI Error	IVG7
UART Error	IVG7
Reserved	IVG7
DMA1 Channel 0 Interrupt (PPI0)	IVG8
DMA1 Channel 1 Interrupt (PPI1)	IVG8
DMA1 Channel 2 Interrupt	IVG8
DMA1 Channel 3 Interrupt	IVG8
DMA1 Channel 4 Interrupt	IVG8
DMA1 Channel 5 Interrupt	IVG8
DMA1 Channel 6 Interrupt	IVG8
DMA1 Channel 7 Interrupt	IVG8
DMA1 Channel 8 Interrupt	IVG8
DMA1 Channel 9 Interrupt	IVG8
DMA1 Channel 10 Interrupt	IVG8
DMA1 Channel 11 Interrupt	IVG8
DMA2 Channel 0 Interrupt (SPORT0 Rx)	IVG9
DMA2 Channel 1 Interrupt (SPORT0 Tx)	IVG9
DMA2 Channel 2 Interrupt (SPORT1 Rx)	IVG9
DMA2 Channel 3 Interrupt (SPORT1 Tx)	IVG9
DMA2 Channel 4 Interrupt (SPI)	IVG9
DMA2 Channel 5 Interrupt (UART Rx)	IVG9
DMA2 Channel 6 Interrupt (UART Tx)	IVG9
DMA2 Channel 7 Interrupt	IVG9
DMA2 Channel 8 Interrupt	IVG9
DMA2 Channel 9 Interrupt	IVG9
DMA2 Channel 10 Interrupt	IVG9
DMA2 Channel 11 Interrupt	IVG9
Timer0 Interrupt	IVG10
Timer1 Interrupt	IVG10
Timer2 Interrupt	IVG10
Timer3 Interrupt	IVG10
Timer4 Interrupt	IVG10
Timer5 Interrupt	IVG10
Timer6 Interrupt	IVG10
Timer7 Interrupt	IVG10
Timer8 Interrupt	IVG10
Timer9 Interrupt	IVG10
Timer10 Interrupt	IVG10
Timer11 Interrupt	IVG10
Programmable Flags 15–0 Interrupt A	IVG11
Programmable Flags 15–0 Interrupt B	IVG11
Programmable Flags 31–16 Interrupt A	IVG11
Programmable Flags 31–16 Interrupt B	IVG11
Programmable Flags 47–32 Interrupt A	IVG11
Programmable Flags 47–32 Interrupt B	IVG11
DMA1 Channel 12/13 Interrupt (Memory DMA/Stream 0)	IVG8
DMA1 Channel 14/15 Interrupt (Memory DMA/Stream 1)	IVG8
DMA2 Channel 12/13 Interrupt (Memory DMA/Stream 0)	IVG9
DMA2 Channel 14/15 Interrupt (Memory DMA/Stream 1)	IVG9
IMDMA Stream 0 Interrupt	IVG12
IMDMA Stream 1 Interrupt	IVG12
Watchdog Timer Interrupt	IVG13
Reserved	IVG7
Reserved	IVG7
Supplemental Interrupt 0	IVG7
Supplemental Interrupt 1	IVG7

Event Control

The ADSP-BF561 provides the user with a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each of the registers is 16 bits wide, while each bit represents a particular event class.

- CEC Interrupt Latch Register (ILAT) – The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but may also be written to clear (cancel) latched events. This register may be read while in supervisor mode and may only be written while in supervisor mode when the corresponding IMASK bit is cleared.
- CEC Interrupt Mask Register (IMASK) – The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and will be processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, thereby preventing the processor from servicing the event

even though the event may be latched in the ILAT register. This register may be read from or written to while in supervisor mode.

Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.

- CEC Interrupt Pending Register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but may be read while in supervisor mode.

The SIC allows further control of event processing by providing six 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 2.

- SIC Interrupt Mask Registers (SIC_IMASKx) – These registers control the masking and unmasking of each peripheral interrupt event. When a bit is set in these registers, that peripheral event is unmasked and will be processed by the system when asserted. A cleared bit in these registers masks the peripheral event, thereby preventing the processor from servicing the event.
- SIC Interrupt Status Registers (SIC_ISRx) – As multiple peripherals can be mapped to a single event, these registers allow the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt; a cleared bit indicates the peripheral is not asserting the event.
- SIC Interrupt Wakeup Enable Registers (SIC_IWRx) – By enabling the corresponding bit in these registers, each peripheral can be configured to wake up the processor, should the processor be in a powered-down mode when the event is generated.

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC will recognize and queue the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the mode of the processor.

DMA CONTROLLERS

The ADSP-BF561 has two independent DMA controllers that support automated data transfers with minimal overhead for the DSP cores. DMA transfers can occur between the ADSP-BF561 internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the SPORTs, SPI port, UART, and PPIs. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The ADSP-BF561 DMA controllers support both 1-dimensional (1-D) and 2-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ± 32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the ADSP-BF561 DMA controllers include:

- A single linear buffer that stops upon completion.
- A circular autorefreshing buffer that interrupts on each full or fractionally full buffer.
- 1-D or 2-D DMA using a linked list of descriptors.
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page.

In addition to the dedicated peripheral DMA channels, each DMA Controller has four memory DMA channels provided for transfers between the various memories of the ADSP-BF561 system. These enable transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

Further, the ADSP-BF561 has a four channel Internal Memory DMA (IMDMA) Controller. The IMDMA Controller allows data transfers between any of the internal L1 and L2 memories.

WATCHDOG TIMER

Each ADSP-BF561 core includes a 32-bit timer, which can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state, via generation of a hardware reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the timer control register, which is set only upon a watchdog generated reset.

The timer is clocked by the system clock (SCLK) at a maximum frequency of f_{SCLK}.

TIMERS

There are 14 programmable timer units in the ADSP-BF561.

Each of the 12 general-purpose timer units can be independently programmed as a Pulse Width Modulator (PWM), internally or externally clocked timer, or pulse width counter. The general-purpose timer units can be used in conjunction with the UART to measure the width of the pulses in the data stream to provide an autobaud detect function for a serial channel. The general-purpose timers can generate interrupts to the processor core providing periodic events for synchronization, either to the processor clock or to a count of external signals.

In addition to the 12 general-purpose programmable timers, another timer is also provided for each core. These extra timers are clocked by the internal processor clock (CCLK) and are typically used as a system tick clock for generation of operating system periodic interrupts.

SERIAL PORTS (SPORTs)

The ADSP-BF561 incorporates two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other DSP components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length – Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most significant bit first or least significant bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The DSP can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1,024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

An additional 250 mV of SPORT input hysteresis can be enabled by setting Bit 15 of the PLL_CTL register. When this bit is set, all SPORT input pins have the increased hysteresis.

SERIAL PERIPHERAL INTERFACE (SPI) PORT

The ADSP-BF561 processor has an SPI-compatible port that enables the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (master output-slave input, MOSI, and master input-slave output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin ($\overline{\text{SPISS}}$) lets other SPI devices select the processor, and seven SPI chip select output pins ($\overline{\text{SPISEL7–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured programmable flag pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface which supports both master/slave modes and multimaster environments.

The baud rate and clock phase/polarities for the SPI port are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI DMA controller can only service unidirectional accesses at any given time.

The SPI port clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

Where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORT

The ADSP-BF561 processor provides a full-duplex universal asynchronous receiver/transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for 5 data bits to 8 data bits, 1 stop bit or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

regulator for the processor can be shut off by writing b#00 to the FREQ bits of the VR_CTL register. This disables both CCLK and SCLK. Furthermore, it sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the lowest static power dissipation. Any critical information stored internally (memory contents, register contents, etc.) must be written to a nonvolatile storage device prior to removing power if the processor state is to be preserved. Since V_{DDEXT} is still supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to have power still applied without drawing unwanted current. The internal supply regulator can be woken up by asserting the $\overline{\text{RESET}}$ pin.

Power Savings

As shown in Table 4, the ADSP-BF561 supports two different power domains. The use of multiple power domains maximizes flexibility, while maintaining compliance with industry standards and conventions. By isolating the internal logic of the ADSP-BF561 into its own power domain, separate from the I/O, the processor can take advantage of Dynamic Power Management, without affecting the I/O devices. There are no sequencing requirements for the various power domains.

Table 4. ADSP-BF561 Power Domains

Power Domain	V_{DD} Range
All internal logic	V_{DDINT}
I/O	V_{DDEXT}

The power dissipated by a processor is largely a function of the clock frequency of the processor and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic.

The dynamic power management feature of the ADSP-BF561 allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The savings in power dissipation can be modeled using the power savings factor and % power savings calculations.

The power savings factor is calculated as:

$$power\ savings\ factor = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{t_{RED}}{t_{NOM}}\right)$$

where the variables in the equations are:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

t_{NOM} is the duration running at $f_{CCLKNOM}$

t_{RED} is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as:

$$\%\ power\ savings = (1 - power\ savings\ factor) \times 100\%$$

VOLTAGE REGULATION

The ADSP-BF561 processor provides an on-chip voltage regulator that can generate appropriate V_{DDINT} voltage levels from the V_{DDEXT} supply. See Operating Conditions on Page 20 for regulator tolerances and acceptable V_{DDEXT} ranges for specific models.

Figure 4 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power (V_{DDEXT}) supplied. While in the hibernate state, V_{DDEXT} can still be applied, thus eliminating the need for external buffers. The voltage regulator can be activated from this power-down state by asserting $\overline{\text{RESET}}$, which will then initiate a boot sequence. The regulator can also be disabled and bypassed at the user's discretion.

The internal voltage regulation feature is not available on any of the 600 MHz speed grade models or automotive grade models. External voltage regulation is required to ensure correct operation of these parts at 600 MHz.

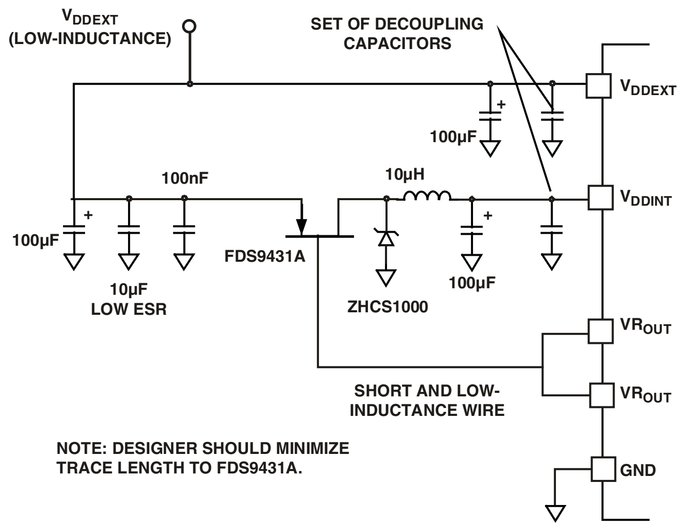
VDDEXT (LOW-INDUCTANCE)
SET OF DECOUPLING CAPACITORS
VDDEXT
100µF
100nF
10µH
VDDINT
100µF
FDS9431A
10µF LOW ESR
ZHCS1000
100µF
VROUT
SHORT AND LOW-INDUCTANCE WIRE
VROUT
NOTE: DESIGNER SHOULD MINIMIZE TRACE LENGTH TO FDS9431A.
GND

Figure 4. Voltage Regulator Circuit

Voltage Regulator Layout Guidelines

Regulator external component placement, board routing, and bypass capacitors all have a significant effect on noise injected into the other analog circuits on-chip. The VROUT1–0 traces and voltage regulator external components should be considered as noise sources when doing board layout and should not be routed or placed near sensitive circuits or components on the

- All registers, I/O, and memory are mapped into a unified 4G byte memory space providing a simplified programming model.
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data types; and separate user and kernel stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded as 16-bits.

DEVELOPMENT TOOLS

The ADSP-BF561 is supported with a complete set of CROSSCORE®[†] software and hardware development tools, including Analog Devices emulators and the VisualDSP++®[‡] development environment. The same emulator hardware that supports other Analog Devices processors also fully emulates the ADSP-BF561.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler that is based on an algebraic syntax, an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ runtime library that includes DSP and mathematical functions. A key point for these tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to Blackfin assembly. The Blackfin processor has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to nonintrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information).
- Insert breakpoints.
- Set conditional breakpoints on registers, memory, and stacks.
- Trace instruction execution.
- Perform linear or statistical profiling of program execution.
- Fill, dump, and graphically plot the contents of memory.
- Perform source level debugging.
- Create custom debugger windows.

The VisualDSP++ IDE lets programmers define and manage software development. Its dialog boxes and property pages let programmers configure and manage all development tools, including color syntax highlighting in the VisualDSP++ editor. These capabilities permit programmers to:

- Control how the development tools process inputs and generate outputs.
- Maintain a one-to-one correspondence with the tool's command line switches.

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of embedded, real-time programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, pre-emptive, cooperative, and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used with standard command line tools. When the VDK is used, the development environment assists the developer with many error prone tasks and assists in managing system resources, automating the generation of various VDK-based objects, and visualizing the system state when debugging an application that uses the VDK.

The Expert Linker can be used to visually manipulate the placement of code and data in the embedded system. Memory utilization can be viewed in a color-coded graphical form. Code and data can be easily moved to different areas of the processor or external memory with the drag of the mouse. Runtime stack and heap usage can be examined. The Expert Linker is fully compatible with existing Linker Definition File (LDF), allowing the developer to move between the graphical and textual environments.

Analog Devices emulators use the IEEE 1149.1 JTAG test access port of the ADSP-BF561 to monitor and control the target board processor during emulation. The emulator provides full-speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect the loading or timing of the target system.

[†] CROSSCORE is a registered trademark of Analog Devices, Inc.
[‡] VisualDSP++ is a registered trademark of Analog Devices, Inc.

TIMING SPECIFICATIONS

Clock and Reset Timing

Table 16 and Figure 8 describe clock and reset operations. Per Absolute Maximum Ratings on Page 22, combinations of CLKIN and clock multipliers must not result in core/system clocks exceeding the maximum limits allowed for the processor, including system clock restrictions related to supply voltage.

Table 16. Clock and Normal Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN (to PLL) Period[1, 2, 3]	25.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse	10.0		ns
t_{CKINH}	CLKIN High Pulse	10.0		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[4]	$11 \times t_{CKIN}$		ns

[1] If DF bit in PLL_CTL register is set t_{CLKIN} is divided by two before going to PLL, then the t_{CLKIN} maximum period is 50 ns and the t_{CLKIN} minimum period is 12.5 ns.
[2] Applies to PLL bypass mode and PLL nonbypass mode.
[3] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 9 on Page 20 through Table 12 on Page 21.
[4] Applies after power-up sequence is complete. See Table 17 and Figure 9 for power-up reset timing.

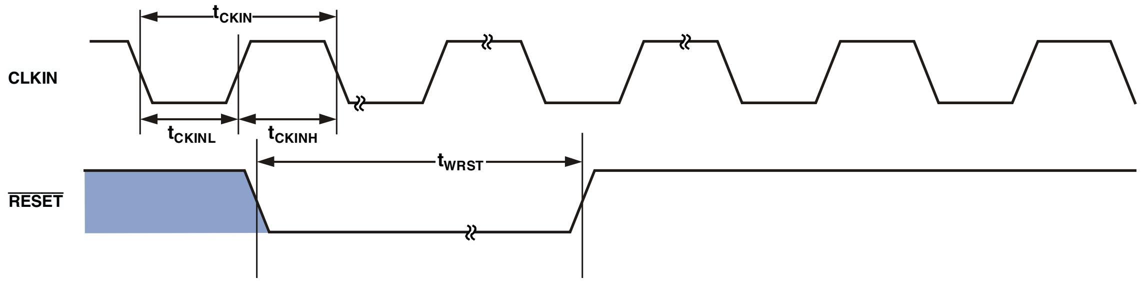

Figure 8. Clock and Normal Reset Timing

Table 17. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted after the V_{DDINT}, V_{DDEXT}, and CLKIN Pins are Stable and Within Specification	$3500 \times t_{CKIN}$		µs

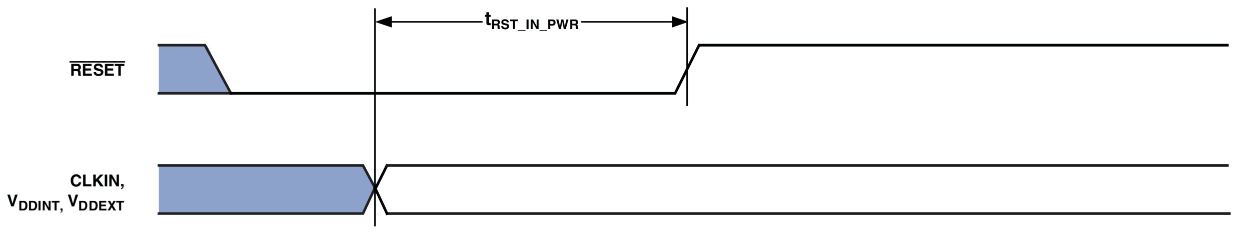

Figure 9. Power-Up Reset Timing

Asynchronous Memory Read Cycle Timing

Table 18. Asynchronous Memory Read Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA31–0 Setup Before CLKOUT	2.1		ns
t_{HDAT}	DATA31–0 Hold After CLKOUT	0.8		ns
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins include $\overline{\text{AMS3–0}}$, $\overline{\text{ABE3–0}}$, ADDR25–2, $\overline{\text{AOE}}$, $\overline{\text{ARE}}$.

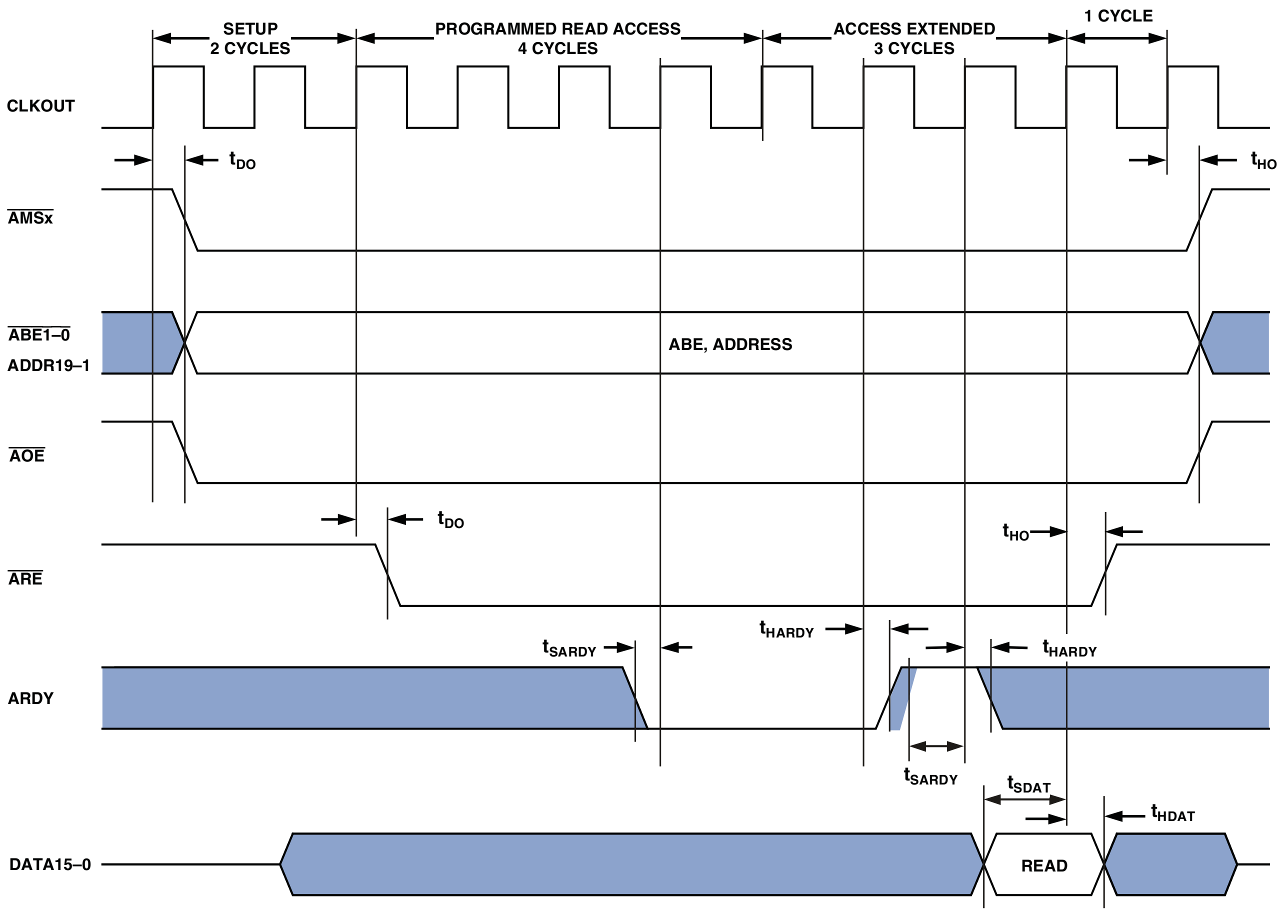

Figure 10. Asynchronous Memory Read Cycle Timing

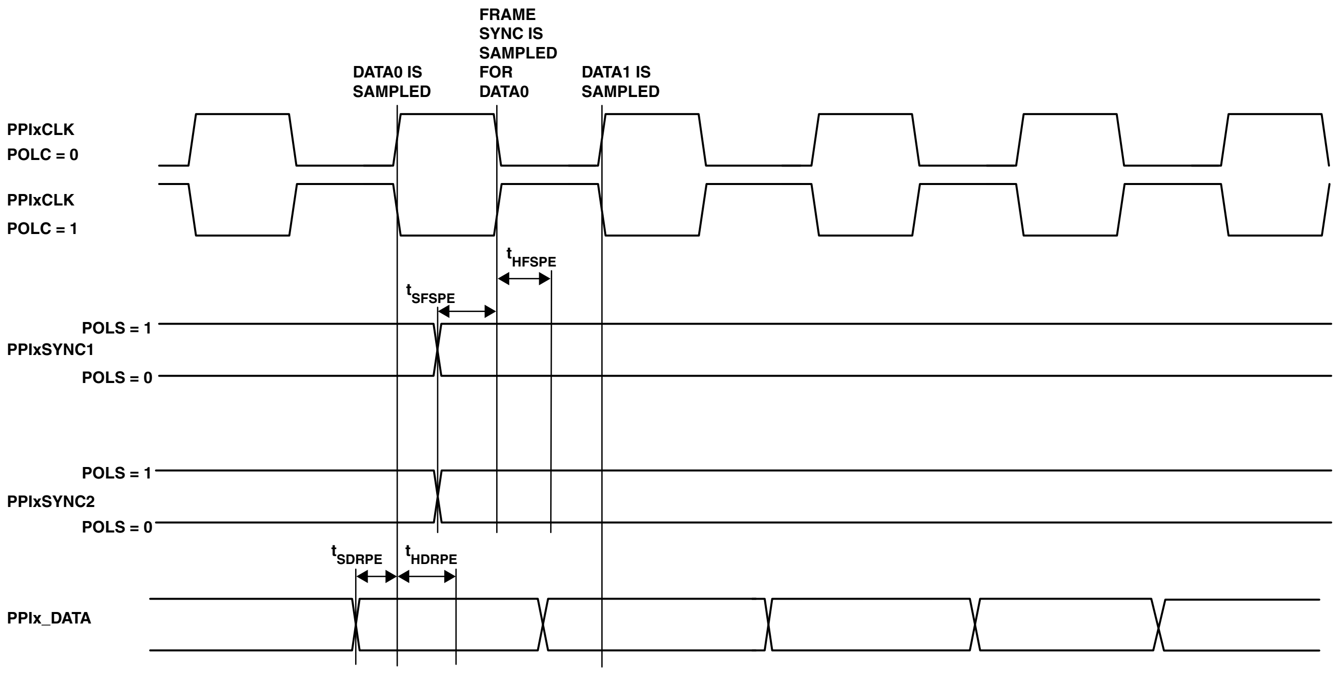

Figure 15. PPI GP Rx Mode with External Frame Sync Timing (Default)

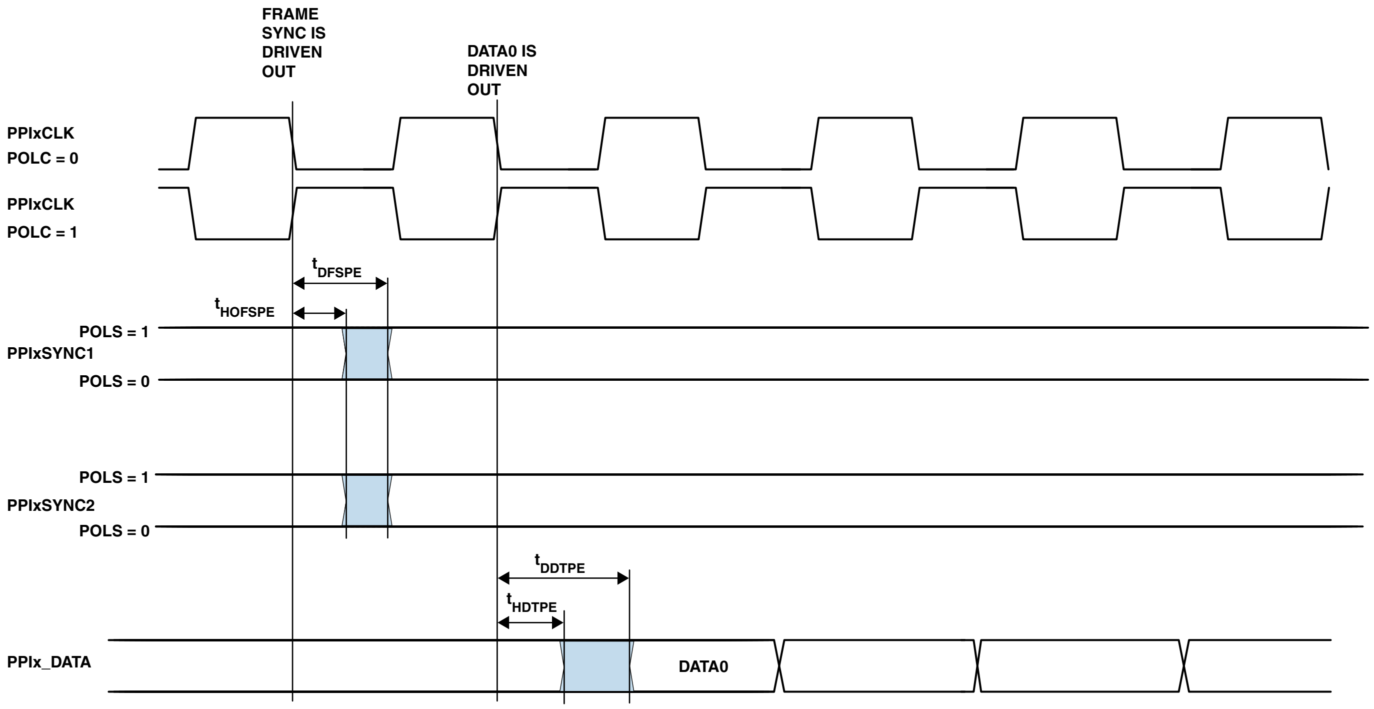

Figure 16. PPI GP Tx Mode with Internal Frame Sync Timing (Default)

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 28 and Figure 24 describe SPI port slave operations.

Table 28. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	8	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0	8	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)	0	10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0	10	ns

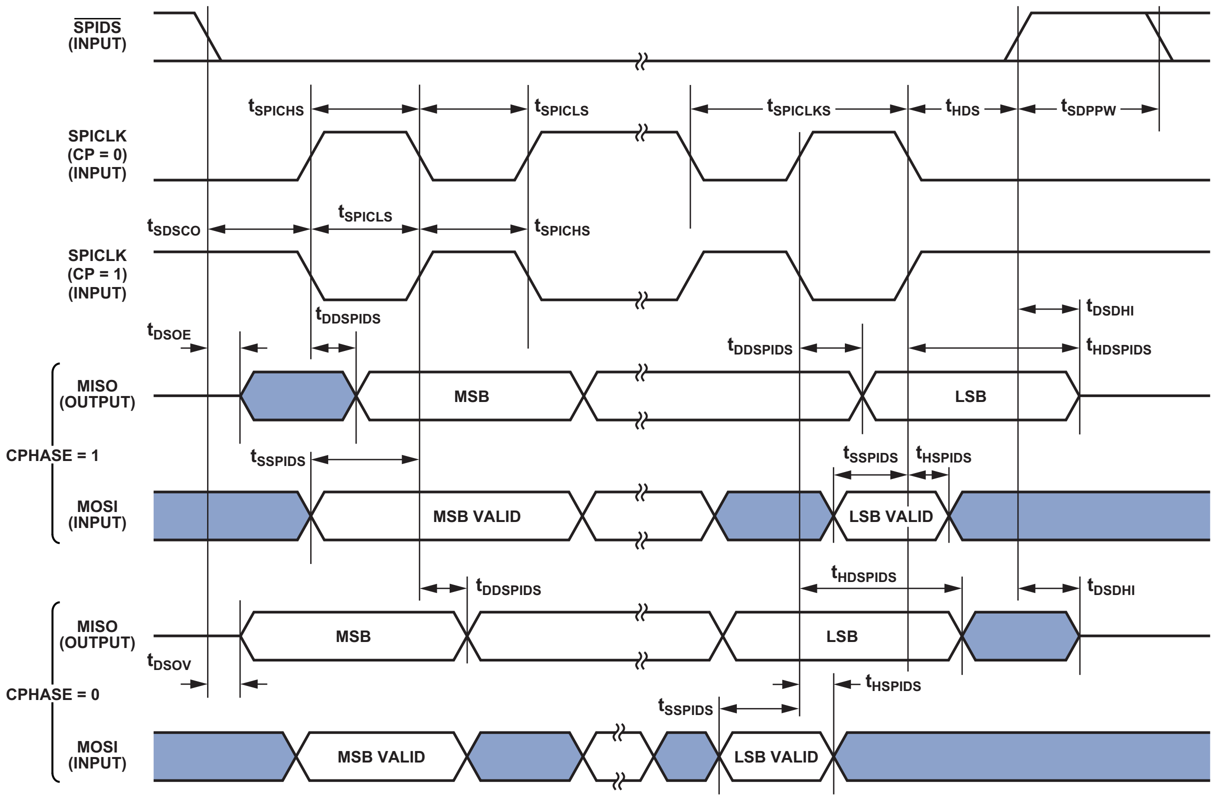

Figure 24. Serial Peripheral Interface (SPI) Port—Slave Timing

OUTPUT DRIVE CURRENTS

Figure 29 through Figure 36 on Page 42 show typical current voltage characteristics for the output drivers of the ADSP-BF561 processor. The curves represent the current drive capability of the output drivers as a function of output voltage. Refer to Table 8 on Page 17 to identify the driver type for a pin.

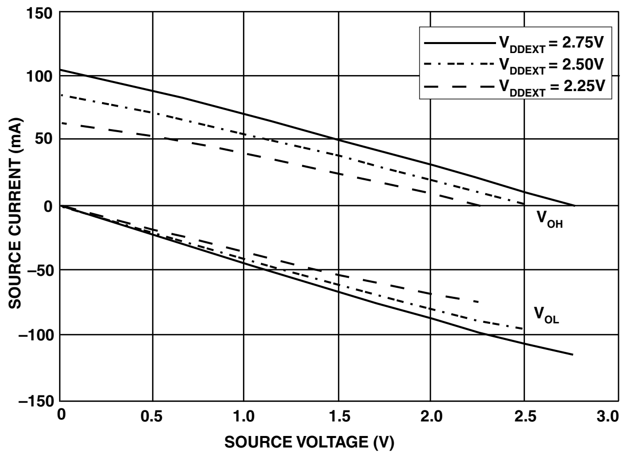

Figure 29. Drive Current A (Low V_{DDEXT})

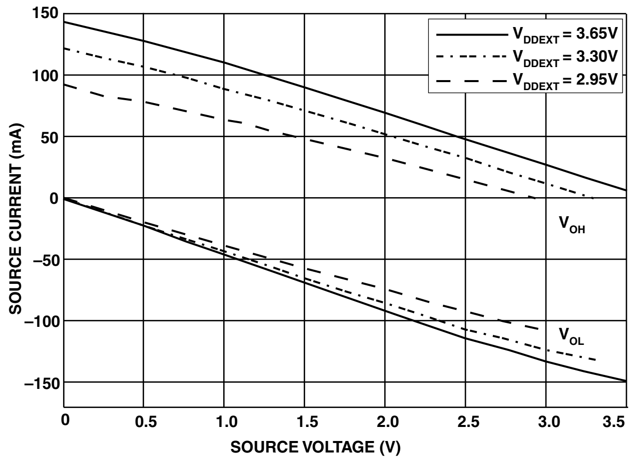

Figure 30. Drive Current A (High V_{DDEXT})

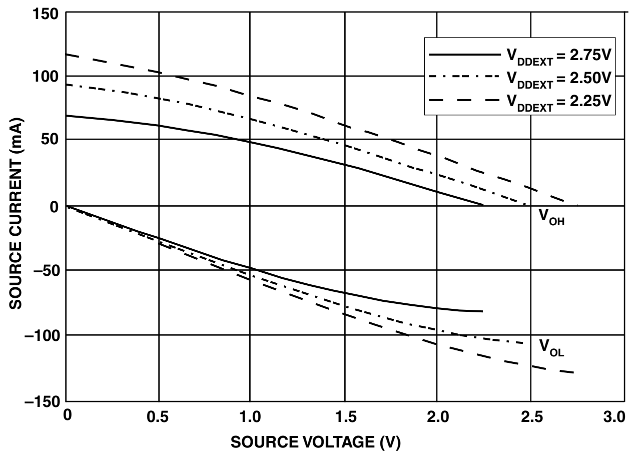

Figure 31. Drive Current B (Low V_{DDEXT})

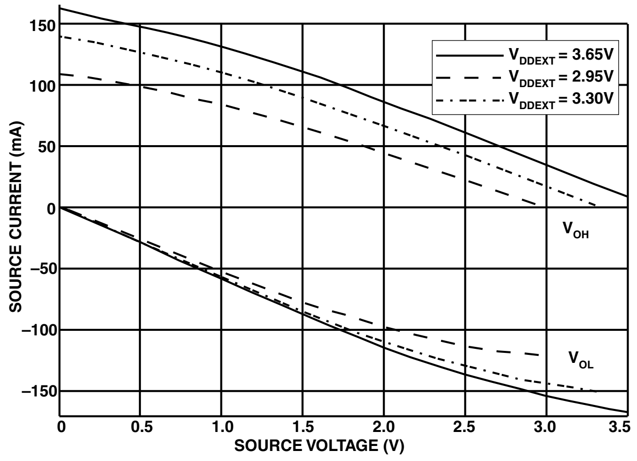

Figure 32. Drive Current B (High V_{DDEXT})

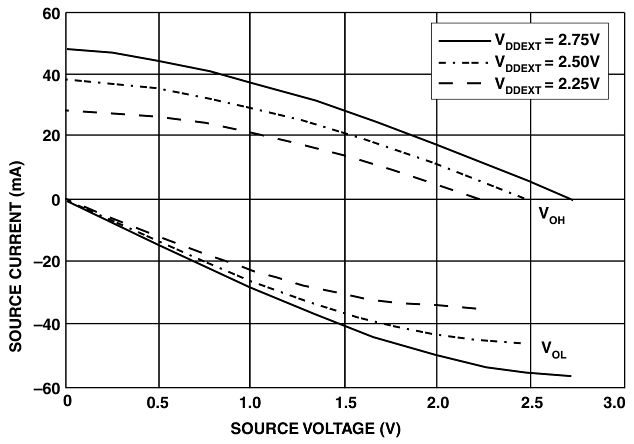

Figure 33. Drive Current C (Low V_{DDEXT})

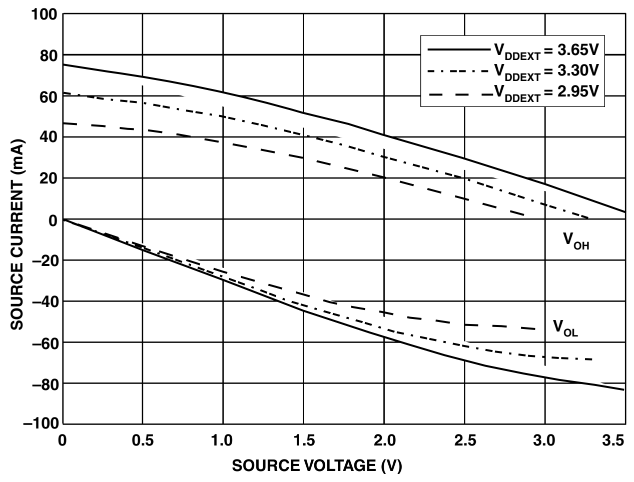

Figure 34. Drive Current C (High V_{DDEXT})

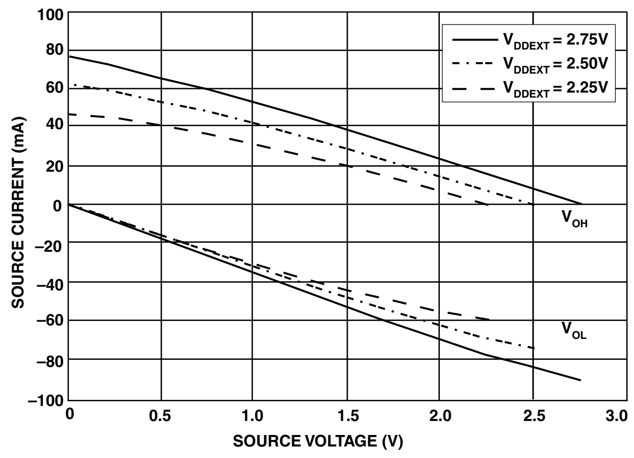

Figure 35. Drive Current D (Low V_{DDEXT})

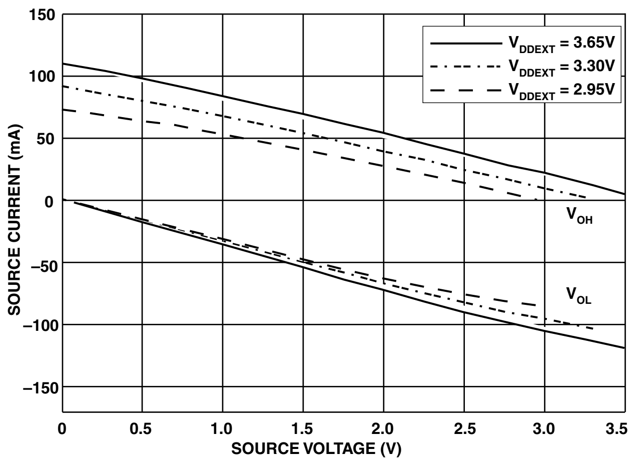

Figure 36. Drive Current D (High V_{DDEXT})

POWER DISSIPATION

Many operating conditions can affect power dissipation. System designers should refer to *Estimating Power for ADSP-BF561 Blackfin Processors (EE-293)* on the Analog Devices website (www.analog.com)—use site search on "EE-293." This document provides detailed information for optimizing your design for lowest power.

See the *ADSP-BF561 Blackfin Processor Hardware Reference Manual* for definitions of the various operating modes and for instructions on how to minimize system power.

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 37 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V.

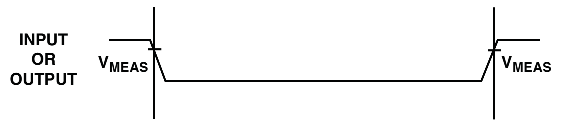

Figure 37. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 38 on Page 43.

The time $t_{ENA\_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches V_{TRIP}(high) or V_{TRIP}(low). V_{TRIP}(high) is 2.0 V and V_{TRIP}(low) is 1.0 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V. Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP}(high) or V_{TRIP}(low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 38 on Page 43.

$$t_{DIS} = t_{DIS\_MEASURED} - t_{DECAY}$$

Table 35. 256-Ball CSP_BGA (17 mm × 17 mm) Ball Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
N9	GND	P5	PF01	R1	PPI1D12	R13	RSCLK1	T9	TDO
N10	BMODE1	P6	PF06	R2	PPI1D11	R14	TSCLK1	T10	TDI
N11	BMODE0	P7	PF08	R3	PPI1D4	R15	NC	T11	$\overline{\text{EMU}}$
N12	RX	P8	PF15	R4	PPI1D1	R16	TFS0	T12	MISO
N13	DR1SEC	P9	NMI1	R5	PF02	T1	VDDEXT	T13	TX
N14	DT1SEC	P10	TMS	R6	PF07	T2	NC	T14	DR1PRI
N15	RFS0	P11	NMI0	R7	PF11	T3	PPI1D3	T15	DT1PRI
N16	DATA30	P12	SCK	R8	PF14	T4	PPI1D2	T16	VDDEXT
P1	PPI1D13	P13	RFS1	R9	TCK	T5	PF03		
P2	PPI1D8	P14	TFS1	R10	$\overline{\text{TRST}}$	T6	PF05		
P3	PPI1D6	P15	DR0SEC	R11	SLEEP	T7	PF10		
P4	PPI1D0	P16	DT0SEC	R12	MOSI	T8	PF13		

Table 37. 256-Ball CSP_BGA (12 mm × 12 mm) Ball Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
N09	TDO	P05	GND	R01	PPI1D7	R13	TX/PF26	T09	TCK
N10	BMODE1	P06	PF5	R02	PPI1D6	R14	TSCLK1	T10	TMS
N11	MOSI	P07	PF11	R03	PPI1D2	R15	DT1PRI	T11	SLEEP
N12	GND	P08	PF15	R04	PPI1D0	R16	RFS0	T12	VDDEXT
N13	RFS1	P09	GND	R05	PF4	T01	VDDEXT	T13	RX/PF27
N14	GND	P10	$\overline{\text{TRST}}$	R06	PF8	T02	PPI1D4	T14	DR1SEC
N15	DT0SEC	P11	NMI0	R07	PF10	T03	VDDEXT	T15	DT1SEC
N16	TSCLK0	P12	GND	R08	PF14	T04	PF2	T16	VDDEXT
P01	PPI1D8	P13	RSCLK1	R09	NMI1	T05	PF6		
P02	GND	P14	TFS1	R10	TDI	T06	VDDEXT		
P03	PPI1D5	P15	RSCLK0	R11	$\overline{\text{EMU}}$	T07	PF12		
P04	PF0	P16	DR0SEC	R12	MISO	T08	VDDEXT		

Table 38. 256-Ball CSP_BGA (12 mm × 12 mm) Ball Assignment (Alphabetically by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{\text{ABE0}}$	E11	$\overline{\text{BR}}$	B12	DT0SEC	N15	GND	N14
$\overline{\text{ABE1}}$	B13	BYPASS	G04	DT1PRI	R15	GND	P02
$\overline{\text{ABE2}}$	A14	CLKIN	F01	DT1SEC	T15	GND	P05
$\overline{\text{ABE3}}$	A15	DATA0	B16	$\overline{\text{EMU}}$	R11	GND	P09
ADDR02	D13	DATA1	C15	GND	C05	GND	P12
ADDR03	G11	DATA2	E12	GND	C11	MISO	R12
ADDR04	B15	DATA3	C16	GND	C13	MOSI	N11
ADDR05	G10	DATA4	E14	GND	D05	NC	M05
ADDR06	B14	DATA5	D15	GND	D06	NC	M13
ADDR07	C14	DATA6	D16	GND	D08	NMI0	P11
ADDR08	F11	DATA7	E15	GND	D14	NMI1	R09
ADDR09	D07	DATA8	F13	GND	E01	PF0	P04
ADDR10	A06	DATA9	F15	GND	E13	PF1	N05
ADDR11	C06	DATA10	F12	GND	F08	PF2	T04
ADDR12	B05	DATA11	F16	GND	F10	PF3	M06
ADDR13	E06	DATA12	F14	GND	G02	PF4	R05
ADDR14	A05	DATA13	G15	GND	G06	PF5	P06
ADDR15	E05	DATA14	G13	GND	G07	PF6	T05
ADDR16	B04	DATA15	G12	GND	G08	PF7	M07
ADDR17	F06	DATA16	H12	GND	G14	PF8	R06
ADDR18	B03	DATA17	H15	GND	H01	PF9	N06
ADDR19	C04	DATA18	H13	GND	H02	PF10	R07
ADDR20	A03	DATA19	H16	GND	H08	PF11	P07
ADDR21	F05	DATA20	H14	GND	H09	PF12	T07
ADDR22	B02	DATA21	J15	GND	H10	PF13	N08
ADDR23	D04	DATA22	J13	GND	J07	PF14	R08
ADDR24	A02	DATA23	J16	GND	J11	PF15	P08
ADDR25	C03	DATA24	K14	GND	J14	PPI0CLK	C02
$\overline{\text{AMS0}}$	C08	DATA25	K15	GND	K07	PPI0D0	L01
$\overline{\text{AMS1}}$	B07	DATA26	K13	GND	K09	PPI0D1	J05
$\overline{\text{AMS2}}$	E07	DATA27	L15	GND	K10	PPI0D2	J03
$\overline{\text{AMS3}}$	A07	DATA28	K12	GND	L03	PPI0D3	J04
$\overline{\text{AOE}}$	C07	DATA29	L16	GND	L07	PPI0D4	K02
ARDY	D09	DATA30	J12	GND	L09	PPI0D5	H05
$\overline{\text{ARE}}$	B08	DATA31	M15	GND	L11	PPI0D6	K01
$\overline{\text{AWE}}$	A08	DR0PRI	L12	GND	L14	PPI0D7	H04
$\overline{\text{BG}}$	A13	DR0SEC	P16	GND	M04	PPI0D8	K03
$\overline{\text{BGH}}$	C12	DR1PRI	M12	GND	M09	PPI0D9	H03
BMODE0	M10	DR1SEC	T14	GND	N07	PPI0D10	F04
BMODE1	N10	DT0PRI	M16	GND	N12	PPI0D11	E02

Table 39. 297-Ball PBGA Ball Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
P15	GND	U11	VDDEXT	AC04	GND	AE21	RX
P16	GND	U12	VDDEXT	AC23	GND	AE22	RFS1
P17	GND	U13	VDDEXT	AC24	GND	AE23	DR1SEC
P18	VDDINT	U14	GND	AC25	DR0SEC	AE24	TFS1
P25	DATA18	U15	VDDINT	AC26	RFS0	AE25	GND
P26	DATA21	U16	VDDINT	AD01	PPI1D7	AE26	NC
R01	PPI0D5	U17	VDDINT	AD02	PPI1D6	AF01	GND
R02	PPI0D6	U18	VDDINT	AD03	GND	AF02	PPI1D4
R10	VDDEXT	U25	DATA24	AD04	GND	AF03	PPI1D2
R11	GND	U26	DATA27	AD05	GND	AF04	PPI1D0
R12	GND	V01	PPI1SYNC3	AD22	GND	AF05	PF1
R13	GND	V02	PPI0D0	AD23	GND	AF06	PF3
R14	GND	V25	DATA26	AD24	GND	AF07	PF5
R15	GND	V26	DATA29	AD25	NC	AF08	PF7
R16	GND	W01	PPI1SYNC1	AD26	RSCLK0	AF09	PF9
R17	GND	W02	PPI1SYNC2	AE01	PPI1D5	AF10	PF11
R18	VDDINT	W25	DATA28	AE02	GND	AF11	PF13
R25	DATA20	W26	DATA31	AE03	PPI1D3	AF12	PF15
R26	DATA23	Y01	PPI1D15	AE04	PPI1D1	AF13	NMI1
T01	PPI0D3	Y02	PPI1D14	AE05	PF0	AF14	TCK
T02	PPI0D4	Y25	DATA30	AE06	PF2	AF15	TDI
T10	VDDEXT	Y26	DT0PRI	AE07	PF4	AF16	TMS
T11	GND	AA01	PPI1D13	AE08	PF6	AF17	SLEEP
T12	GND	AA02	PPI1D12	AE09	PF8	AF18	NMI0
T13	GND	AA25	DT0SEC	AE10	PF10	AF19	SCK
T14	GND	AA26	TSCLK0	AE11	PF12	AF20	TX
T15	GND	AB01	PPI1D11	AE12	PF14	AF21	RSCLK1
T16	GND	AB02	PPI1D10	AE13	NC	AF22	DR1PRI
T17	GND	AB03	GND	AE14	TDO	AF23	TSCLK1
T18	VDDINT	AB24	GND	AE15	$\overline{\text{TRST}}$	AF24	DT1SEC
T25	DATA22	AB25	TFS0	AE16	$\overline{\text{EMU}}$	AF25	DT1PRI
T26	DATA25	AB26	DR0PRI	AE17	BMODE1	AF26	GND
U01	PPI0D1	AC01	PPI1D9	AE18	BMODE0		
U02	PPI0D2	AC02	PPI1D8	AE19	MISO		
U10	VDDEXT	AC03	GND	AE20	MOSI		

Table 40. 297-Ball PBGA Ball Assignment (Alphabetically by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
$\overline{\text{ABE0}}$	A22	$\overline{\text{BR}}$	B20	DT0SEC	AA25	GND	N15
$\overline{\text{ABE1}}$	B22	BYPASS	H01	DT1PRI	AF25	GND	N16
$\overline{\text{ABE2}}$	A23	CLKIN	J01	DT1SEC	AF24	GND	N17
$\overline{\text{ABE3}}$	B23	DATA0	E25	$\overline{\text{EMU}}$	AE16	GND	P11
ADDR02	D25	DATA1	D26	GND	A01	GND	P12
ADDR03	C26	DATA2	F25	GND	A26	GND	P13
ADDR04	C25	DATA3	E26	GND	B02	GND	P14
ADDR05	B26	DATA4	G25	GND	B25	GND	P15
ADDR06	A25	DATA5	F26	GND	C03	GND	P16
ADDR07	B24	DATA6	H25	GND	C04	GND	P17
ADDR08	A24	DATA7	G26	GND	C05	GND	R11
ADDR09	A10	DATA8	J25	GND	C22	GND	R12
ADDR10	B10	DATA9	H26	GND	C23	GND	R13
ADDR11	A09	DATA10	K25	GND	C24	GND	R14
ADDR12	B09	DATA11	J26	GND	D03	GND	R15
ADDR13	A08	DATA12	L25	GND	D04	GND	R16
ADDR14	B08	DATA13	K26	GND	D23	GND	R17
ADDR15	A07	DATA14	M25	GND	D24	GND	T11
ADDR16	B07	DATA15	L26	GND	E03	GND	T12
ADDR17	A06	DATA16	N25	GND	E24	GND	T13
ADDR18	B06	DATA17	M26	GND	J02	GND	T14
ADDR19	A05	DATA18	P25	GND	L11	GND	T15
ADDR20	B05	DATA19	N26	GND	L12	GND	T16
ADDR21	A04	DATA20	R25	GND	L13	GND	T17
ADDR22	B04	DATA21	P26	GND	L14	GND	U14
ADDR23	A03	DATA22	T25	GND	L15	GND	AB03
ADDR24	B03	DATA23	R26	GND	L16	GND	AB24
ADDR25	A02	DATA24	U25	GND	L17	GND	AC03
$\overline{\text{AMS0}}$	B12	DATA25	T26	GND	M02	GND	AC04
$\overline{\text{AMS1}}$	A12	DATA26	V25	GND	M11	GND	AC23
$\overline{\text{AMS2}}$	B11	DATA27	U26	GND	M12	GND	AC24
$\overline{\text{AMS3}}$	A11	DATA28	W25	GND	M13	GND	AD03
$\overline{\text{AOE}}$	B13	DATA29	V26	GND	M14	GND	AD04
ARDY	B14	DATA30	Y25	GND	M15	GND	AD05
$\overline{\text{ARE}}$	A14	DATA31	W26	GND	M16	GND	AD22
$\overline{\text{AWE}}$	A13	DR0PRI	AB26	GND	M17	GND	AD23
$\overline{\text{BG}}$	B21	DR0SEC	AC25	GND	N11	GND	AD24
$\overline{\text{BGH}}$	A21	DR1PRI	AF22	GND	N12	GND	AE02
BMODE0	AE18	DR1SEC	AE23	GND	N13	GND	AE25
BMODE1	AE17	DT0PRI	Y26	GND	N14	GND	AF01

Figure 52 lists the top view of the 297-Ball PBGA ball configuration. Figure 53 lists the bottom view.

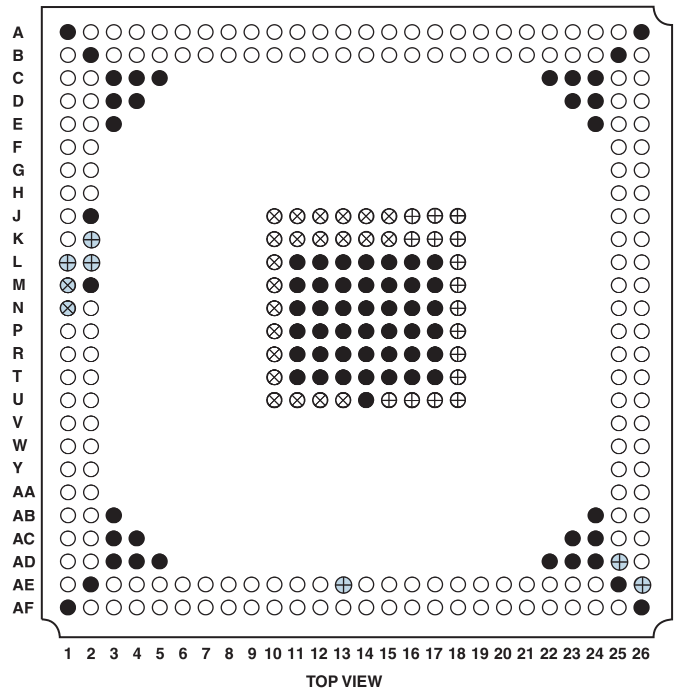

Figure 52. 297-Ball PBGA Ball Configuration (Top View)

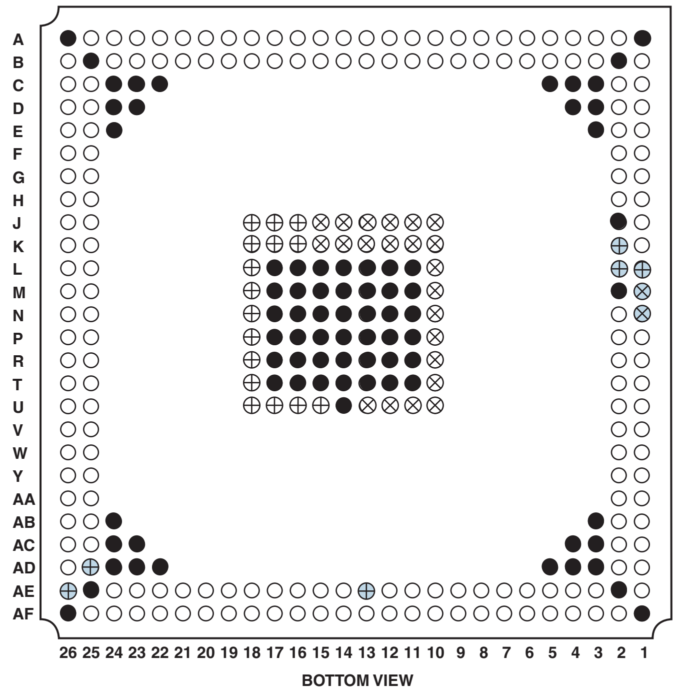

Figure 53. 297-Ball PBGA Ball Configuration (Bottom View)

SURFACE-MOUNT DESIGN

Table 41 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Table 41. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
256-Ball CSP_BGA (BC-256-1)	Solder Mask Defined	0.30 mm diameter	0.43 mm diameter
256-Ball CSP_BGA (BC-256-4)	Solder Mask Defined	0.43 mm diameter	0.55 mm diameter
297-Ball PBGA (B-297)	Solder Mask Defined	0.43 mm diameter	0.58 mm diameter

AUTOMOTIVE PRODUCTS

Some ADSP-BF561 models are available for automotive applications with controlled manufacturing. Note that these special models may have specifications that differ from the general release models.

The automotive grade products shown in Table 42 are available for use in automotive applications. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

Table 42. Automotive Products

Product Family[1]	Temperature Range[2]	Speed Grade (Max)[3]	Package Description	Package Option
ADBF561WBBZ5xx	–40°C to +85°C	533 MHz	297-Ball PBGA	B-297
ADBF561WBBCZ5xx	–40°C to +85°C	533 MHz	256-Ball CSP_BGA	BC-256-4

[1] xx denotes silicon revision.
[2] Referenced temperature is ambient temperature.
[3] The internal voltage regulation feature is not available. External voltage regulation is required to ensure correct operation.

ORDERING GUIDE

Model	Temperature Range[1]	Speed Grade (Max)	Package Description	Package Option
ADSP-BF561SKBCZ-6V[2]	0°C to +70°C	600 MHz	256-Ball CSP_BGA	BC-256-1
ADSP-BF561SKBCZ-5V[2]	0°C to +70°C	533 MHz	256-Ball CSP_BGA	BC-256-1
ADSP-BF561SKBCZ500[2]	0°C to +70°C	500 MHz	256-Ball CSP_BGA	BC-256-1
ADSP-BF561SKB500	0°C to +70°C	500 MHz	297-Ball PBGA	B-297
ADSP-BF561SKB600	0°C to +70°C	600 MHz	297-Ball PBGA	B-297
ADSP-BF561SKBZ500[2]	0°C to +70°C	500 MHz	297-Ball PBGA	B-297
ADSP-BF561SKBZ600[2]	0°C to +70°C	600 MHz	297-Ball PBGA	B-297
ADSP-BF561SBB600	–40°C to +85°C	600 MHz	297-Ball PBGA	B-297
ADSP-BF561SBB500	–40°C to +85°C	500 MHz	297-Ball PBGA	B-297
ADSP-BF561SBBZ600[2]	–40°C to +85°C	600 MHz	297-Ball PBGA	B-297
ADSP-BF561SBBZ500[2]	–40°C to +85°C	500 MHz	297-Ball PBGA	B-297
ADSP-BF561SKBCZ-6A[2]	0°C to +70°C	600 MHz	256-Ball CSP_BGA	BC-256-4
ADSP-BF561SKBCZ-5A[2]	0°C to +70°C	500 MHz	256-Ball CSP_BGA	BC-256-4
ADSP-BF561SBBCZ-5A[2]	–40°C to +85°C	500 MHz	256-Ball CSP_BGA	BC-256-4

[1] Referenced temperature is ambient temperature.
[2] Z = RoHS compliant part.