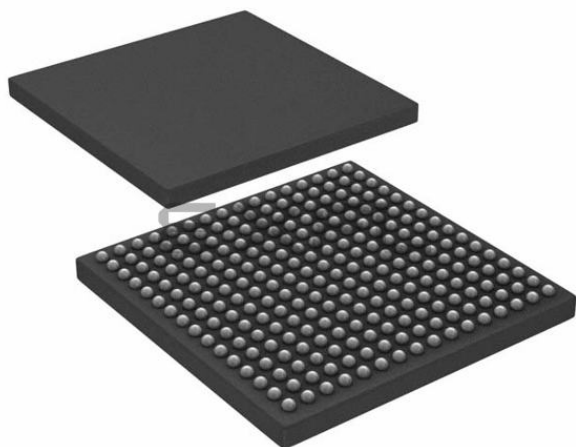




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Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Active
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	500MHz
Non-Volatile Memory	External
On-Chip RAM	328kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.25V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LFBGA, CSPBGA
Supplier Device Package	256-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf561skbcz500

ADSP-BF561* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- Low Cost ICE-1000 and High Performance ICE-2000 USB-based JTAG Emulators
- Multimedia Starter Kit
- The ADSP-BF561 EZ-Kit Lite evaluation hardware provides a low-cost hardware solution for evaluating the ADSP-BF561 Blackfin processor.
- USB-Based Emulator and High Performance USB-Based Emulator

DOCUMENTATION

Application Notes

- AN-813: Interfacing the ADSP-BF533/ADSP-BF561 Blackfin® Processors to High Speed Parallel ADCs
- EE-120: Interfacing Assembly Language Programs to C
- EE-126: The ABCs of SDRAM Memories
- EE-175: Emulator and Evaluation Hardware Troubleshooting Guide for VisualDSP++ Users
- EE-183: Rational Sample Rate Conversion with Blackfin® Processors
- EE-185: Fast Floating-Point Arithmetic Emulation on Blackfin® Processors
- EE-228: Switching Regulator Design Considerations for ADSP-BF533 Blackfin® Processors
- EE-261: Understanding Jitter Requirements of PLL-Based Processors
- EE-269: A Beginner's Guide to Ethernet 802.3
- EE-281: Hardware Design Checklist for the Blackfin® Processors
- EE-289: Implementing FAT32 File Systems on ADSP-BF533 Blackfin® Processors
- EE-293: Estimating Power for ADSP-BF561 Blackfin® Processors
- EE-294: Energy-Aware Programming on Blackfin Processors
- EE-300: Interfacing Blackfin® EZ-KIT Lite® Boards to CMOS Image Sensors
- EE-314: Booting the ADSP-BF561 Blackfin® Processor
- EE-323: Implementing Dynamically Loaded Software Modules
- EE-326: Blackfin® Processor and SDRAM Technology
- EE-330: Windows Vista Compatibility in VisualDSP++ 5.0 Development Tools
- EE-332: Cycle Counting and Profiling
- EE-336: Putting ADSP-BF54x Blackfin® Processor Booting into Practice
- EE-339: Using External Switching Regulators with Blackfin® Processors
- EE-340: Connecting SHARC® and Blackfin® Processors over SPI
- EE-356: Emulator and Evaluation Hardware Troubleshooting Guide for CCES Users

Data Sheet

REFERENCE MATERIALS

Customer Case Studies

- Dahua Case Study
- UTAS Medical Equipment Ensures High Quality Patient Care with Help from Analog Devices

Technical Articles

- An Efficient Asynchronous Sampling-rate Conversion Algorithm for Multi-channel Audio Applications
- Blackfin Processor Targets Digital Media Open Source Applications
- Blackfin Processor's Parallel Peripheral Interface Simplifies LCD Connection in Portable Multimedia
- Designing IPTV Set-top Boxes Without Getting Boxed In
- Enhance Processor Performance in Open-Source Applications
- High Performance DSPs for Portable Applications
- Is it Really Possible to Play DVD Quality Media While Executing Linux Applications?
- Understanding Advanced Processor Features Promotes Efficient Coding
- Video Filtering Considerations for Media Processors

White Papers

- A BDTI Analysis of the Analog Devices ADSP-BF5xx
- Blackfin Car Telematics Platform Brings Low Cost Telematics to the Mass Market
- Device-Based Social Networking

- LabVIEW 1000m Below the Waves: Synchronized Sampling of Autonomous Units Through Sound
- Secure, Field Upgradeable OS Architecture for Blackfin
- Security Without Compromise
- Unifying Microarchitecture for Embedded Media Processing

DESIGN RESOURCES

- ADSP-BF561 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADSP-BF561 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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REVISION HISTORY

9/09—Rev. D to Rev. E

Correct all outstanding document errata.

Revised Figure 5	13
Added 533 MHz operation Table 10	20
Removed reference to 1.8 V operation Table 12	21
Added Table 17 and Figure 9 Power-Up Reset Timing	23
Removed references to T_j from t_{SCLK} parameter Table 20	26
Added new SPORT timing parameters and diagram Table 23	32
Figure 21	33

writing the appropriate values into the Interrupt Assignment Registers (SIC_IAR7–0). Table 2 describes the inputs into the SIC and the default mappings into the CEC.

Table 2. System Interrupt Controller (SIC)

Peripheral Interrupt Event	Default Mapping
PLL Wakeup	IVG7
DMA1 Error (Generic)	IVG7
DMA2 Error (Generic)	IVG7
IMDMA Error	IVG7
PPIO Error	IVG7
PPI1 Error	IVG7
SPORT0 Error	IVG7
SPORT1 Error	IVG7
SPI Error	IVG7
UART Error	IVG7
Reserved	IVG7
DMA1 Channel 0 Interrupt (PPIO)	IVG8
DMA1 Channel 1 Interrupt (PPI1)	IVG8
DMA1 Channel 2 Interrupt	IVG8
DMA1 Channel 3 Interrupt	IVG8
DMA1 Channel 4 Interrupt	IVG8
DMA1 Channel 5 Interrupt	IVG8
DMA1 Channel 6 Interrupt	IVG8
DMA1 Channel 7 Interrupt	IVG8
DMA1 Channel 8 Interrupt	IVG8
DMA1 Channel 9 Interrupt	IVG8
DMA1 Channel 10 Interrupt	IVG8
DMA1 Channel 11 Interrupt	IVG8
DMA2 Channel 0 Interrupt (SPORT0 Rx)	IVG9
DMA2 Channel 1 Interrupt (SPORT0 Tx)	IVG9
DMA2 Channel 2 Interrupt (SPORT1 Rx)	IVG9
DMA2 Channel 3 Interrupt (SPORT1 Tx)	IVG9
DMA2 Channel 4 Interrupt (SPI)	IVG9
DMA2 Channel 5 Interrupt (UART Rx)	IVG9
DMA2 Channel 6 Interrupt (UART Tx)	IVG9
DMA2 Channel 7 Interrupt	IVG9
DMA2 Channel 8 Interrupt	IVG9
DMA2 Channel 9 Interrupt	IVG9
DMA2 Channel 10 Interrupt	IVG9
DMA2 Channel 11 Interrupt	IVG9
Timer0 Interrupt	IVG10
Timer1 Interrupt	IVG10
Timer2 Interrupt	IVG10
Timer3 Interrupt	IVG10
Timer4 Interrupt	IVG10
Timer5 Interrupt	IVG10
Timer6 Interrupt	IVG10

Table 2. System Interrupt Controller (SIC) (Continued)

Peripheral Interrupt Event	Default Mapping
Timer7 Interrupt	IVG10
Timer8 Interrupt	IVG10
Timer9 Interrupt	IVG10
Timer10 Interrupt	IVG10
Timer11 Interrupt	IVG10
Programmable Flags 15–0 Interrupt A	IVG11
Programmable Flags 15–0 Interrupt B	IVG11
Programmable Flags 31–16 Interrupt A	IVG11
Programmable Flags 31–16 Interrupt B	IVG11
Programmable Flags 47–32 Interrupt A	IVG11
Programmable Flags 47–32 Interrupt B	IVG11
DMA1 Channel 12/13 Interrupt (Memory DMA/Stream 0)	IVG8
DMA1 Channel 14/15 Interrupt (Memory DMA/Stream 1)	IVG8
DMA2 Channel 12/13 Interrupt (Memory DMA/Stream 0)	IVG9
DMA2 Channel 14/15 Interrupt (Memory DMA/Stream 1)	IVG9
IMDMA Stream 0 Interrupt	IVG12
IMDMA Stream 1 Interrupt	IVG12
Watchdog Timer Interrupt	IVG13
Reserved	IVG7
Reserved	IVG7
Supplemental Interrupt 0	IVG7
Supplemental Interrupt 1	IVG7

Event Control

The ADSP-BF561 provides the user with a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each of the registers is 16 bits wide, while each bit represents a particular event class.

- CEC Interrupt Latch Register (ILAT) – The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but may also be written to clear (cancel) latched events. This register may be read while in supervisor mode and may only be written while in supervisor mode when the corresponding IMASK bit is cleared.
- CEC Interrupt Mask Register (IMASK) – The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and will be processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, thereby preventing the processor from servicing the event

ADSP-BF561

regulator for the processor can be shut off by writing b#00 to the FREQ bits of the VR_CTL register. This disables both CCLK and SCLK. Furthermore, it sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the lowest static power dissipation. Any critical information stored internally (memory contents, register contents, etc.) must be written to a nonvolatile storage device prior to removing power if the processor state is to be preserved. Since V_{DDEXT} is still supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to have power still applied without drawing unwanted current. The internal supply regulator can be woken up by asserting the RESET pin.

Power Savings

As shown in Table 4, the ADSP-BF561 supports two different power domains. The use of multiple power domains maximizes flexibility, while maintaining compliance with industry standards and conventions. By isolating the internal logic of the ADSP-BF561 into its own power domain, separate from the I/O, the processor can take advantage of Dynamic Power Management, without affecting the I/O devices. There are no sequencing requirements for the various power domains.

Table 4. ADSP-BF561 Power Domains

Power Domain	V _{DD} Range
All internal logic	V_{DDINT}
I/O	V_{DDEXT}

The power dissipated by a processor is largely a function of the clock frequency of the processor and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation, while reducing the voltage by 25% reduces dynamic power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic.

The dynamic power management feature of the ADSP-BF561 allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The savings in power dissipation can be modeled using the power savings factor and % power savings calculations.

The power savings factor is calculated as:

$$\text{power savings factor} = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}} \right)^2 \times \left(\frac{t_{RED}}{t_{NOM}} \right)$$

where the variables in the equations are:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

t_{NOM} is the duration running at $f_{CCLKNOM}$

t_{RED} is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as:

$$\% \text{ power savings} = (1 - \text{power savings factor}) \times 100\%$$

VOLTAGE REGULATION

The ADSP-BF561 processor provides an on-chip voltage regulator that can generate appropriate V_{DDINT} voltage levels from the V_{DDEXT} supply. See [Operating Conditions on Page 20](#) for regulator tolerances and acceptable V_{DDEXT} ranges for specific models.

Figure 4 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power (V_{DDEXT}) supplied. While in the hibernate state, V_{DDEXT} can still be applied, thus eliminating the need for external buffers. The voltage regulator can be activated from this power-down state by asserting RESET, which will then initiate a boot sequence. The regulator can also be disabled and bypassed at the user's discretion.

The internal voltage regulation feature is not available on any of the 600 MHz speed grade models or automotive grade models. External voltage regulation is required to ensure correct operation of these parts at 600 MHz.

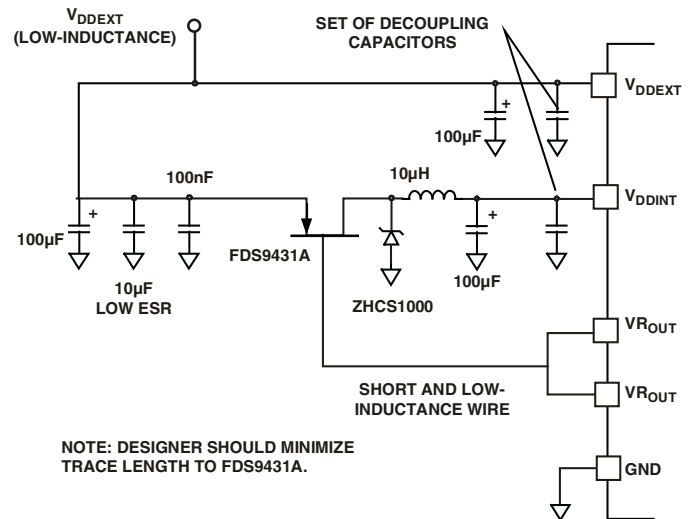


Figure 4. Voltage Regulator Circuit

Voltage Regulator Layout Guidelines

Regulator external component placement, board routing, and bypass capacitors all have a significant effect on noise injected into the other analog circuits on-chip. The VROUT1-0 traces and voltage regulator external components should be considered as noise sources when doing board layout and should not be routed or placed near sensitive circuits or components on the

ADSP-BF561

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in [Table 13](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 13. Absolute Maximum Ratings

Parameter	Value
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.42 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.5 V to +3.8 V
Input Voltage ¹	–0.5 V to +3.8 V
Output Voltage Swing	–0.5 V to $V_{DDEXT} + 0.5$ V
Load Capacitance ²	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature Under Bias	125°C

¹ Applies to 100% transient duty cycle. For other duty cycles see [Table 14](#).

² For proper SDRAM controller operation, the maximum load capacitance is 50 pF (at 3.3 V) or 30 pF (at 2.5 V) for ADDR19–1, DATA15–0, ABE1–0/SDQM1–0, CLKOUT, SCKE, SA10, SRAS, SCAS, SWE, and SMS.

Table 14. Maximum Duty Cycle for Input Transient Voltage¹

V_{IN} Min (V)	V_{IN} Max (V) ²	Maximum Duty Cycle
–0.50	3.80	100%
–0.70	4.00	40%
–0.80	4.10	25%
–0.90	4.20	15%
–1.00	4.30	10%

¹ Applies to all signal pins with the exception of CLKIN, XTAL, VROUT1–0.

² Only one of the listed options can apply to a particular design.

PACKAGE INFORMATION

The information presented in [Figure 7](#) and [Table 15](#) provides details about the package branding for the Blackfin processors. For a complete listing of product availability, see the [Ordering Guide on Page 63](#).



Figure 7. Product Information on Package

Table 15. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

ESD SENSITIVITY



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

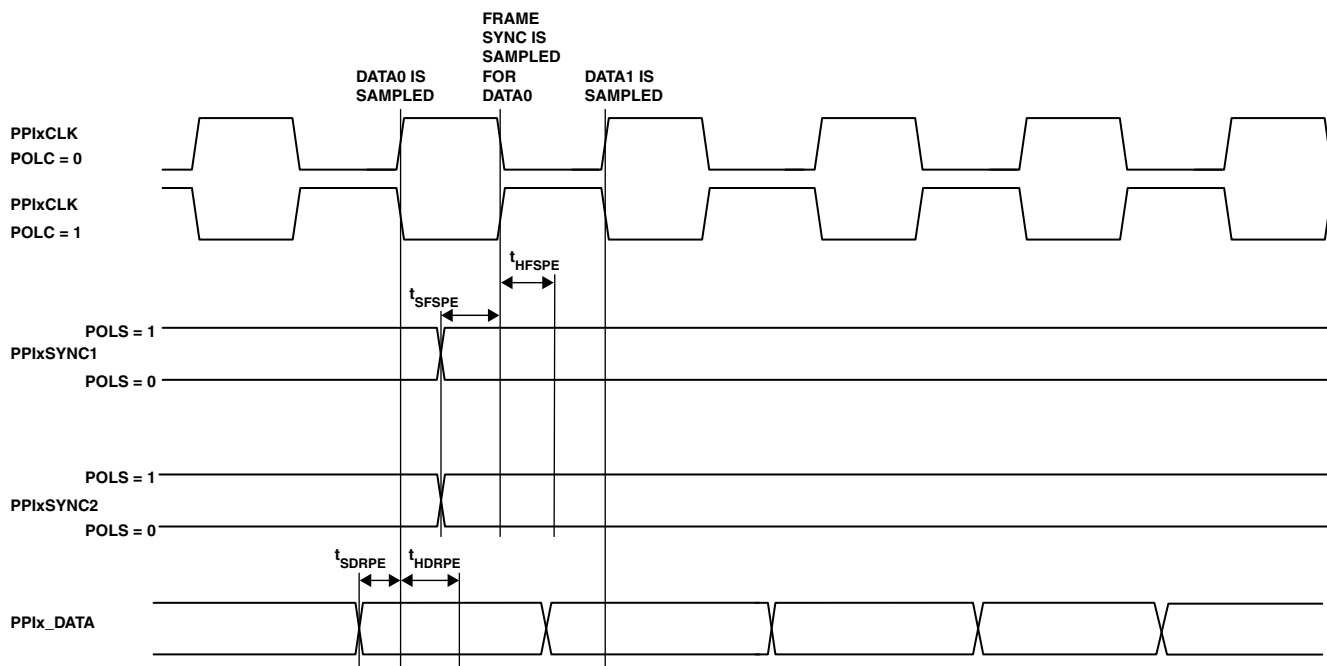


Figure 15. PPI GP Rx Mode with External Frame Sync Timing (Default)

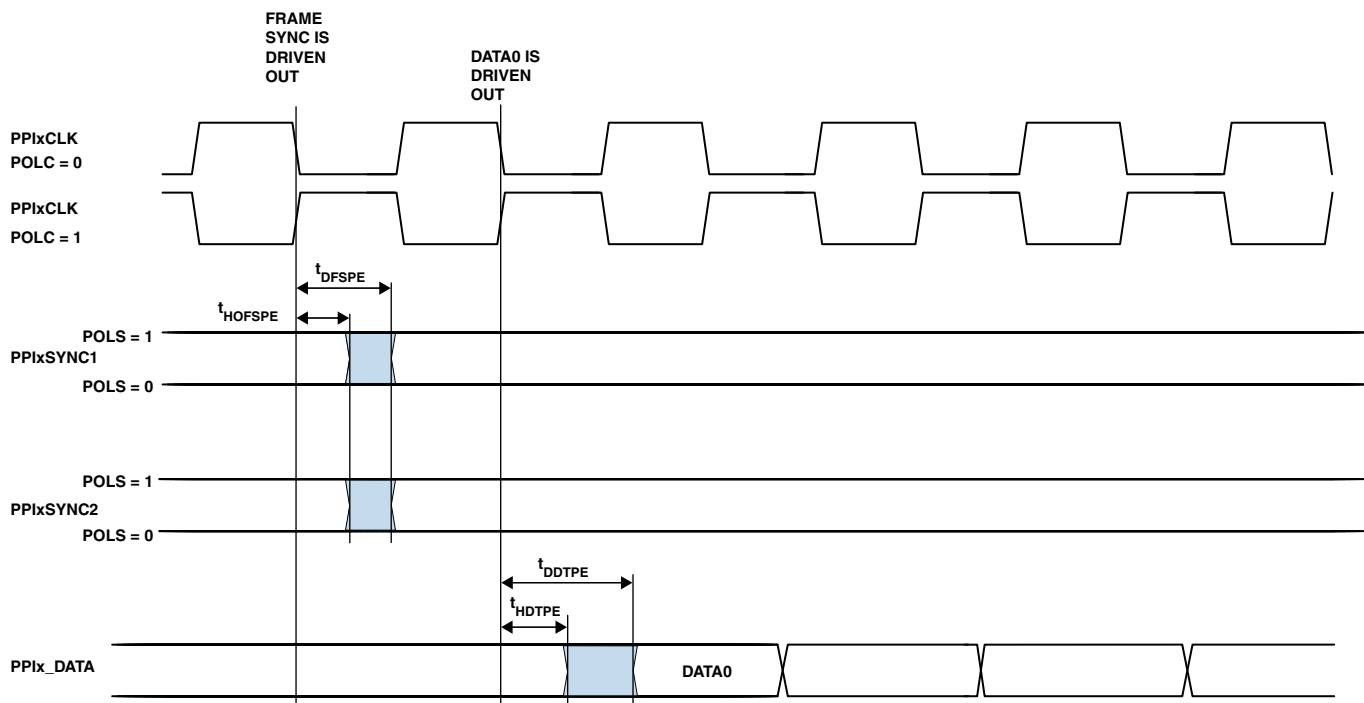


Figure 16. PPI GP Tx Mode with Internal Frame Sync Timing (Default)

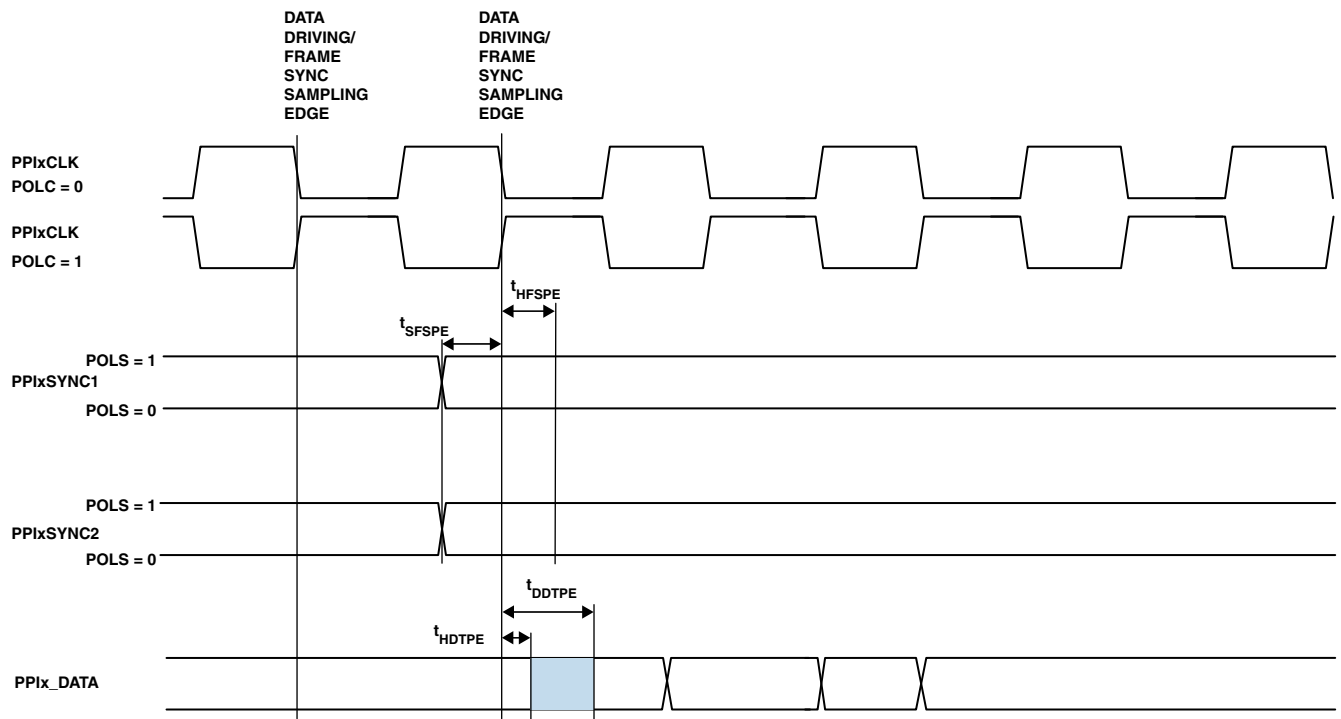


Figure 19. PPI GP Tx Mode with External Frame Sync Timing (Bit 4 of PLL_CTL Set)

ADSP-BF561

Serial Ports

Table 23 through Table 26 on Page 34 and Figure 20 on Page 33 through Figure 22 on Page 34 describe Serial Port operations.

Table 23. Serial Ports—External Clock

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{SFSE} TFSx/RFSx Setup Before TSCLKx/RSCLKx ¹	3.0		ns
t_{HFSE} TFSx/RFSx Hold After TSCLKx/RSCLKx ¹	3.0		ns
t_{SDRE} Receive Data Setup Before RSCLKx ¹	3.0		ns
t_{HDRE} Receive Data Hold After RSCLKx ¹	3.0		ns
t_{SCLKW} TSCLKx/RSCLKx Width	4.5		ns
t_{SCLK} TSCLKx/RSCLKx Period	15.0		ns
t_{SUDTE} Start-Up Delay From SPORT Enable To First External TFSx	4.0		TSCLKx
t_{SUDRE} Start-Up Delay From SPORT Enable To First External RFSx	4.0		RSCLKx
<i>Switching Characteristics</i>			
t_{DFSE} TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx) ²		10.0	ns
t_{HOFSE} TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx) ²	0.0		ns
t_{DDTE} Transmit Data Delay After TSCLKx ²		10.0	ns
t_{HDTTE} Transmit Data Hold After TSCLKx ²	0.0		ns

¹ Referenced to sample edge.

² Referenced to drive edge.

Table 24. Serial Ports—Internal Clock

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{SFSI} TFSx/RFSx Setup Before TSCLKx/RSCLKx ¹	8.0		ns
t_{HFSI} TFSx/RFSx Hold After TSCLKx/RSCLKx ¹	–2.0		ns
t_{SDRI} Receive Data Setup Before RSCLKx ¹	6.0		ns
t_{HDRI} Receive Data Hold After RSCLKx ¹	0.0		ns
t_{SCLKW} TSCLKx/RSCLKx Width	4.5		ns
t_{SCLK} TSCLKx/RSCLKx Period	15.0		ns
<i>Switching Characteristics</i>			
t_{DFSI} TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx) ²		3.0	ns
t_{HOFSI} TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx) ²	–1.0		ns
t_{DDTI} Transmit Data Delay After TSCLKx ²		3.0	ns
t_{HDTI} Transmit Data Hold After TSCLKx ²	–2.0		ns
t_{SCLKIW} TSCLKx/RSCLKx Width	4.5		ns

¹ Referenced to sample edge.

² Referenced to drive edge.

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Table 25. Serial Ports—Enable and Three-State

Parameter	Min	Max	Unit
<i>Switching Characteristics</i>			
t_{DTENE} Data Enable Delay from External TSCLKx ¹	0		ns
t_{DDTE} Data Disable Delay from External TSCLKx ¹		10.0	ns
t_{DTENI} Data Enable Delay from Internal TSCLKx ¹	-2.0		ns
t_{DDTI} Data Disable Delay from Internal TSCLKx ¹		3.0	ns

¹ Referenced to drive edge.

Table 26. External Late Frame Sync

Parameter	Min	Max	Unit
<i>Switching Characteristics</i>			
$t_{DDTLFSE}$ Data Delay from Late External TFSx or External RFSx with MCMEN = 1, MFD = 0 ^{1,2}		10.0	ns
$t_{DTENLFS}$ Data Enable from Late FS or MCMEN = 1, MFD = 0 ^{1,2}	0		ns

¹ MCMEN = 1, TFSx enable and TFSx valid follow $t_{DTENLFS}$ and $t_{DDTLFSE}$.

² If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKx}/2$, then $t_{DDTE/I}$ and $t_{DTENE/I}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

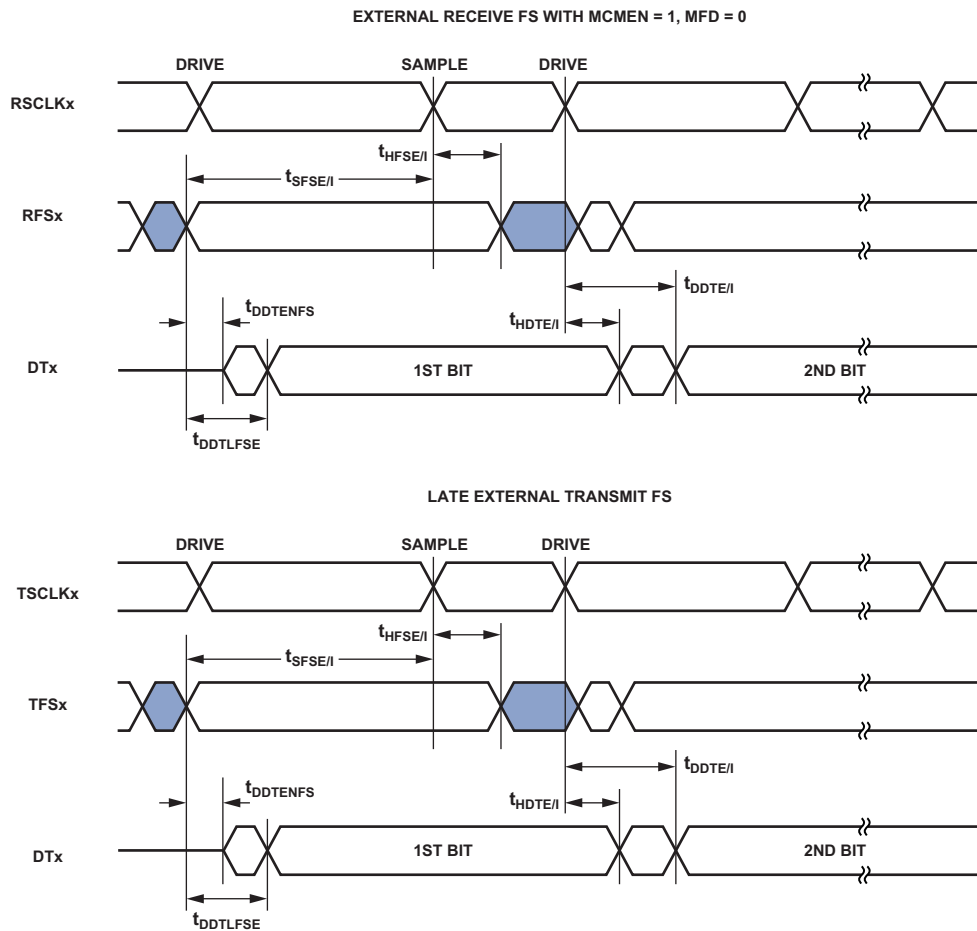


Figure 22. External Late Frame Sync

ADSP-BF561

JTAG Test and Emulation Port Timing

Table 31 and Figure 28 describe JTAG port operations.

Table 31. JTAG Port Timing

Parameter	Min	Max	Unit
<i>Timing Parameters</i>			
t_{TCK} TCK Period	20		ns
t_{STAP} TDI, TMS Setup Before TCK High	4		ns
t_{HTAP} TDI, TMS Hold After TCK High	4		ns
t_{SSYS} System Inputs Setup Before TCK High ¹	4		ns
t_{HSYS} System Inputs Hold After TCK High ¹	5		ns
t_{TRSTW} $\overline{TRST}$ Pulse Width ² (Measured in TCK Cycles)	4		TCK
<i>Switching Characteristics</i>			
t_{DTDO} TDO Delay from TCK Low		10	ns
t_{DSYS} System Outputs Delay After TCK Low ³	0	12	ns

¹ System Inputs = DATA31–0, ARDY, PF47–0, PPI0CLK, PPI1CLK, RSCLK0–1, RFS0–1, DR0PRI, DR0SEC, TSCLK0–1, TFS0–1, DR1PRI, DR1SEC, MOSI, MISO, SCK, RX, RESET, NMIO, NMII, BMODE1–0, $\overline{BR}$, and PPIxD7–0.

² 50 MHz maximum

³ System Outputs = DATA31–0, ADDR25–2, $\overline{ABE3}$ –0, $\overline{AOE}$, $\overline{ARE}$, $\overline{AWE}$, $\overline{AMS3}$ –0, $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SCKE, CLKOUT, SA10, $\overline{SMS3}$ –0, PF47–0, RSCLK0–1, RFS0–1, TSCLK0–1, TFS0–1, DT0PRI, DT0SEC, DT1PRI, DT1SEC, MOSI, MISO, SCK, TX, $\overline{BG}$, $\overline{BGH}$, and PPIxD7–0.

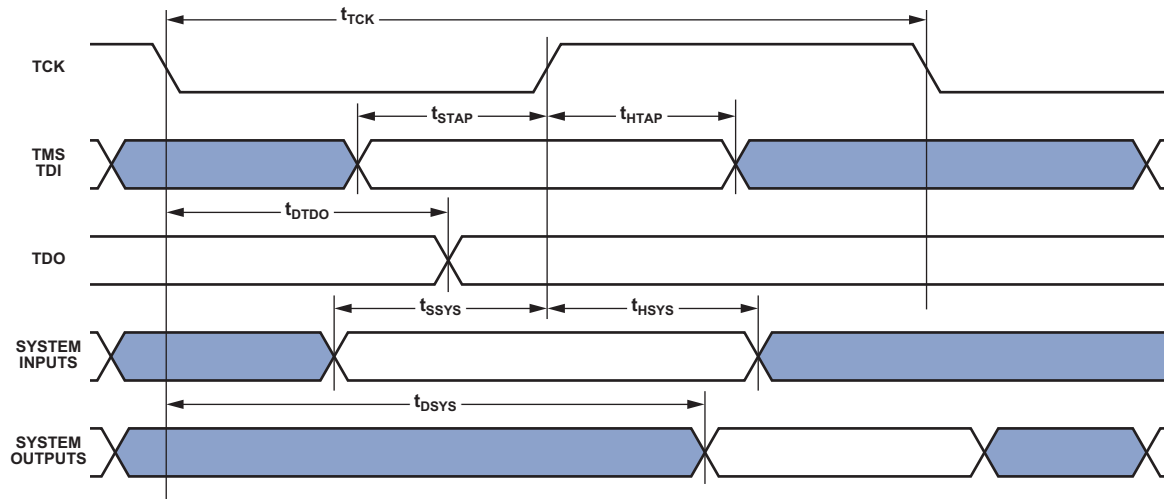


Figure 28. JTAG Port Timing

OUTPUT DRIVE CURRENTS

Figure 29 through Figure 36 on Page 42 show typical current voltage characteristics for the output drivers of the ADSP-BF561 processor. The curves represent the current drive capability of the output drivers as a function of output voltage. Refer to Table 8 on Page 17 to identify the driver type for a pin.

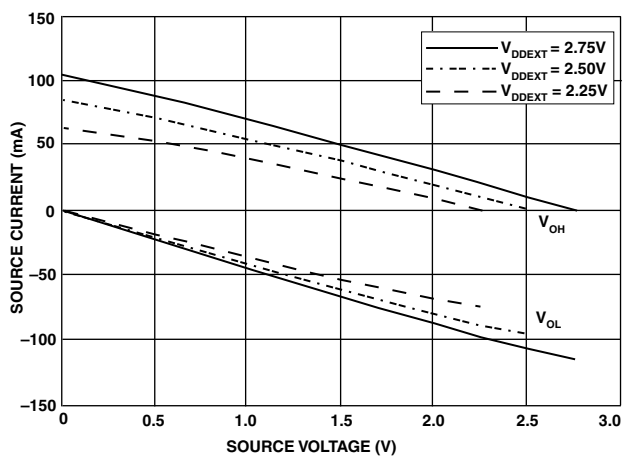


Figure 29. Drive Current A (Low V_{DDEXT})

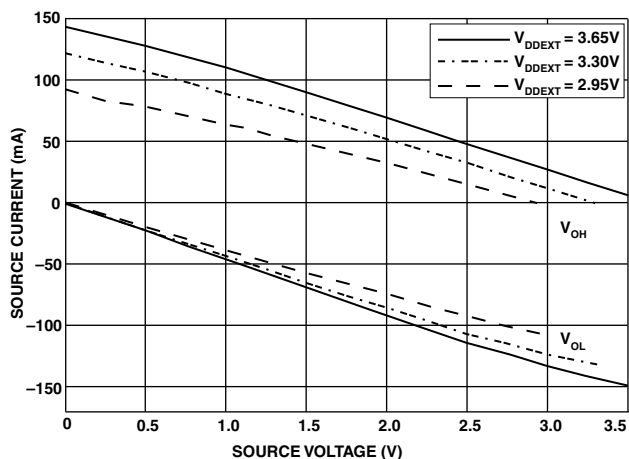


Figure 30. Drive Current A (High V_{DDEXT})

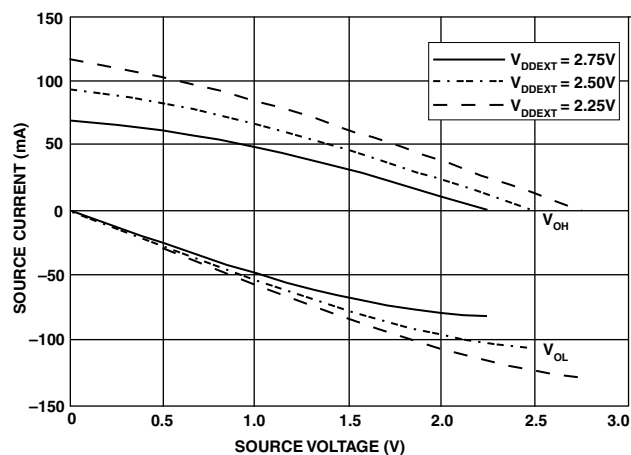


Figure 31. Drive Current B (Low V_{DDEXT})

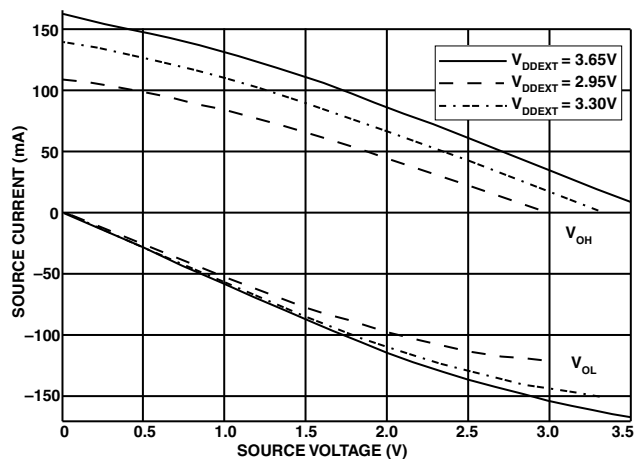


Figure 32. Drive Current B (High V_{DDEXT})

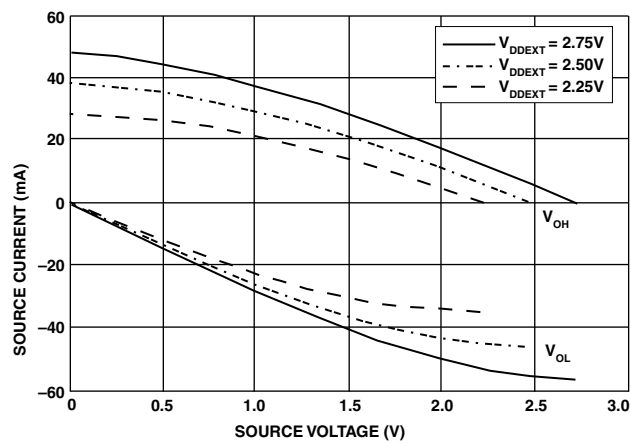


Figure 33. Drive Current C (Low V_{DDEXT})

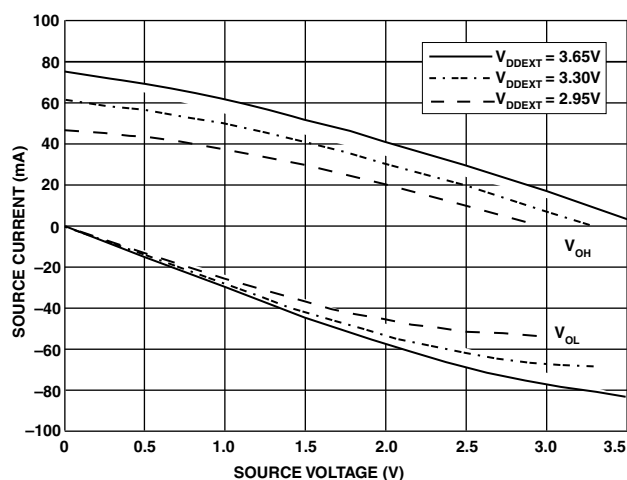


Figure 34. Drive Current C (High V_{DDEXT})

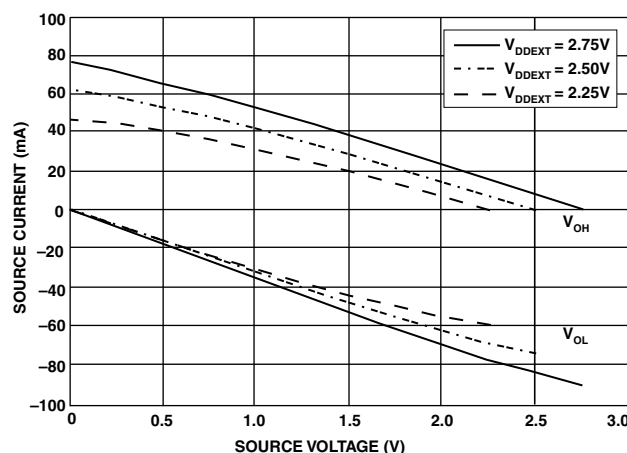


Figure 35. Drive Current D (Low V_{DDEXT})

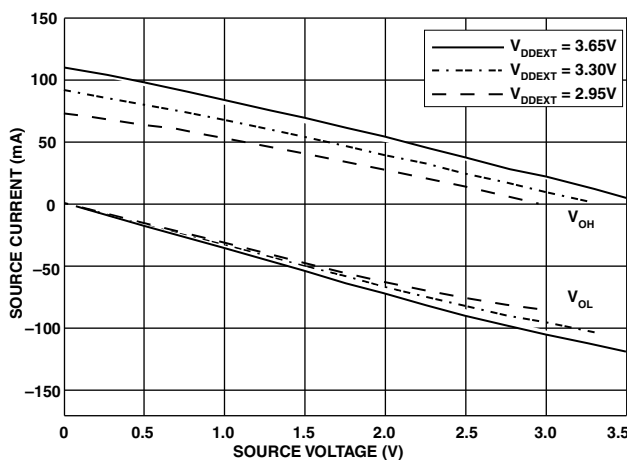


Figure 36. Drive Current D (High V_{DDEXT})

POWER DISSIPATION

Many operating conditions can affect power dissipation. System designers should refer to *Estimating Power for ADSP-BF561 Blackfin Processors (EE-293)* on the Analog Devices website (www.analog.com)—use site search on “EE-293.” This document provides detailed information for optimizing your design for lowest power.

See the *ADSP-BF561 Blackfin Processor Hardware Reference Manual* for definitions of the various operating modes and for instructions on how to minimize system power.

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 37 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V.



Figure 37. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 38 on Page 43.

The time $t_{ENA_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches V_{TRIP} (high) or V_{TRIP} (low). V_{TRIP} (high) is 2.0 V and V_{TRIP} (low) is 1.0 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V. Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP} (high) or V_{TRIP} (low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 38 on Page 43.

$$t_{DIS} = t_{DIS_MEASURED} - t_{DECAY}$$

Table 35. 256-Ball CSP_BGA (17 mm × 17 mm) Ball Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
N9	GND	P5	PF01	R1	PPI1D12	R13	RSCLK1	T9	TDO
N10	BMODE1	P6	PF06	R2	PPI1D11	R14	TSCLK1	T10	TDI
N11	BMODE0	P7	PF08	R3	PPI1D4	R15	NC	T11	$\overline{\text{EMU}}$
N12	RX	P8	PF15	R4	PPI1D1	R16	TFS0	T12	MISO
N13	DR1SEC	P9	NMI1	R5	PF02	T1	VDDEXT	T13	TX
N14	DT1SEC	P10	TMS	R6	PF07	T2	NC	T14	DR1PRI
N15	RFS0	P11	NMI0	R7	PF11	T3	PPI1D3	T15	DT1PRI
N16	DATA30	P12	SCK	R8	PF14	T4	PPI1D2	T16	VDDEXT
P1	PPI1D13	P13	RFS1	R9	TCK	T5	PF03		
P2	PPI1D8	P14	TFS1	R10	$\overline{\text{TRST}}$	T6	PF05		
P3	PPI1D6	P15	DR0SEC	R11	SLEEP	T7	PF10		
P4	PPI1D0	P16	DT0SEC	R12	MOSI	T8	PF13		

256-BALL CSP_BGA (12 mm) BALL ASSIGNMENT

Table 37 lists the 256-Ball CSP_BGA (12 mm × 12 mm) ball assignment by ball number. Table 38 on Page 53 lists the ball assignment alphabetically by signal.

Table 37. 256-Ball CSP_BGA (12 mm × 12 mm) Ball Assignment (Numerically by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A01	VDDEXT	C09	$\overline{SM52}$	F01	CLKIN	H09	GND	L01	PPI0D0
A02	ADDR24	C10	$\overline{SRA5}$	F02	VDDEXT	H10	GND	L02	PPI1SYNC2
A03	ADDR20	C11	GND	F03	$\overline{RESET}$	H11	VDDINT	L03	GND
A04	VDDEXT	C12	$\overline{BGH}$	F04	PPI0D10	H12	DATA16	L04	PPI1SYNC3
A05	ADDR14	C13	GND	F05	ADDR21	H13	DATA18	L05	VDDEXT
A06	ADDR10	C14	ADDR07	F06	ADDR17	H14	DATA20	L06	PPI1D11
A07	$\overline{AMS3}$	C15	DATA1	F07	VDDINT	H15	DATA17	L07	GND
A08	$\overline{AWE}$	C16	DATA3	F08	GND	H16	DATA19	L08	VDDINT
A09	VDDEXT	D01	PPI0D13	F09	VDDINT	J01	VROUT0	L09	GND
A10	$\overline{SM53}$	D02	PPI0D15	F10	GND	J02	VROUT1	L10	VDDEXT
A11	SCLK0	D03	PPI0SYNC3	F11	ADDR08	J03	PPI0D2	L11	GND
A12	SCLK1	D04	ADDR23	F12	DATA10	J04	PPI0D3	L12	DR0PRI
A13	$\overline{BG}$	D05	GND	F13	DATA8	J05	PPI0D1	L13	TFS0
A14	$\overline{ABE2}$	D06	GND	F14	DATA12	J06	VDDEXT	L14	GND
A15	$\overline{ABE3}$	D07	ADDR09	F15	DATA9	J07	GND	L15	DATA27
A16	VDDEXT	D08	GND	F16	DATA11	J08	VDDINT	L16	DATA29
B01	PPI1CLK	D09	ARDY	G01	XTAL	J09	VDDINT	M01	PPI1D15
B02	ADDR22	D10	$\overline{SCAS}$	G02	GND	J10	VDDINT	M02	PPI1D13
B03	ADDR18	D11	SA10	G03	VDDEXT	J11	GND	M03	PPI1D9
B04	ADDR16	D12	VDDEXT	G04	BYPASS	J12	DATA30	M04	GND
B05	ADDR12	D13	ADDR02	G05	PPI0D14	J13	DATA22	M05	NC
B06	VDDEXT	D14	GND	G06	GND	J14	GND	M06	PF3
B07	$\overline{AMS1}$	D15	DATA5	G07	GND	J15	DATA21	M07	PF7
B08	$\overline{ARE}$	D16	DATA6	G08	GND	J16	DATA23	M08	VDDINT
B09	$\overline{SM51}$	E01	GND	G09	VDDINT	K01	PPI0D6	M09	GND
B10	SCKE	E02	PPI0D11	G10	ADDR05	K02	PPI0D4	M10	BMODE0
B11	VDDEXT	E03	PPI0D12	G11	ADDR03	K03	PPI0D8	M11	SCK
B12	$\overline{BR}$	E04	PPI0SYNC1	G12	DATA15	K04	PPI1SYNC1	M12	DR1PRI
B13	$\overline{ABE1}$	E05	ADDR15	G13	DATA14	K05	PPI1D14	M13	NC
B14	ADDR06	E06	ADDR13	G14	GND	K06	VDDEXT	M14	VDDEXT
B15	ADDR04	E07	$\overline{AMS2}$	G15	DATA13	K07	GND	M15	DATA31
B16	DATA0	E08	VDDINT	G16	VDDEXT	K08	VDDINT	M16	DT0PRI
C01	PPI0SYNC2	E09	$\overline{SM50}$	H01	GND	K09	GND	N01	PPI1D12
C02	PPI0CLK	E10	$\overline{SWE}$	H02	GND	K10	GND	N02	PPI1D10
C03	ADDR25	E11	$\overline{ABE0}$	H03	PPI0D9	K11	VDDINT	N03	PPI1D3
C04	ADDR19	E12	DATA2	H04	PPI0D7	K12	DATA28	N04	PPI1D1
C05	GND	E13	GND	H05	PPI0D5	K13	DATA26	N05	PF1
C06	ADDR11	E14	DATA4	H06	VDDINT	K14	DATA24	N06	PF9
C07	$\overline{AOE}$	E15	DATA7	H07	VDDINT	K15	DATA25	N07	GND
C08	$\overline{AMS0}$	E16	VDDEXT	H08	GND	K16	VDDEXT	N08	PF13

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Table 37. 256-Ball CSP_BGA (12 mm × 12 mm) Ball Assignment (Numerically by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
N09	TDO	P05	GND	R01	PPI1D7	R13	TX/PF26	T09	TCK
N10	BMODE1	P06	PF5	R02	PPI1D6	R14	TSCLK1	T10	TMS
N11	MOSI	P07	PF11	R03	PPI1D2	R15	DT1PRI	T11	SLEEP
N12	GND	P08	PF15	R04	PPI1D0	R16	RFS0	T12	VDDEXT
N13	RFS1	P09	GND	R05	PF4	T01	VDDEXT	T13	RX/PF27
N14	GND	P10	$\overline{\text{TRST}}$	R06	PF8	T02	PPI1D4	T14	DR1SEC
N15	DT0SEC	P11	NMI0	R07	PF10	T03	VDDEXT	T15	DT1SEC
N16	TSCLK0	P12	GND	R08	PF14	T04	PF2	T16	VDDEXT
P01	PPI1D8	P13	RSCLK1	R09	NMI1	T05	PF6		
P02	GND	P14	TFS1	R10	TDI	T06	VDDEXT		
P03	PPI1D5	P15	RSCLK0	R11	$\overline{\text{EMU}}$	T07	PF12		
P04	PF0	P16	DR0SEC	R12	MISO	T08	VDDEXT		

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Figure 52 lists the top view of the 297-Ball PBGA ball configuration. Figure 53 lists the bottom view.

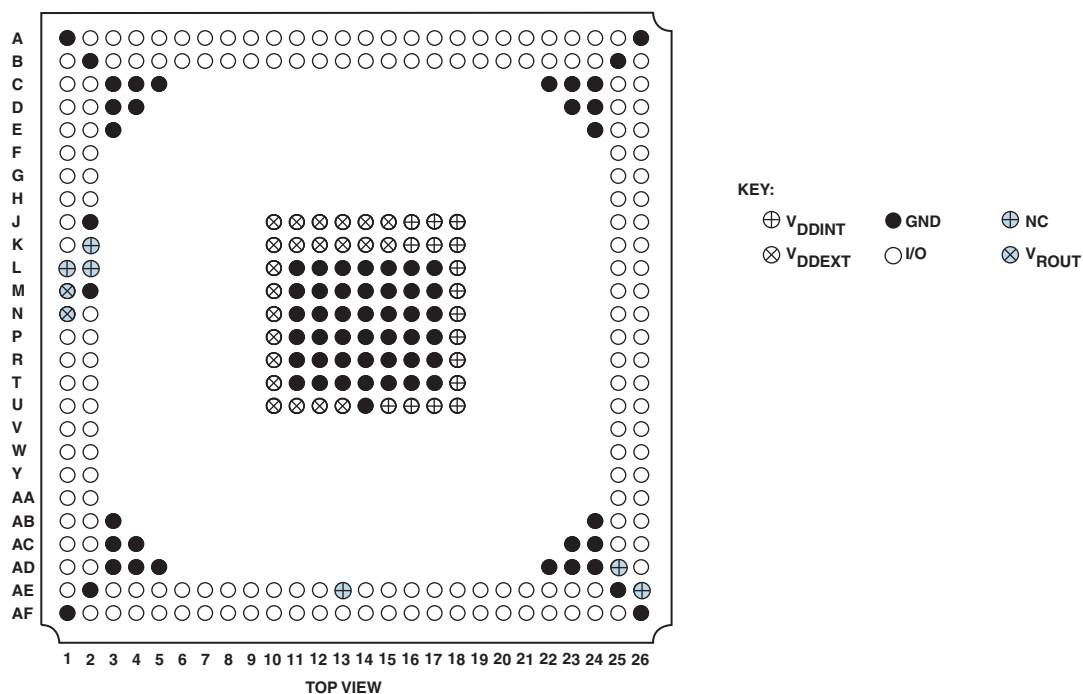


Figure 52. 297-Ball PBGA Ball Configuration (Top View)

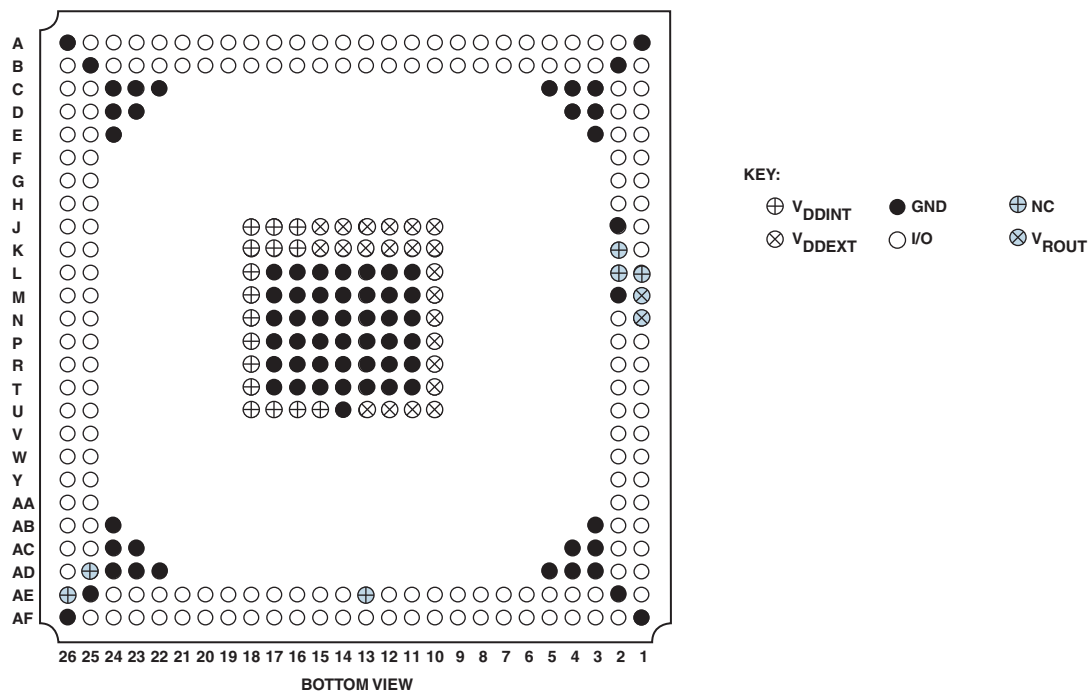


Figure 53. 297-Ball PBGA Ball Configuration (Bottom View)

OUTLINE DIMENSIONS

Dimensions in the outline dimension figures are shown in millimeters.

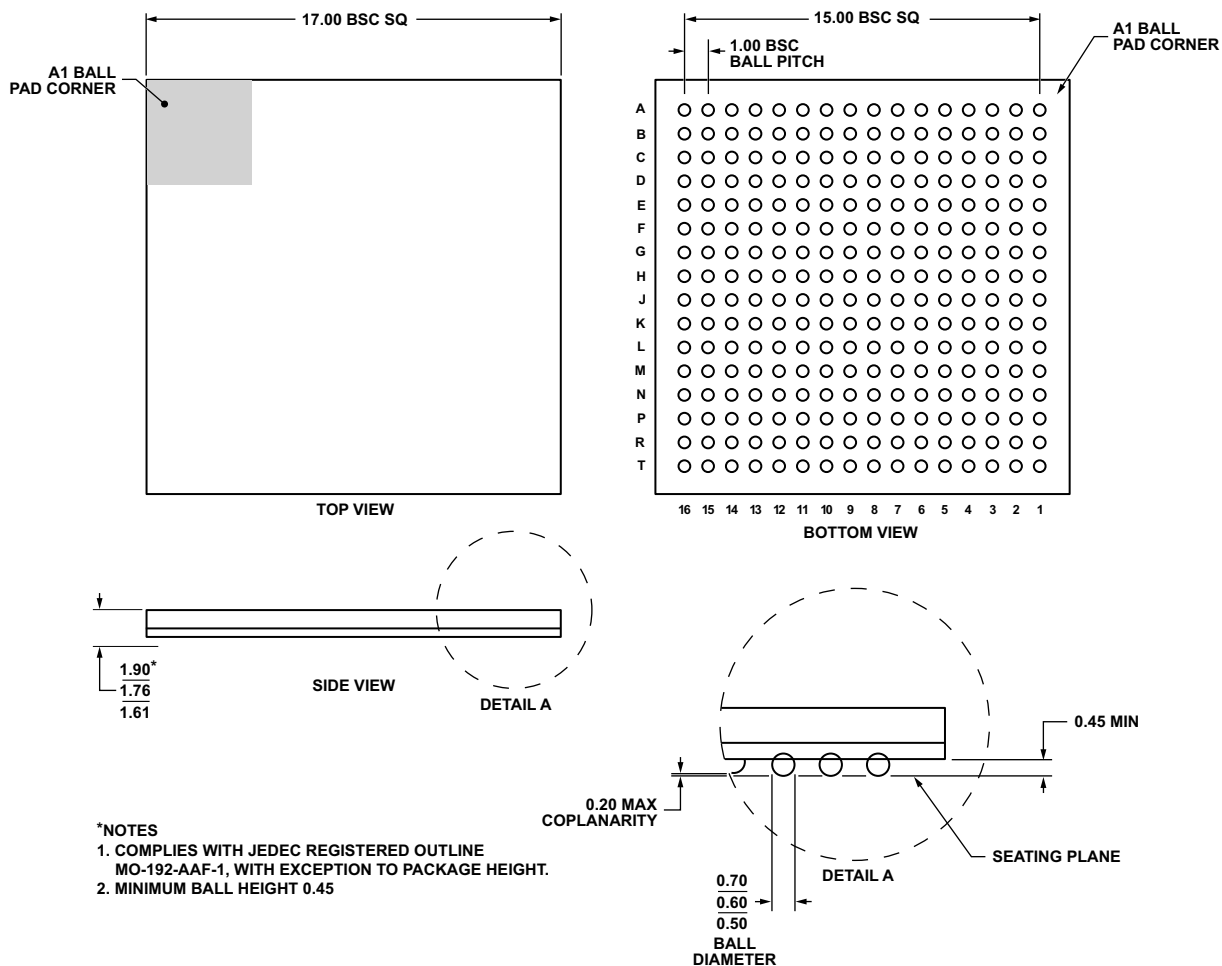
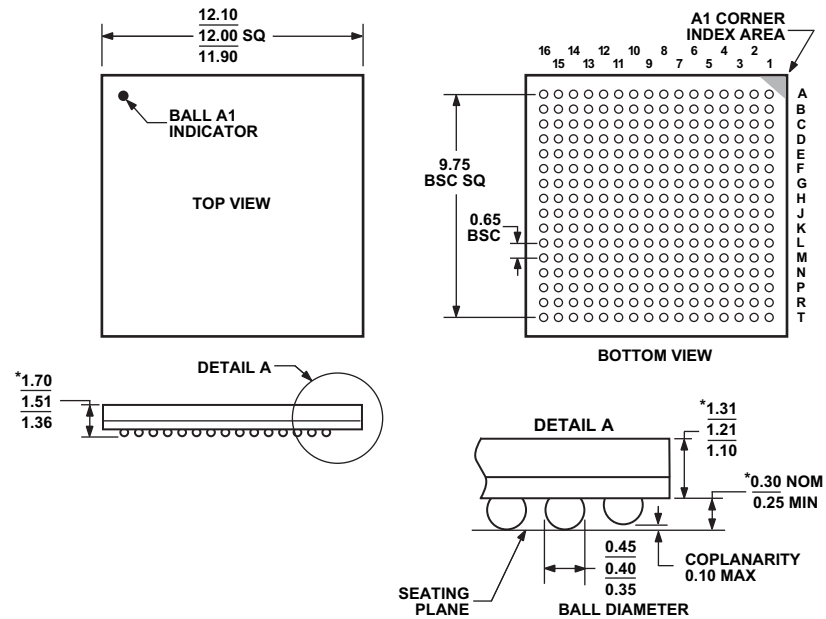
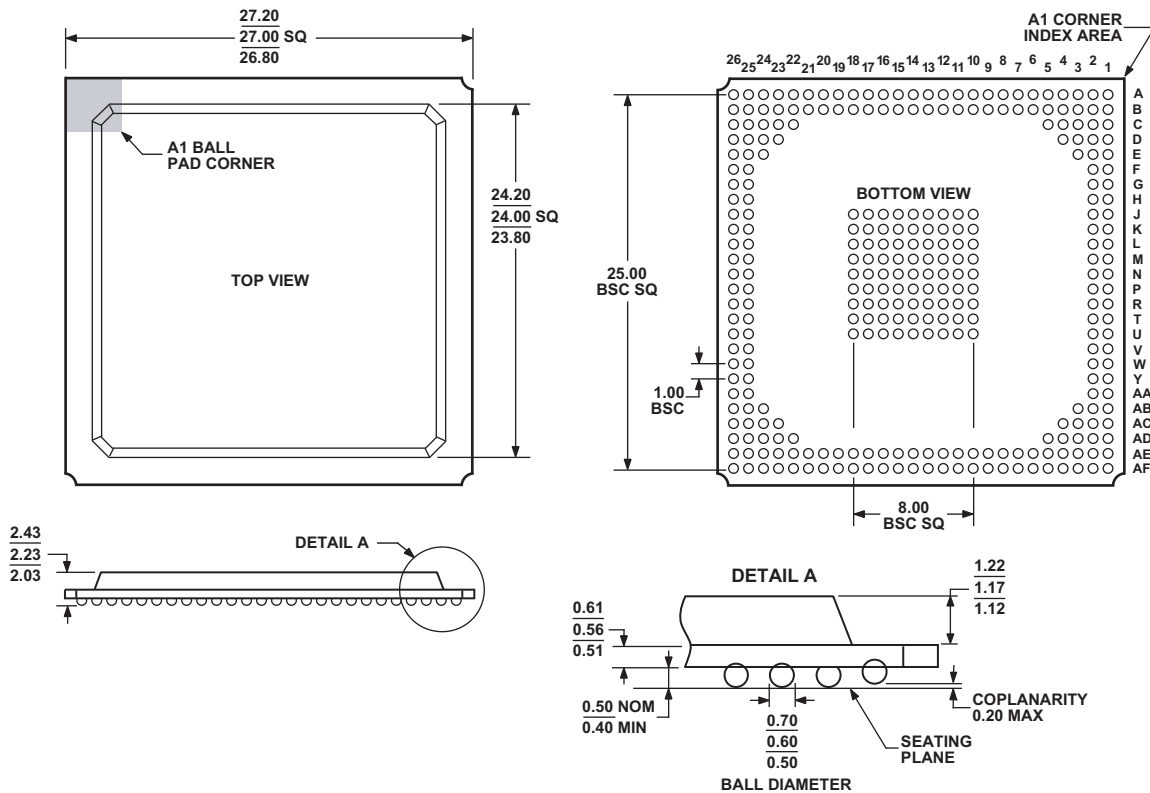


Figure 54. 256-Ball Chip Scale Package Ball Grid Array (CSP_BGA) (BC-256-4)



*COMPLIANT TO JEDEC STANDARDS MO-225 WITH EXCEPTION TO DIMENSIONS INDICATED BY AN ASTERISK.

Figure 55. 256-Ball Chip Scale Package Ball Grid Array (CSP_BGA) (BC-256-1)



COMPLIANT TO JEDEC STANDARDS MS-034-AAL-1

Figure 56. 297-Ball Plastic Ball Grid Array (PBGA) (B-297)

