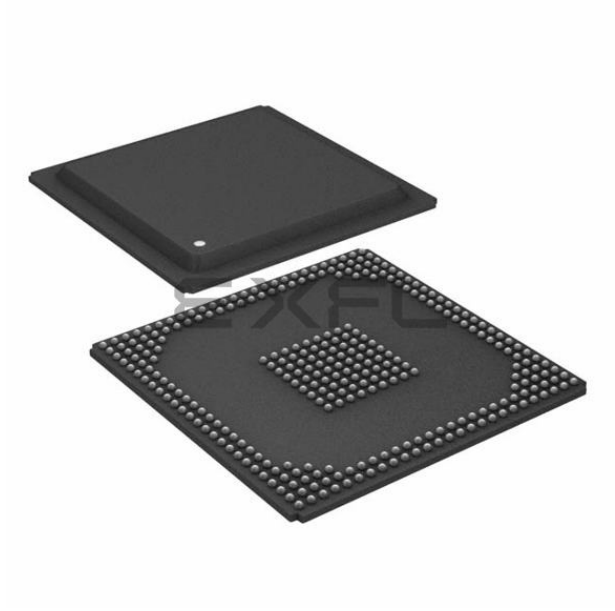

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	SPI, SSP, UART
Clock Rate	600MHz
Non-Volatile Memory	External
On-Chip RAM	328kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.35V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	297-BGA
Supplier Device Package	297-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf561skbz600

- ADSP-BF561: Blackfin Embedded Symmetric Multiprocessor Data Sheet

Emulator Manuals

- HPUSB, USB, and HPPCI Emulator User's Guide
- ICE-1000/ICE-2000 Emulator User's Guide
- ICE-100B Emulator User's Guide

Evaluation Kit Manuals

- ADSP-BF561 EZ-KIT Lite® Evaluation System Manual
- Blackfin® A-V EZ-Extender® Manual
- Blackfin® EZ-Extender® Manual
- Blackfin® FPGA EZ-Extender® Manual
- Blackfin®/SHARC® USB EZ-Extender® Manual

Integrated Circuit Anomalies

- ADSP-BF561 Blackfin Anomaly List for Revisions 0.3, 0.5

Processor Manuals

- ADSP-BF561 Blackfin ® Processor Hardware Reference
- ADSP-BF5xx/ADSP-BF60x Blackfin® Processor Programming Reference
- Blackfin Processors: Manuals

Product Highlight

- ADSP-BF561 Blackfin Dual-Core Embedded Processor
- Blackfin Processor Family Product Highlight
- EZ-KIT Lite for Analog Devices ADSP-BF561 Blackfin Processor

Software Manuals

- CrossCore® Embedded Studio 2.5.0 Assembler and Preprocessor Manual
- CrossCore® Embedded Studio 2.5.0 C/C++ Compiler and Library Manual for Blackfin Processors
- CrossCore® Embedded Studio 2.5.0 Linker and Utilities Manual
- CrossCore® Embedded Studio 2.5.0 Loader and Utilities Manual
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- lwIP for CrossCore® Embedded Studio 1.0.0 User's Guide
- VisualDSP++® 5.0 Assembler and Preprocessor Manual
- VisualDSP++® 5.0 C/C++ Compiler and Library Manual for Blackfin Processors
- VisualDSP++® 5.0 Device Drivers and System Services Manual for Blackfin Processors
- VisualDSP++® 5.0 Kernel (VDK) Users Guide
- VisualDSP++® 5.0 Licensing Guide
- VisualDSP++® 5.0 Linker and Utilities Manual
- VisualDSP++® 5.0 Loader and Utilities Manual
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SOFTWARE AND SYSTEMS REQUIREMENTS

- Software and Tools Anomalies Search

TOOLS AND SIMULATIONS

- ADSP-BF561 Blackfin Processor BSDL File 256-Ball CSP BGA Package
- ADSP-BF561 Blackfin Processor BSDL File 256-Ball Sparse CSP_BGA Package
- ADSP-BF561 Blackfin Processor BSDL File 297-Ball PBGA Package
- ADSP-BF561 Blackfin Processor Core B BSDL File All Packages
- Designing with BGA
- Blackfin Processors Software and Tools
- ADSP-BF561 Blackfin Processor IBIS Datafile for 12x12 CSP BGA Package (02/2008)
- ADSP-BF561 Blackfin Processor IBIS Datafile for 17x17 CSP BGA Package (11/2008)
- ADSP-BF561 Blackfin Processor IBIS Datafile for 27x27 PBGA Package (02/2008)

REFERENCE MATERIALS

Customer Case Studies

- Dahua Case Study
- UTAS Medical Equipment Ensures High Quality Patient Care with Help from Analog Devices

Technical Articles

- An Efficient Asynchronous Sampling-rate Conversion Algorithm for Multi-channel Audio Applications
- Blackfin Processor Targets Digital Media Open Source Applications
- Blackfin Processor's Parallel Peripheral Interface Simplifies LCD Connection in Portable Multimedia
- Designing IPTV Set-top Boxes Without Getting Boxed In
- Enhance Processor Performance in Open-Source Applications
- High Performance DSPs for Portable Applications
- Is it Really Possible to Play DVD Quality Media While Executing Linux Applications?
- Understanding Advanced Processor Features Promotes Efficient Coding
- Video Filtering Considerations for Media Processors

White Papers

- A BDTI Analysis of the Analog Devices ADSP-BF5xx
- Blackfin Car Telematics Platform Brings Low Cost Telematics to the Mass Market
- Device-Based Social Networking
- LabVIEW 1000m Below the Waves: Synchronized Sampling of Autonomous Units Through Sound
- Secure, Field Upgradeable OS Architecture for Blackfin
- Security Without Compromise
- Unifying Microarchitecture for Embedded Media Processing

DESIGN RESOURCES

- ADSP-BF561 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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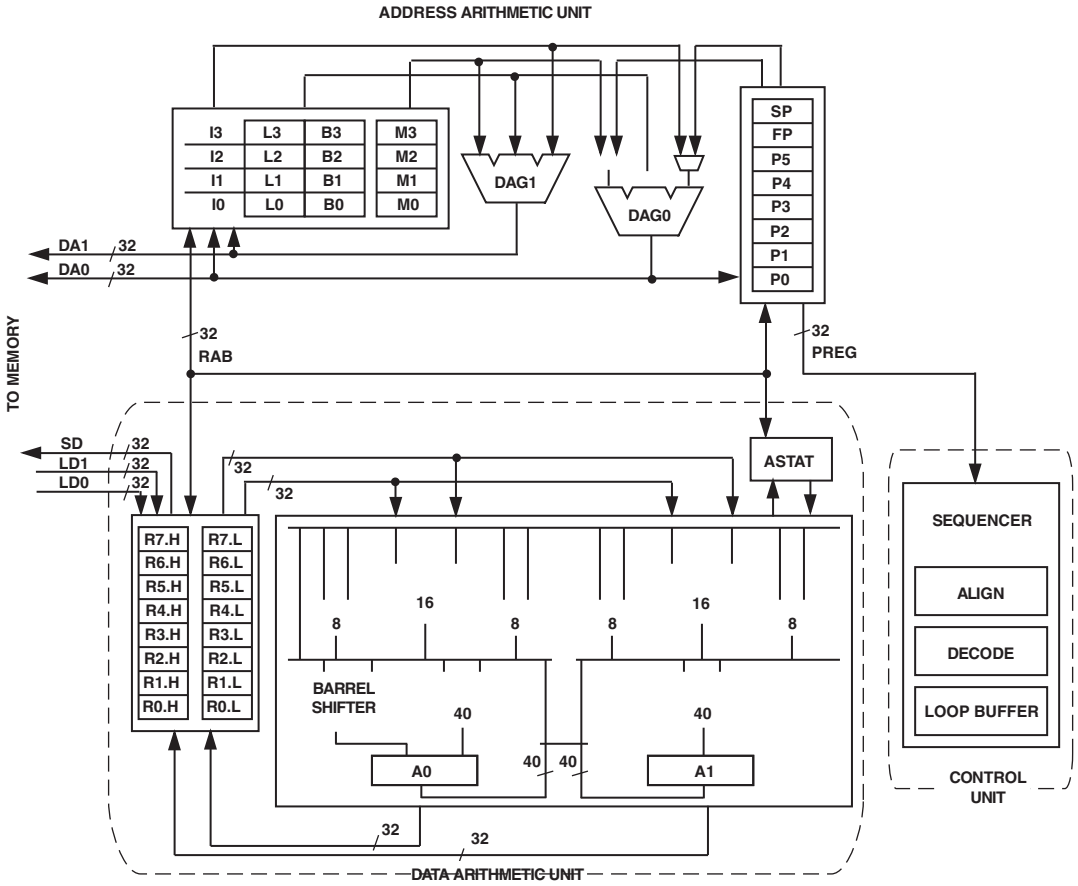

Figure 2. Blackfin Processor Core

MEMORY ARCHITECTURE

The ADSP-BF561 views memory as a single unified 4G byte address space, using 32-bit addresses. All resources including internal memory, external memory, and I/O control registers occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low latency memory as cache or SRAM very close to the processor, and larger, lower cost and performance memory systems farther away from the processor. The ADSP-BF561 memory map is shown in Figure 3.

The L1 memory system in each core is the highest performance memory available to each Blackfin core. The L2 memory provides additional capacity with lower performance. Lastly, the off-chip memory system, accessed through the External Bus Interface Unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing more than 768M bytes of physical memory. The memory DMA controllers provide high bandwidth data movement capability. They can perform block transfers of code or data between the internal L1/L2 memories and the external memory spaces.

Internal (On-Chip) Memory

The ADSP-BF561 has four blocks of on-chip memory providing high bandwidth access to the core.

The first is the L1 instruction memory of each Blackfin core consisting of 16K bytes of four-way set-associative cache memory and 16K bytes of SRAM. The cache memory may also be configured as an SRAM. This memory is accessed at full processor speed. When configured as SRAM, each of the two 16K banks of memory is broken into 4K sub-banks which can be independently accessed by the processor and DMA.

The second on-chip memory block is the L1 data memory of each Blackfin core which consists of four banks of 16K bytes each. Two of the L1 data memory banks can be configured as one way of a two-way set-associative cache or as an SRAM. The other two banks are configured as SRAM. All banks are accessed at full processor speed. When configured as SRAM, each of the four 16K banks of memory is broken into 4K sub-banks which can be independently accessed by the processor and DMA.

The third memory block associated with each core is a 4K byte scratchpad SRAM which runs at the same speed as the L1 memories, but is only accessible as data SRAM (it cannot be configured as cache memory and is not accessible via DMA).

PIN DESCRIPTIONS

ADSP-BF561 pin definitions are listed in Table 8. In order to maintain maximum function and reduce package size and pin count, some pins have multiple functions. In cases where pin function is reconfigurable, the default state is shown in plain text, while alternate functionality is shown in italics.

All pins are three-stated during and immediately after reset, except the external memory interface, asynchronous memory control, and synchronous memory control pins. These pins are all driven high, with the exception of CLKOUT, which toggles at the system clock rate. However if $\overline{BR}$ is active, the memory pins are also three-stated.

All I/O pins have their input buffers disabled, with the exception of the pins that need pull-ups or pull-downs if unused, as noted in Table 8.

Table 8. Pin Descriptions

Pin Name	Type	Function	Driver Type[1]
EBIU			
ADDR25–2	O	Address Bus for Async/Sync Access	A
DATA31–0	I/O	Data Bus for Async/Sync Access	A
$\overline{ABE3–0}$/SDQM3–0	O	Byte Enables/Data Masks for Async/Sync Access	A
$\overline{BR}$	I	Bus Request (This pin should be pulled HIGH if not used.)	
$\overline{BG}$	O	Bus Grant	A
$\overline{BGH}$	O	Bus Grant Hang	A
EBIU (ASYNC)			
$\overline{AMS3–0}$	O	Bank Select	A
ARDY	I	Hardware Ready Control (This pin should be pulled HIGH if not used.)	
$\overline{AOE}$	O	Output Enable	A
$\overline{AWE}$	O	Write Enable	A
$\overline{ARE}$	O	Read Enable	A
EBIU (SDRAM)			
$\overline{SRAS}$	O	Row Address Strobe	A
$\overline{SCAS}$	O	Column Address Strobe	A
$\overline{SWE}$	O	Write Enable	A
SCKE	O	Clock Enable	A
SCLK0/CLKOUT	O	Clock Output Pin 0	B
SCLK1	O	Clock Output Pin 1	B
SA10	O	SDRAM A10 Pin	A
$\overline{SMS3–0}$	O	Bank Select	A

Table 8. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
PF/SPI/TIMER			
PF0/*SPISS*/*TMR0*	I/O	Programmable Flag/*Slave SPI Select/Timer*	C
PF1/*SPISEL1*/*TMR1*	I/O	Programmable Flag/*SPI Select/Timer*	C
PF2/*SPISEL2*/*TMR2*	I/O	Programmable Flag/*SPI Select/Timer*	C
PF3/*SPISEL3*/*TMR3*	I/O	Programmable Flag/*SPI Select/Timer*	C
PF4/*SPISEL4*/*TMR4*	I/O	Programmable Flag/*SPI Select/Timer*	C
PF5/*SPISEL5*/*TMR5*	I/O	Programmable Flag/*SPI Select/Timer*	C
PF6/*SPISEL6*/*TMR6*	I/O	Programmable Flag/*SPI Select/Timer*	C
PF7/*SPISEL7*/*TMR7*	I/O	Programmable Flag/*SPI Select/Timer*	C
PF8	I/O	Programmable Flag	C
PF9	I/O	Programmable Flag	C
PF10	I/O	Programmable Flag	C
PF11	I/O	Programmable Flag	C
PF12	I/O	Programmable Flag	C
PF13	I/O	Programmable Flag	C
PF14	I/O	Programmable Flag	C
PF15/*EXT CLK*	I/O	Programmable Flag/*External Timer Clock Input*	C
PPI0			
PPI0D15–8/*PF47–40*	I/O	PPI Data/*Programmable Flag Pins*	C
PPI0D7–0	I/O	PPI Data Pins	C
PPI0CLK	I	PPI Clock	
PPI0SYNC1/*TMR8*	I/O	PPI Sync/*Timer*	C
PPI0SYNC2/*TMR9*	I/O	PPI Sync/*Timer*	C
PPI0SYNC3	I/O	PPI Sync	C
PPI1			
PPI1D15–8/*PF39–32*	I/O	PPI Data/*Programmable Flag Pins*	C
PPI1D7–0	I/O	PPI Data Pins	C
PPI1CLK	I	PPI Clock	
PPI1SYNC1/*TMR10*	I/O	PPI Sync/*Timer*	C
PPI1SYNC2/*TMR11*	I/O	PPI Sync/*Timer*	C
PPI1SYNC3	I/O	PPI Sync	C
SPORT0			
RSCLK0/*PF28*	I/O	Sport0 Receive Serial Clock/*Programmable Flag*	D
RFS0/*PF19*	I/O	Sport0 Receive Frame Sync/*Programmable Flag*	C
DR0PRI	I	Sport0 Receive Data Primary	
DR0SEC/*PF20*	I/O	Sport0 Receive Data Secondary/*Programmable Flag*	C
TSCLK0/*PF29*	I/O	Sport0 Transmit Serial Clock/*Programmable Flag*	D
TFS0/*PF16*	I/O	Sport0 Transmit Frame Sync/*Programmable Flag*	C
DT0PRI/*PF18*	I/O	Sport0 Transmit Data Primary/*Programmable Flag*	C
DT0SEC/*PF17*	I/O	Sport0 Transmit Data Secondary/*Programmable Flag*	C

Table 11. Phase-Locked Loop Operating Conditions

Parameter	Min	Max	Unit
Voltage Controlled Oscillator (VCO) Frequency	50	Maximum f_{CCLK}	MHz

Table 12. System Clock (SCLK) Requirements

Parameter[1]		Max V_{DDEXT} = 2.5V/3.3V	Unit
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} \geq 1.14$ V)	133[2]	MHz
f_{SCLK}	CLKOUT/SCLK Frequency ($V_{DDINT} < 1.14$ V)	100	MHz

[1] t_{SCLK} (= $1/f_{SCLK}$) must be greater than or equal to t_{CCLK}.
[2] Rounded number. Guaranteed to t_{SCLK} = 7.5 ns. See Table 20 on Page 26.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Typical	Max	Unit
V_{OH}	High Level Output Voltage[1]	V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage[1]	V_{DDEXT} = 3.0 V, I_{OL} = 2.0 mA			0.4	V
I_{IH}	High Level Input Current[2]	V_{DDEXT} = Maximum, V_{IN} = V_{DD} Maximum			10.0	µA
I_{IHP}	High Level Input Current JTAG[3]	V_{DDEXT} = Maximum, V_{IN} = V_{DD} Maximum			50.0	µA
I_{IL}[4]	Low Level Input Current[2]	V_{DDEXT} = Maximum, V_{IN} = 0 V			10.0	µA
I_{OZH}	Three-State Leakage Current[5]	V_{DDEXT} = Maximum, V_{IN} = V_{DD} Maximum			10.0	µA
I_{OZL}[4]	Three-State Leakage Current[5]	V_{DDEXT} = Maximum, V_{IN} = 0 V			10.0	µA
C_{IN}	Input Capacitance[6]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		4	8[7]	pF
$I_{DDHIBERNATE}$[8]	V_{DDEXT} Current in Hibernate Mode	CLKIN=0 MHz, V_{DDEXT} = 3.65 V with Voltage Regulator Off (V_{DDINT} = 0 V)		50		µA
$I_{DDDEEPSLEEP}$[9]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 0.8 V, $T_{JUNCTION}$ = 25°C		70		mA
I_{DD_TYP}[9, 10]	V_{DDINT} Current	V_{DDINT} = 0.8 V, f_{CCLK} = 50 MHz, $T_{JUNCTION}$ = 25°C		127		mA
I_{DD_TYP}[9, 10]	V_{DDINT} Current	V_{DDINT} = 1.25 V, f_{CCLK} = 500 MHz, $T_{JUNCTION}$ = 25°C		660		mA
I_{DD_TYP}[9, 10]	V_{DDINT} Current	V_{DDINT} = 1.35 V, f_{CCLK} = 600 MHz, $T_{JUNCTION}$ = 25°C		818		mA

[1] Applies to output and bidirectional pins.
[2] Applies to input pins except JTAG inputs.
[3] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{TRST}$).
[4] Absolute value.
[5] Applies to three-statable pins.
[6] Applies to all signal pins.
[7] Guaranteed, but not tested.
[8] CLKIN must be tied to V_{DDEXT} or GND during hibernate.
[9] Maximum current drawn. See *Estimating Power for ADSP-BF561 Blackfin Processors (EE-293)* on the Analog Devices website (www.analog.com)—use site search on "EE-293".
[10] Both cores executing 75% dual MAC, 25% ADD instructions with moderate data bus activity.

System designers should refer to *Estimating Power for the ADSP-BF561 (EE-293)*, which provides detailed information for optimizing designs for lowest power. All topics discussed in this section are described in detail in EE-293. Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 21 shows the current dissipation for internal circuitry (V_{DDINT}).

TIMING SPECIFICATIONS

Clock and Reset Timing

Table 16 and Figure 8 describe clock and reset operations. Per Absolute Maximum Ratings on Page 22, combinations of CLKIN and clock multipliers must not result in core/system clocks exceeding the maximum limits allowed for the processor, including system clock restrictions related to supply voltage.

Table 16. Clock and Normal Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN (to PLL) Period[1, 2, 3]	25.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse	10.0		ns
t_{CKINH}	CLKIN High Pulse	10.0		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[4]	$11 \times t_{CKIN}$		ns

[1] If DF bit in PLL_CTL register is set t_{CLKIN} is divided by two before going to PLL, then the t_{CLKIN} maximum period is 50 ns and the t_{CLKIN} minimum period is 12.5 ns.
[2] Applies to PLL bypass mode and PLL nonbypass mode.
[3] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 9 on Page 20 through Table 12 on Page 21.
[4] Applies after power-up sequence is complete. See Table 17 and Figure 9 for power-up reset timing.

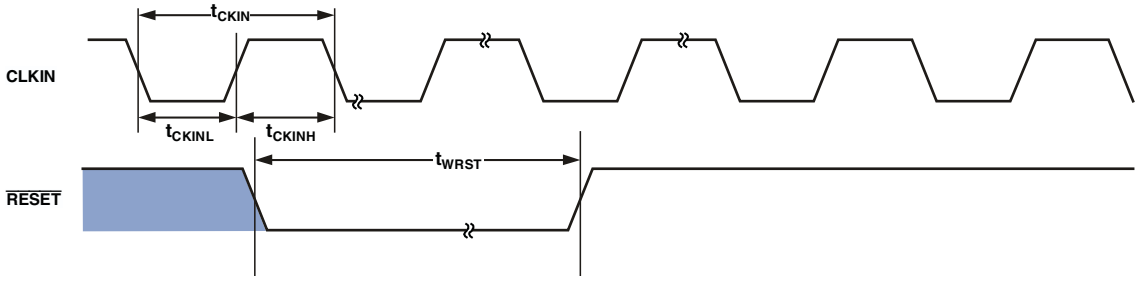

Figure 8. Clock and Normal Reset Timing

Table 17. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted after the V_{DDINT}, V_{DDEXT}, and CLKIN Pins are Stable and Within Specification	$3500 \times t_{CKIN}$		µs

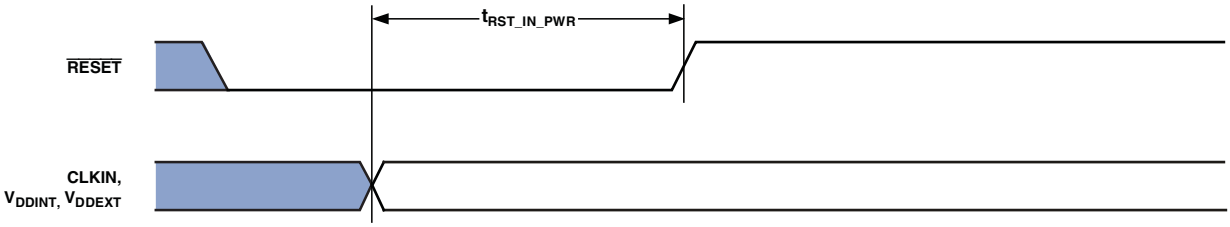

Figure 9. Power-Up Reset Timing

Asynchronous Memory Read Cycle Timing

Table 18. Asynchronous Memory Read Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA31–0 Setup Before CLKOUT	2.1		ns
t_{HDAT}	DATA31–0 Hold After CLKOUT	0.8		ns
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE3-0}$, ADDR25–2, $\overline{AOE}$, $\overline{ARE}$.

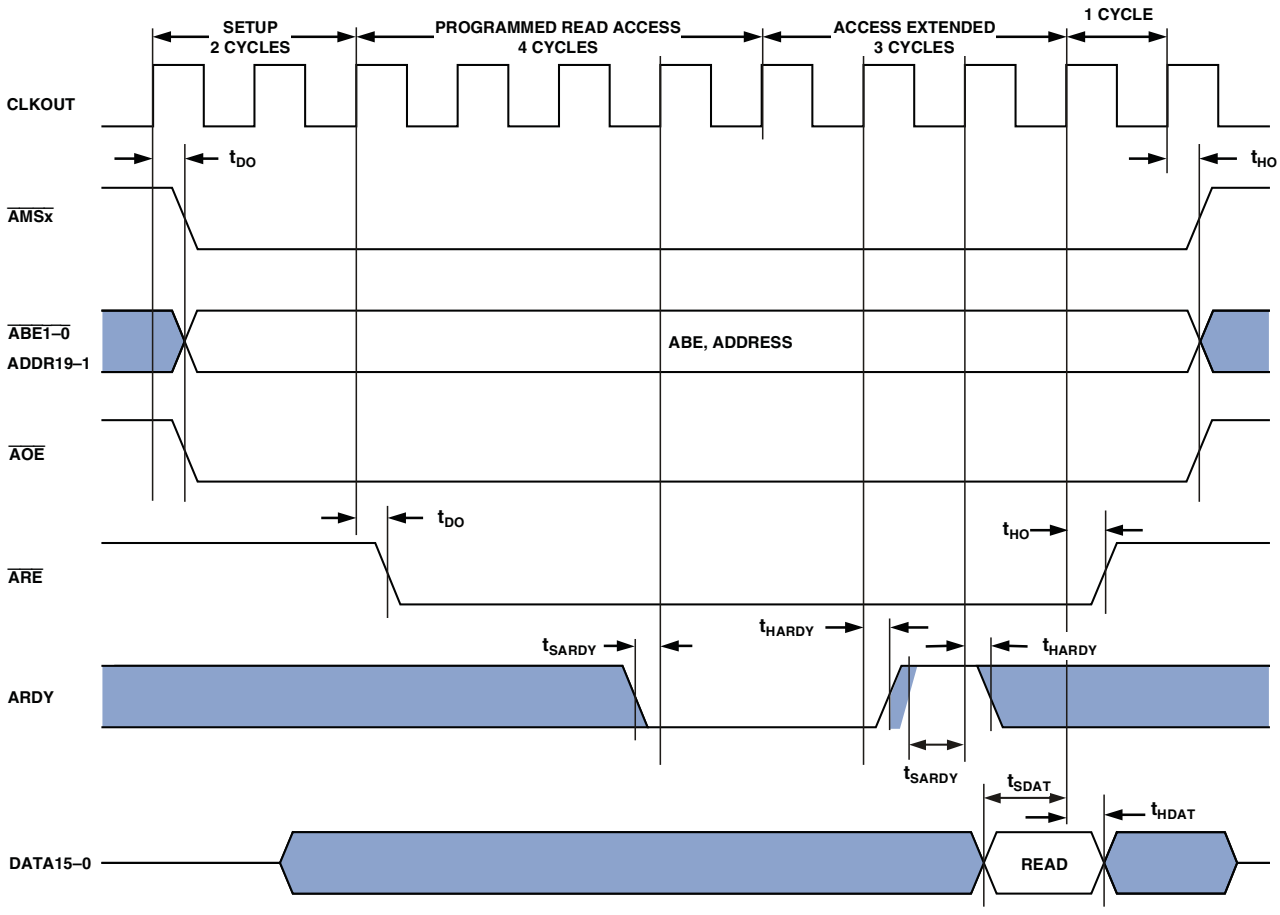

Figure 10. Asynchronous Memory Read Cycle Timing

External Port Bus Request and Grant Cycle Timing

Table 21 and Figure 13 describe external port bus request and bus grant operations.

Table 21. External Port Bus Request and Grant Cycle Timing

Parameter[1, 2]		Min	Max	Unit
Timing Requirements				
t_{BS}	$\overline{BR}$ Asserted to CLKOUT High Setup	4.6		ns
t_{BH}	CLKOUT High to $\overline{BR}$ Deasserted Hold Time	0.0		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{AMSx}$, Address and $\overline{ARE}$/$\overline{AWE}$ Disable		4.5	ns
t_{SE}	CLKOUT Low to $\overline{AMSx}$, Address and $\overline{ARE}$/$\overline{AWE}$ Enable		4.5	ns
t_{DBG}	CLKOUT High to $\overline{BG}$ Asserted Setup		3.6	ns
t_{EBG}	CLKOUT High to $\overline{BG}$ Deasserted Hold Time		3.6	ns
t_{DBH}	CLKOUT High to $\overline{BGH}$ Asserted Setup		3.6	ns
t_{EBH}	CLKOUT High to $\overline{BGH}$ Deasserted Hold Time		3.6	ns

[1] These are preliminary timing parameters that are based on worst-case operating conditions.
[2] The pad loads for these timing parameters are 20 pF.

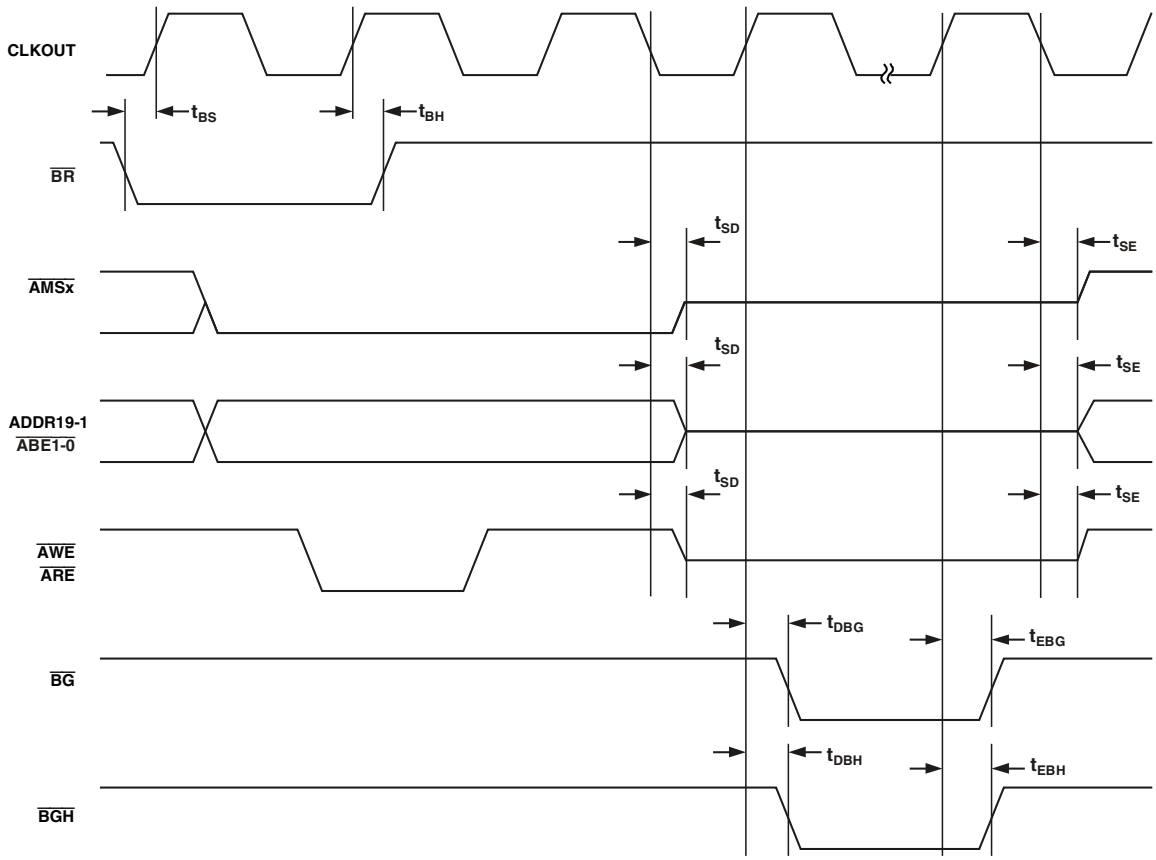

Figure 13. External Port Bus Request and Grant Cycle Timing

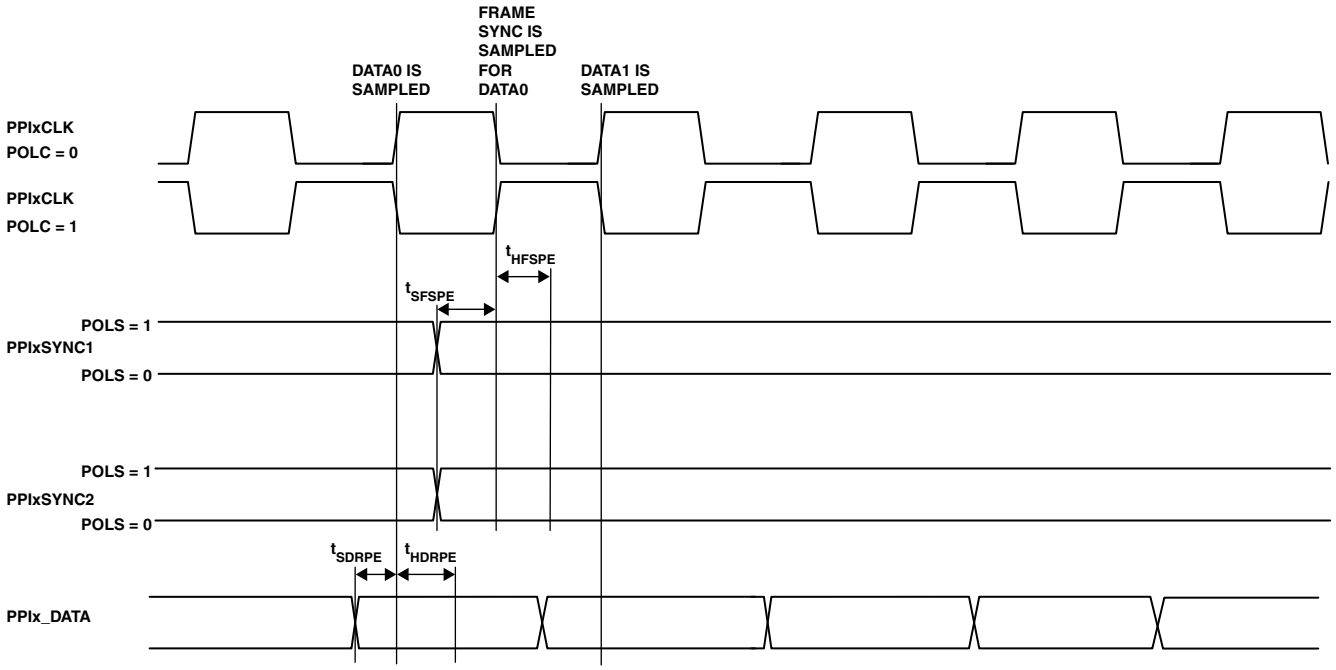

Figure 15. PPI GP Rx Mode with External Frame Sync Timing (Default)

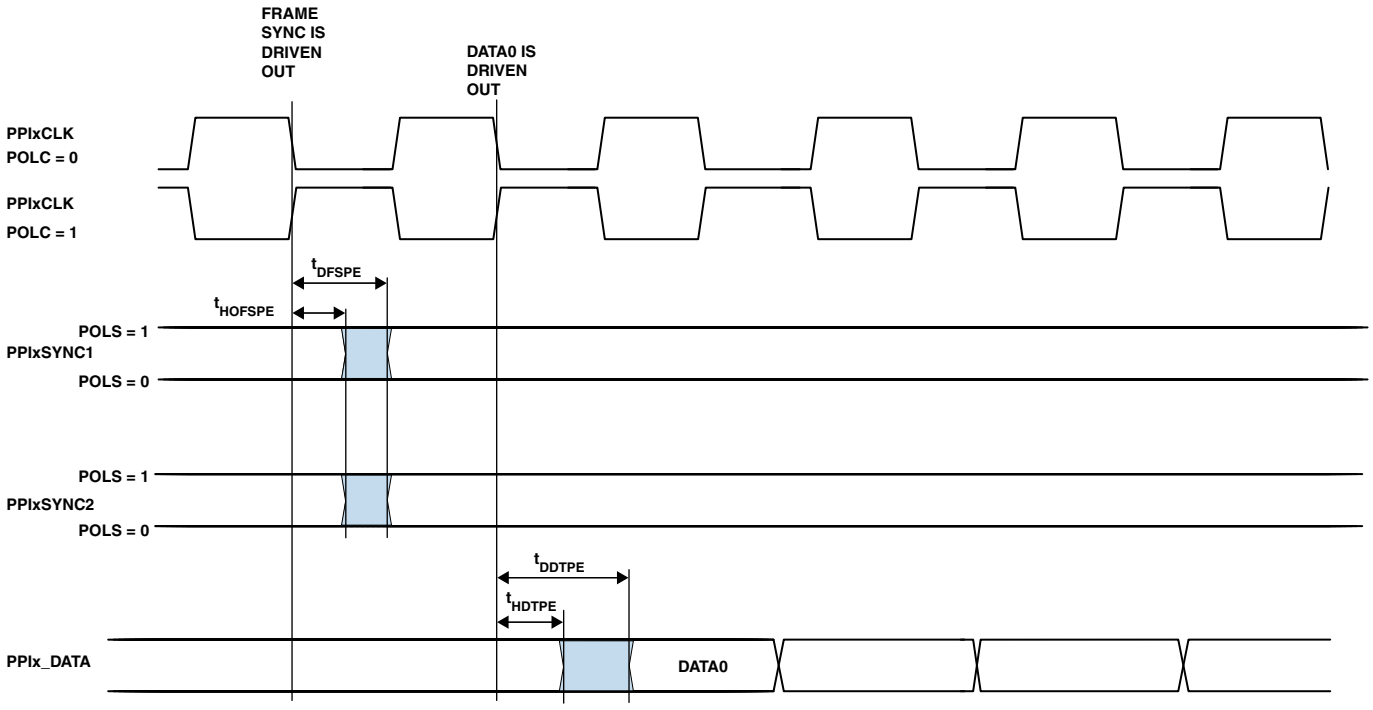

Figure 16. PPI GP Tx Mode with Internal Frame Sync Timing (Default)

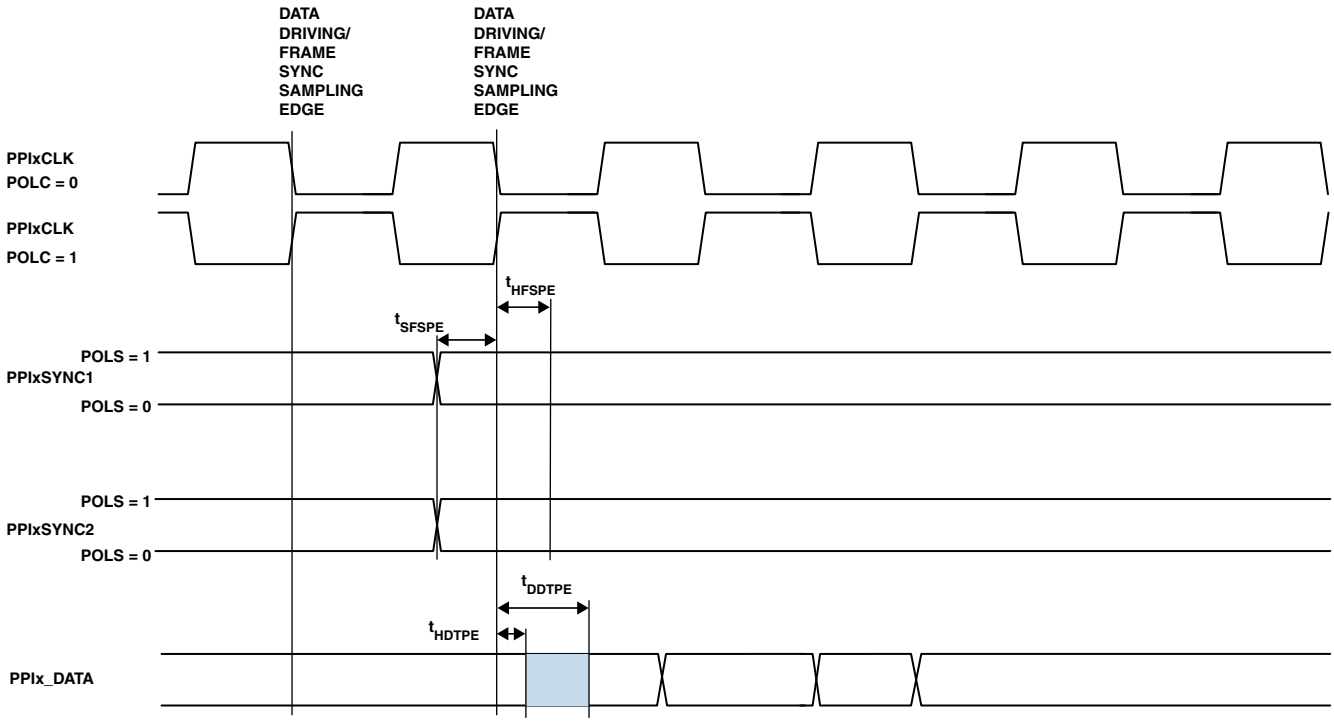

Figure 19. PPI GP Tx Mode with External Frame Sync Timing (Bit 4 of PLL_CTL Set)

Serial Peripheral Interface (SPI) Port— Master Timing

Table 27 and Figure 23 describe SPI port master operations.

Table 27. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	7.5		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	–1.5		ns
Switching Characteristics				
t_{SDSCIM}	$\overline{SPISELx}$ Low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISELx}$ High	$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)	0	6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	–1.0	+4.0	ns

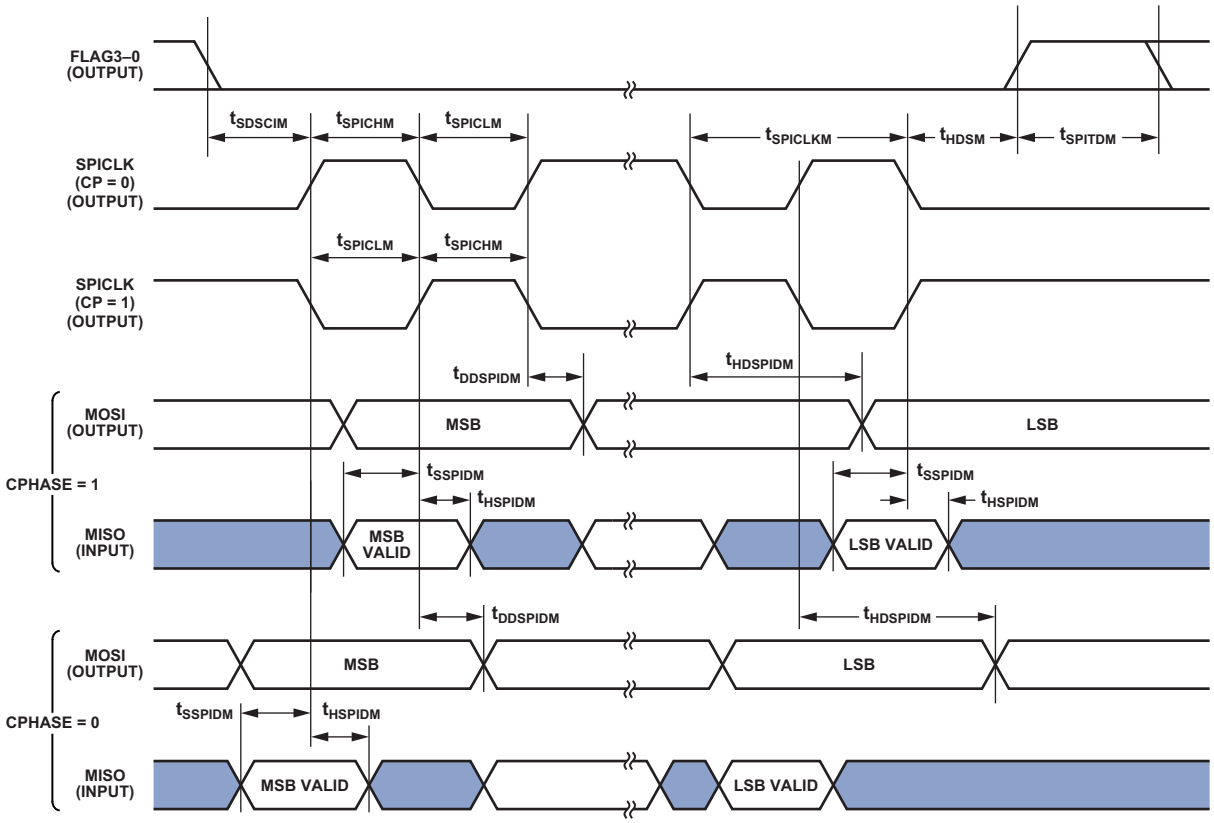

Figure 23. Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port— Slave Timing

Table 28 and Figure 24 describe SPI port slave operations.

Table 28. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	8	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0	8	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)	0	10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0	10	ns

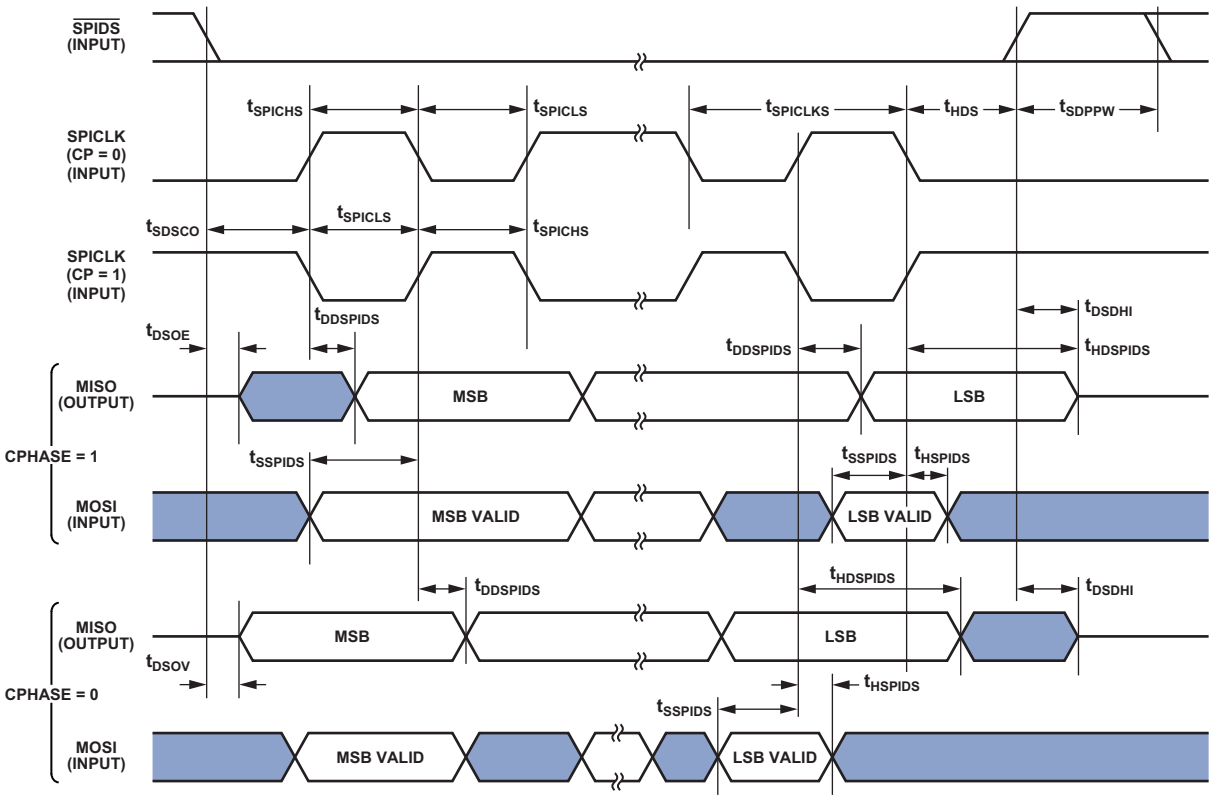

Figure 24. Serial Peripheral Interface (SPI) Port—Slave Timing

Programmable Flags Cycle Timing

Table 29 and Figure 26 describe programmable flag operations.

Table 29. Programmable Flags Cycle Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	Flag Input Pulse Width	t_{SCLK} + 1		ns
Switching Characteristic				
t_{DFO}	Flag Output Delay from CLKOUT Low		6	ns

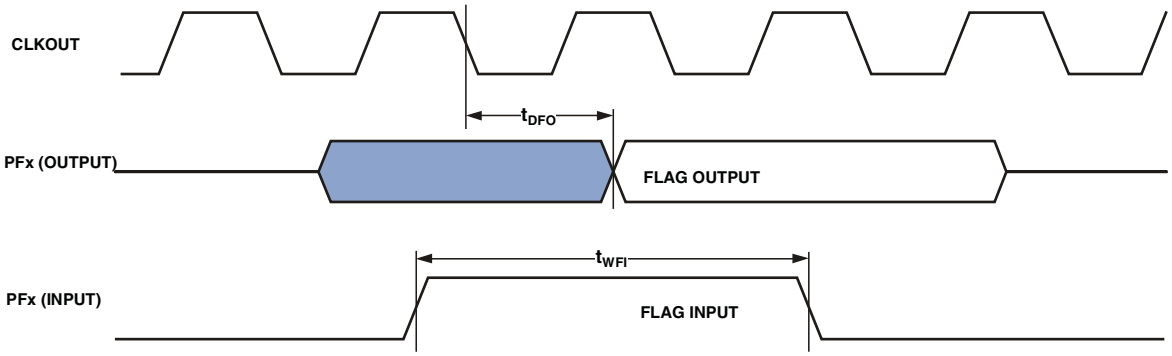

Figure 26. Programmable Flags Cycle Timing

Timer Cycle Timing

Table 30 and Figure 27 describe timer expired operations. The input signal is asynchronous in width capture mode and external clock mode and has an absolute maximum input frequency of $f_{SCLK}/2$ MHz.

Table 30. Timer Cycle Timing

Parameter		Min	Max	Unit
Timing Characteristics				
t_{WL}	Timer Pulse Width Input Low[1] (Measured in SCLK Cycles)	1		SCLK
t_{WH}	Timer Pulse Width Input High[1] (Measured in SCLK Cycles)	1		SCLK
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output[2] (Measured in SCLK Cycles)	1	$(2^{32}-1)$	SCLK

[1] The minimum pulse widths apply for TMRx input pins in width capture and external clock modes. They also apply to the PF1 or PPIxCLK input pins in PWM output mode.
[2] The minimum time for t_{HTO} is one cycle, and the maximum time for t_{HTO} equals $(2^{32}-1)$ cycles.

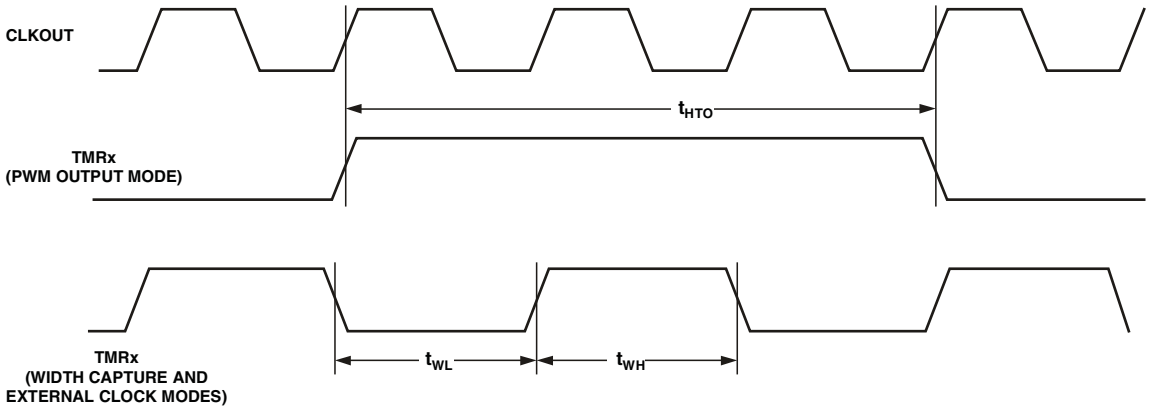

Figure 27. Timer PWM_OUT Cycle Timing

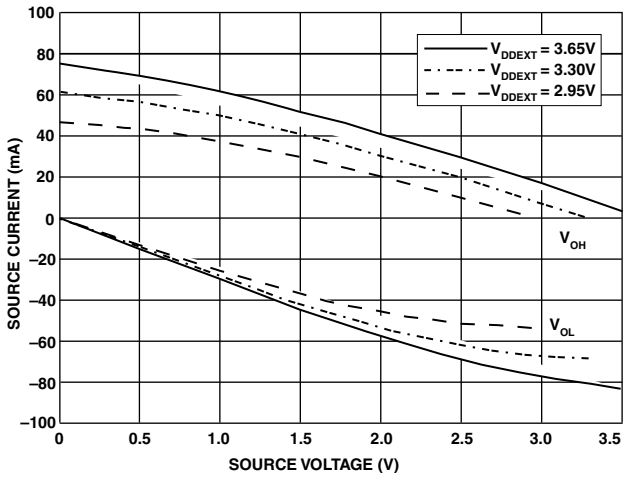

Figure 34. Drive Current C (High V_{DDEXT})

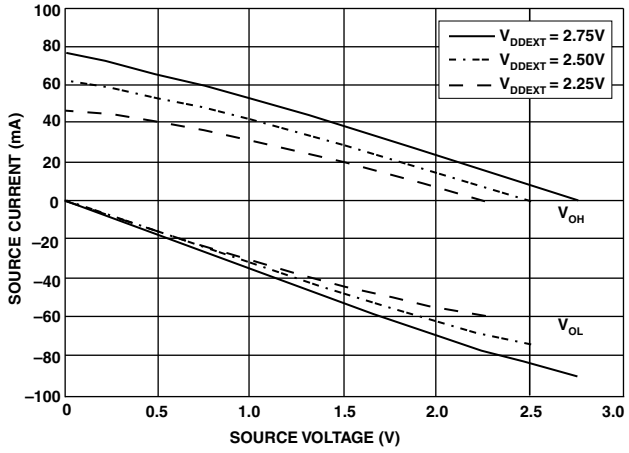

Figure 35. Drive Current D (Low V_{DDEXT})

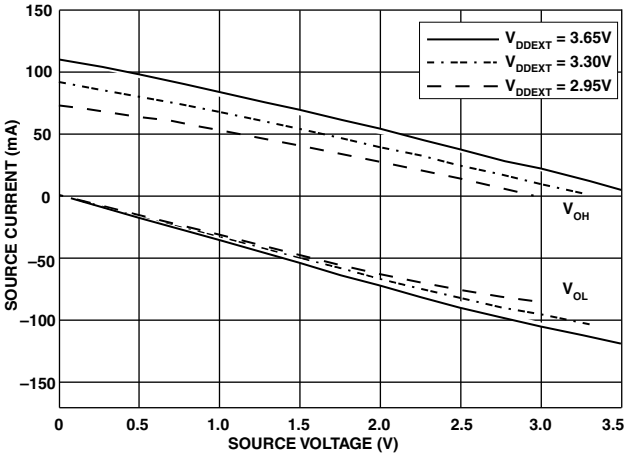

Figure 36. Drive Current D (High V_{DDEXT})

POWER DISSIPATION

Many operating conditions can affect power dissipation. System designers should refer to *Estimating Power for ADSP-BF561 Blackfin Processors (EE-293)* on the Analog Devices website (www.analog.com)—use site search on "EE-293." This document provides detailed information for optimizing your design for lowest power.

See the *ADSP-BF561 Blackfin Processor Hardware Reference Manual* for definitions of the various operating modes and for instructions on how to minimize system power.

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 37 shows the measurement point for ac measurements (except output enable/disable). The measurement point V_{MEAS} is 1.5 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V.

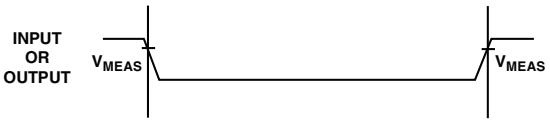

Figure 37. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving.

The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown on the right side of Figure 38 on Page 43.

The time $t_{ENA\_MEASURED}$ is the interval, from when the reference signal switches, to when the output voltage reaches V_{TRIP}(high) or V_{TRIP}(low). V_{TRIP}(high) is 2.0 V and V_{TRIP}(low) is 1.0 V for V_{DDEXT} (nominal) = 2.5 V/3.3 V. Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the V_{TRIP}(high) or V_{TRIP}(low) trip voltage.

Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time Measurement

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown on the left side of Figure 38 on Page 43.

$$t_{DIS} = t_{DIS\_MEASURED} - t_{DECAY}$$

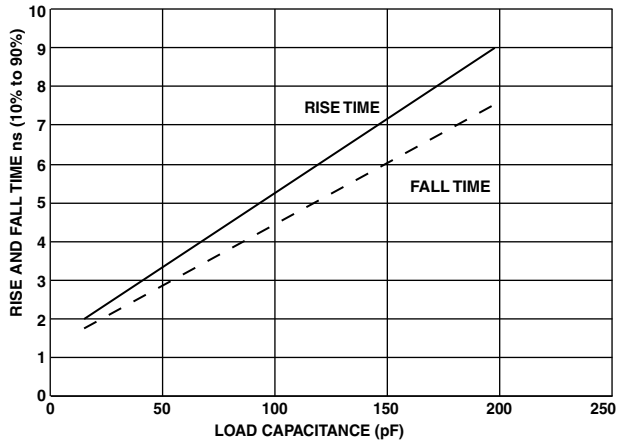

Figure 43. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver B at V_{DDEXT} (max)

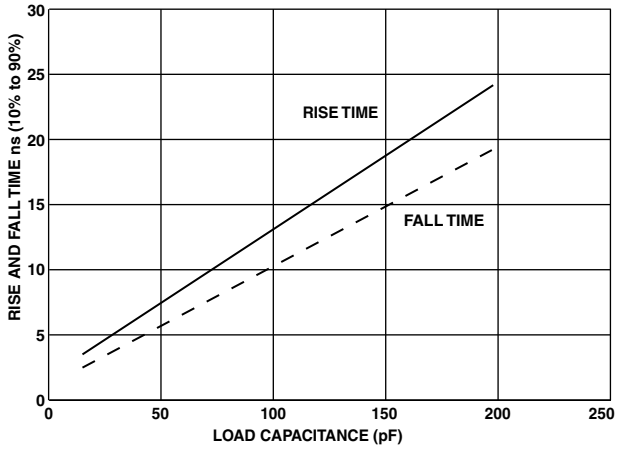

Figure 44. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver C at V_{DDEXT} (min)

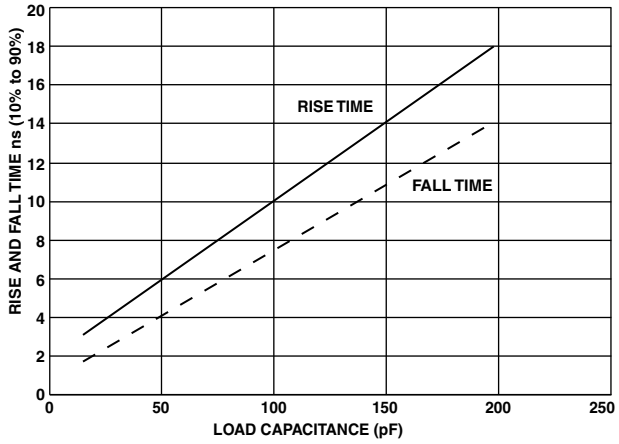

Figure 45. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver C at V_{DDEXT} (max)

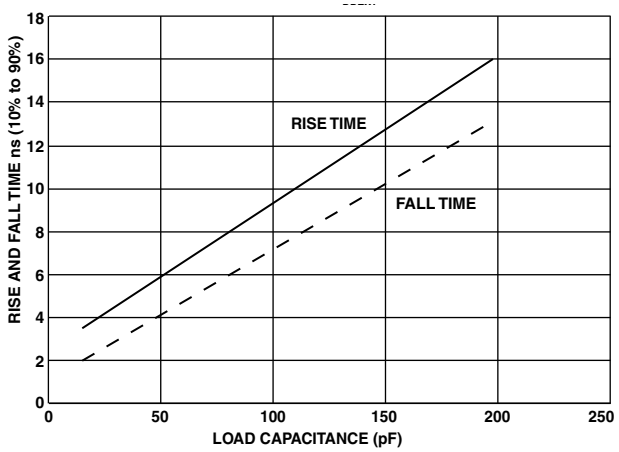

Figure 46. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver D at V_{DDEXT} (min)

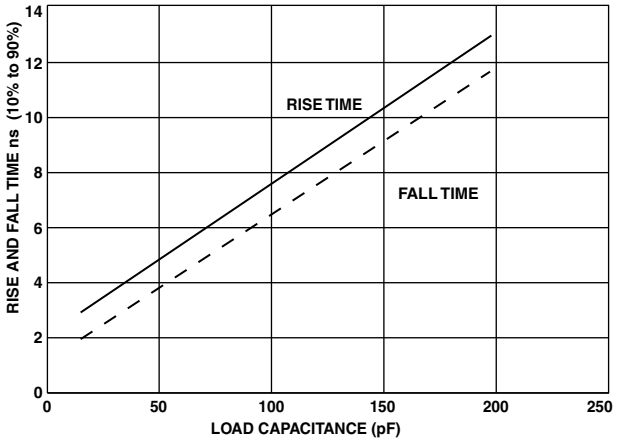

Figure 47. Typical Rise and Fall Times (10% to 90%) versus Load Capacitance for Driver D at V_{DDEXT} (max)

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:
T_J = junction temperature (°C).

T_{CASE} = case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = from Table 32 on Page 45 through Table 34 on Page 45.

P_D = power dissipation (see Power Dissipation on Page 42 for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:
T_A = ambient temperature (°C).

In Table 32 through Table 34, airflow measurements comply with JEDEC standards JESD51–2 and JESD51–6, and the junction-to-board measurement complies with JESD51–8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Thermal resistance θ_{JA} in Table 32 through Table 34 is the figure of merit relating to performance of the package and board in a convective environment. θ_{JMA} represents the thermal resistance under two conditions of airflow. θ_{JB} represents the heat extracted from the periphery of the board. Ψ_{JT} represents the correlation between T_J and T_{CASE}. Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

Table 32. Thermal Characteristics for BC-256-4 (17 mm × 17 mm) Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	18.1	°C/W
θ_{JMA}	1 Linear m/s Airflow	15.9	°C/W
θ_{JMA}	2 Linear m/s Airflow	15.1	°C/W
θ_{JC}	Not Applicable	3.72	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.11	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.18	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.18	°C/W

Table 33. Thermal Characteristics for BC-256-1 (12 mm × 12 mm) Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	25.6	°C/W
θ_{JMA}	1 Linear m/s Airflow	22.4	°C/W
θ_{JMA}	2 Linear m/s Airflow	21.6	°C/W
θ_{JB}	Not Applicable	18.9	°C/W
θ_{JC}	Not Applicable	4.85	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.15	°C/W
Ψ_{JT}	1 Linear m/s Airflow	n/a	°C/W
Ψ_{JT}	2 Linear m/s Airflow	n/a	°C/W

Table 34. Thermal Characteristics for B-297 Package

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	20.6	°C/W
θ_{JMA}	1 Linear m/s Airflow	17.8	°C/W
θ_{JMA}	2 Linear m/s Airflow	17.4	°C/W
θ_{JB}	Not Applicable	16.3	°C/W
θ_{JC}	Not Applicable	7.15	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.37	°C/W
Ψ_{JT}	1 Linear m/s Airflow	n/a	°C/W
Ψ_{JT}	2 Linear m/s Airflow	n/a	°C/W

Figure 52 lists the top view of the 297-Ball PBGA ball configuration. Figure 53 lists the bottom view.

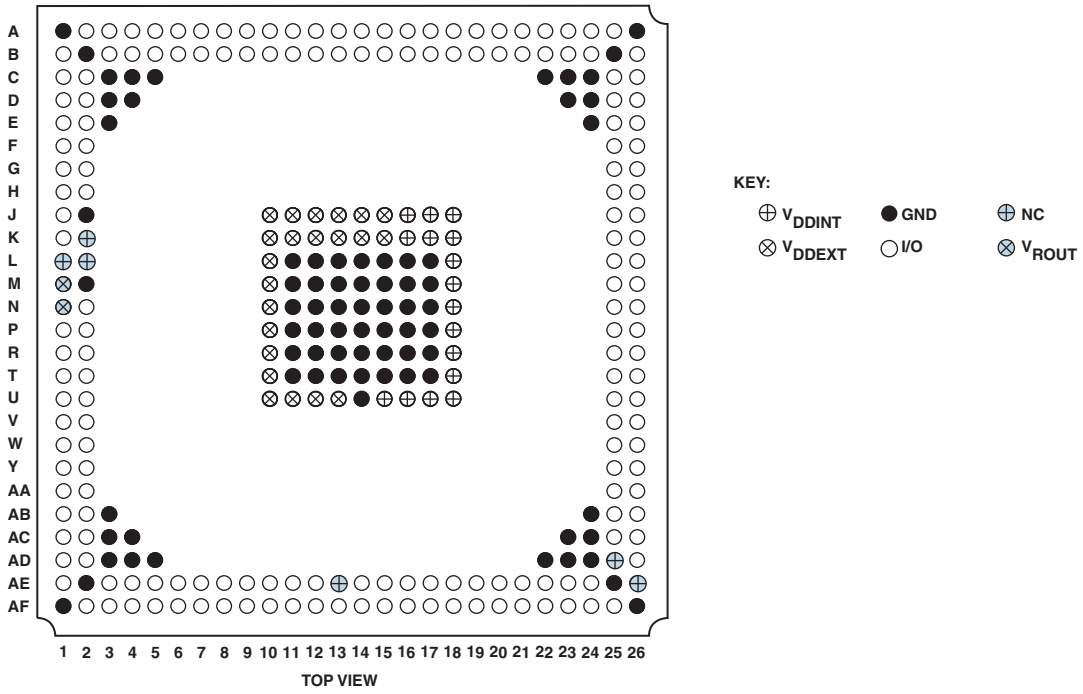

Figure 52. 297-Ball PBGA Ball Configuration (Top View)

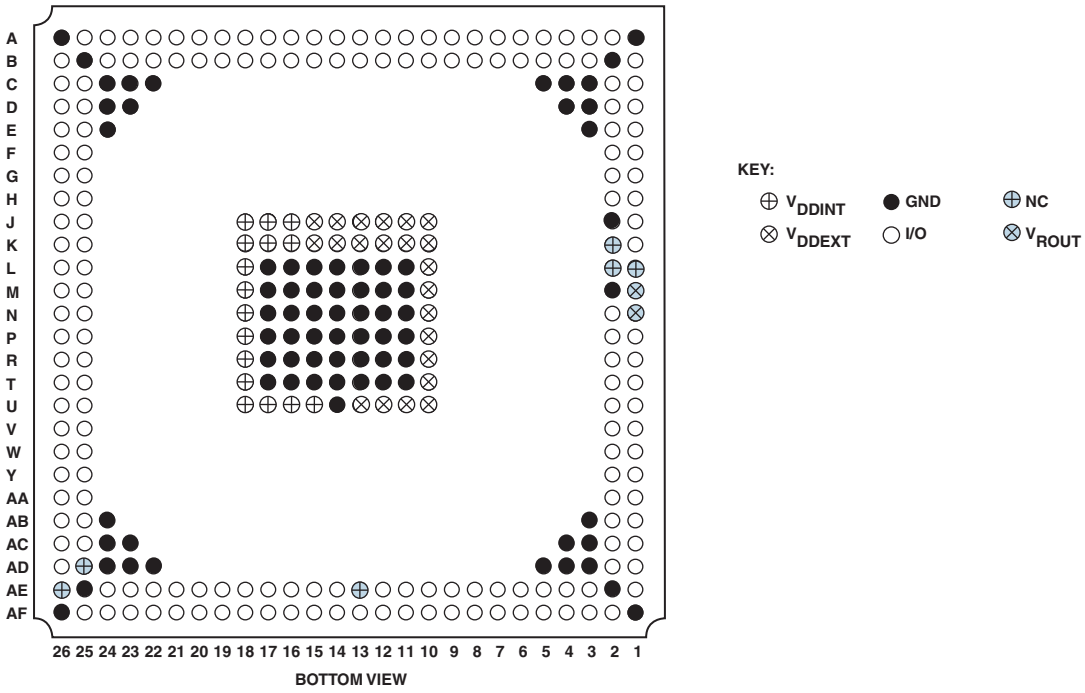

Figure 53. 297-Ball PBGA Ball Configuration (Bottom View)

OUTLINE DIMENSIONS

Dimensions in the outline dimension figures are shown in millimeters.

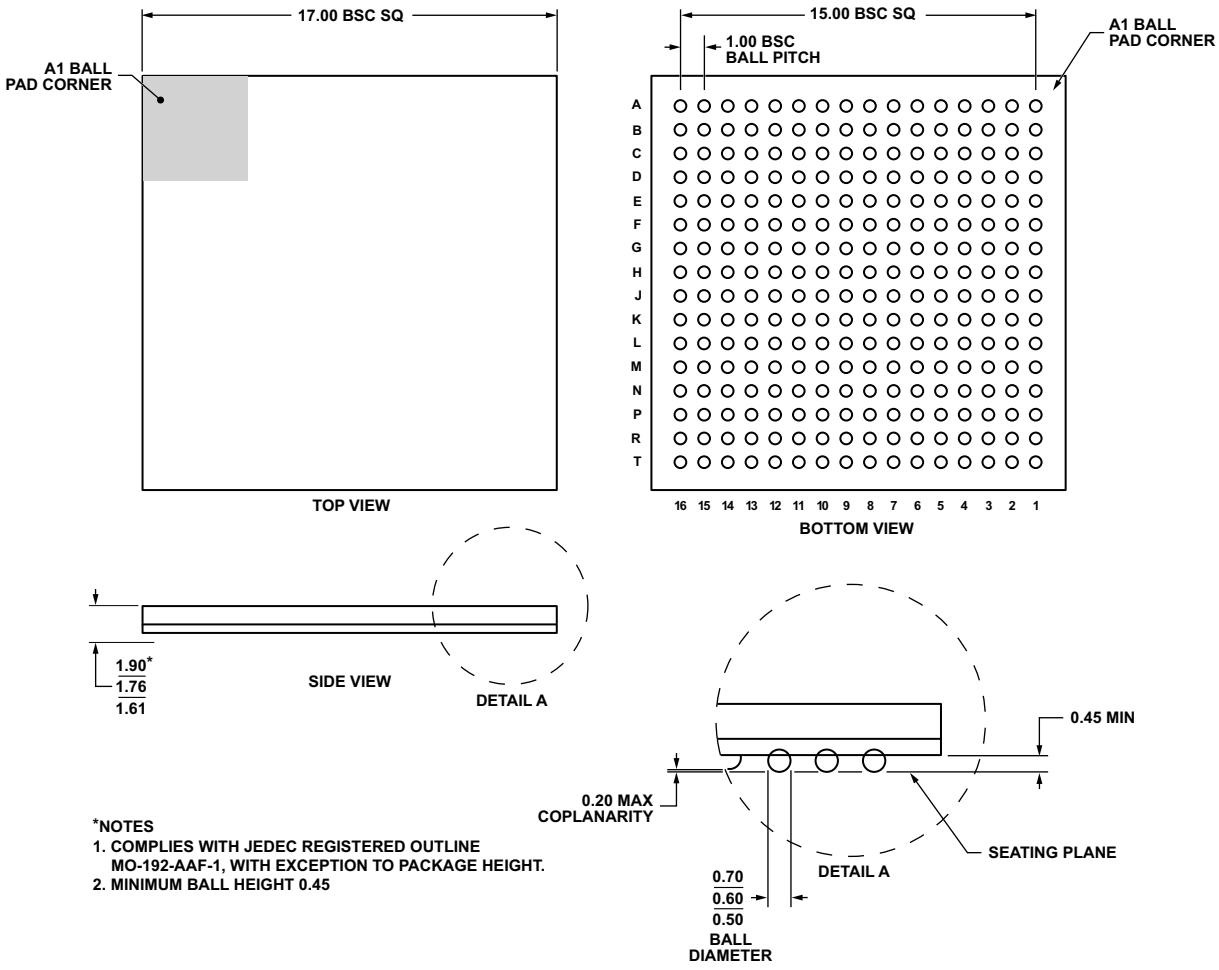

Figure 54. 256-Ball Chip Scale Package Ball Grid Array (CSP_BGA) (BC-256-4)