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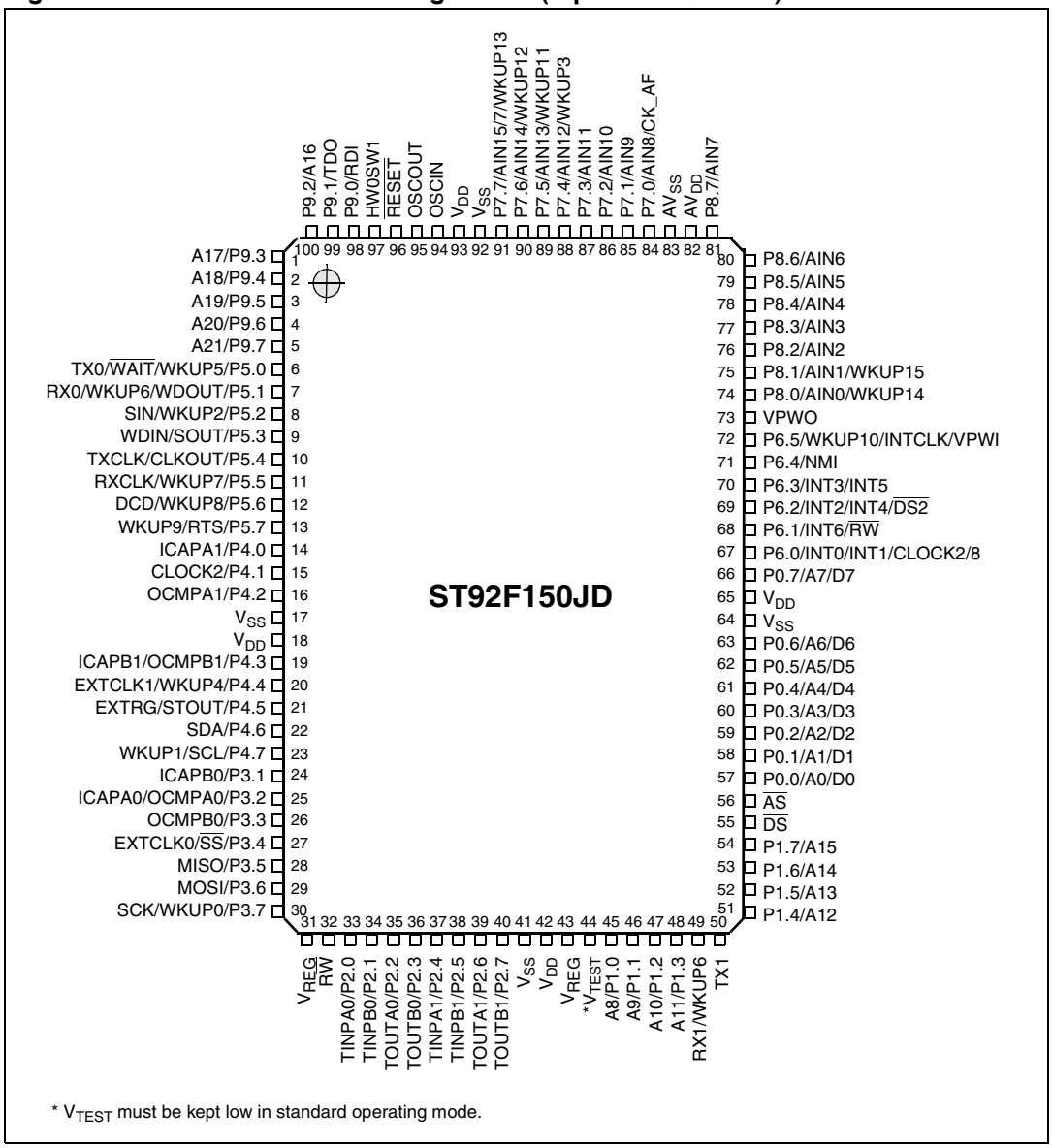
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST9
Core Size	8/16-Bit
Speed	24MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st92f124r9tb

Figure 11. ST92F150JD: Pin configuration (top-view PQFP100)



* V_{TEST} must be kept low in standard operating mode.

5 Operating modes

To optimize the performance versus the power consumption of the device, the ST92F124/F150/F250 supports different operating modes that can be dynamically selected depending on the performance and functionality requirements of the application at a given moment.

RUN MODE: This is the full speed execution mode with CPU and peripherals running at the maximum clock speed delivered by the Phase Locked Loop (PLL) of the Clock Control Unit (CCU).

SLOW MODE: Power consumption can be significantly reduced by running the CPU and the peripherals at reduced clock speed using the CPU Prescaler and CCU Clock Divider.

WAIT FOR INTERRUPT MODE: The Wait For Interrupt (WFI) instruction suspends program execution until an interrupt request is acknowledged. During WFI, the CPU clock is halted while the peripheral and interrupt controller keep running at a frequency depending on the CCU programming.

LOW POWER WAIT FOR INTERRUPT MODE: Combining SLOW mode and Wait For Interrupt mode, it is possible to reduce the power consumption by more than 80%.

STOP MODE: When the STOP is requested by executing the STOP bit writing sequence (see dedicated section on Wake-up Management Unit paragraph), and if NMI is kept low, the CPU and the peripherals stop operating. Operations resume after a wake-up line is activated (16 wake-up lines plus NMI pin). See the RCCU and Wake-up Management Unit paragraphs in the following for the details. The difference with the HALT mode consists in the way the CPU exits this state: when the STOP is executed, the status of the registers is recorded; and when the system exits from the STOP mode, the CPU continues the execution with the same status, without a system reset.

When the MCU enters STOP mode, the Watchdog stops counting. After the MCU exits from STOP mode, the Watchdog resumes counting from where it left off.

When the MCU exits from STOP mode, the oscillator, which was sleeping too, requires about 5 ms to restart working properly (at a 4 MHz oscillator frequency). An internal counter is present to guarantee that all operations after exiting STOP Mode, take place with the clock stabilized.

The counter is active only when the oscillation has already taken place. This means that 1-2 ms must be added to take into account the first phase of the oscillator restart.

In STOP mode, the oscillator is stopped. Therefore, if the PLL is used to provide the CPU clock before entering STOP mode, it will have to be selected again when the MCU exits STOP mode.

HALT MODE: When executing the HALT instruction, and if the Watchdog is not enabled, the CPU and its peripherals stop operating and the status of the machine remains frozen (the clock is also stopped). A reset is necessary to exit from Halt mode.

Register Group: E (System)
Reset Value: xxxx xx00 (xxh)

7							0
RG4	RG3	RG2	RG1	RG0	RPS	0	0

Bits 7:3 = **RG[4:0]**: *Register Group number.*
These bits contain the number (in the range 0 to 31) of the register block specified in the `srp0` or `srp` instructions. In single 16-register mode the number indicates the lower of the two 8-register blocks to which the 16 working registers are to be mapped, while in twin 8-register mode it indicates the 8-register block to which `r0` to `r7` are to be mapped.

Bit 2 = **RPS**: *Register Pointer Selector.*
This bit is set by the instructions `srp0` and `srp1` to indicate that the twin register pointing mode is selected. The bit is reset by the `srp` instruction to indicate that the single register pointing mode is selected.

0: Single register pointing mode

1: Twin register pointing mode

Bits 1:0: Reserved. Forced by hardware to zero.

POINTER 1 REGISTER (RP1)
R233 - Read/Write
Register Group: E (System)
Reset Value: xxxx xx00 (xxh)

7							0
RG4	RG3	RG2	RG1	RG0	RPS	0	0

This register is only used in the twin register pointing mode. When using the single register pointing mode, or when using only one of the twin register groups, the RP1 register must be considered as RESERVED and may NOT be used as a general purpose register.

Bits 7:3 = **RG[4:0]:** *Register Group number.* These bits contain the number (in the range 0 to 31) of the 8-register block specified in the `srp1` instruction, to which `r8` to `r15` are to be mapped.

Bit 2 = **RPS**: *Register Pointer Selector.*
This bit is set by the `srp0` and `srp1` instructions to indicate that the twin register pointing mode is selected. The bit is reset by the `srp` instruction to indicate that the single register pointing mode is selected.

0: Single register pointing mode

1: Twin register pointing mode

Bits 1:0: Reserved. Forced by hardware to zero.

9 Interrupts

9.1 Introduction

The ST9 responds to peripheral and external events through its interrupt channels. Current program execution can be suspended to allow the ST9 to execute a specific response routine when such an event occurs, providing that interrupts have been enabled, and according to a priority mechanism. If an event generates a valid interrupt request, the current program status is saved and control passes to the appropriate Interrupt Service Routine.

The ST9 CPU can receive requests from the following sources:

- On-chip peripherals
- External pins
- Top-Level Pseudo-non-maskable interrupt

9.1.1 On-chip peripheral interrupt sources

Dedicated Channels

The following on-chip peripherals have dedicated interrupt channels with interrupt control registers located in their peripheral register page.

- A/D Converter
- I^2C
- JPBLD
- MFT
- SCI-M

Standard Channels

Other on-chip peripherals have their interrupts mapped to the INTxx interrupt channel group. These channels have control registers located in Pages 0 and 60. These peripherals are:

- CAN
- E^3 TM/FLASH
- EFT Timer
- RCCU
- SCI-A
- SPI
- STIM timer
- WDT Timer
- WUIMU

External Interrupts

Up to eight external interrupts, with programmable input trigger edge, are available and are mapped to the INTxx interrupt channel group in page 0.

INTERRUPT PRIORITY LEVEL REGISTER LOW (SIPLRL)

R253 - Read/Write
Register Page: Page 60
Reset Value: 1111 1111

7							0
PL2H	PL1H	PL2G	PL1G	PL2F	PL1F	PL2E	PL1E

Bits 7:6 = **PL2H, PL1H:** *INTH0,H1 Priority Level.*

Bits 5:4 = **PL2G, PL1G**: *INTG0, G1 Priority Level.*

Bits 3:2 = **PL2F, PL1F**: *INTF0, F1 Priority Level.*

Bits 1:0 = **PL2E, PL1E**: *INTE0, E1 Priority Level.*

These bits are set and cleared by software.

The priority is a three-bit value. The LSB is fixed by hardware at 0 for even channels and at 1 for odd channels

Table 28. PL bit assignment

Interrupt channel pair	3-bit priority level		
INTH0	PL2H	PL1H	0
INTH1	PL2H	PL1H	1
INTG0	PL2G	PL1G	0
INTG1	PL2G	PL1G	1
INTF0	PL2F	PL1F	0
INTF1	PL2F	PL1F	1
INTE0	PL2E	PL1E	0
INTE1	PL2E	PL1E	1

Table 29. PL bit meaning

PL2x	PL1x	Hardware bit	Priority
0	0	0 1	0 (Highest) 1
0	1	0 1	2 3
1	0	0 1	4 5
1	1	0 1	6 7 (Lowest)

7							0
WUM7	WUM6	WUM5	WUM4	WUM3	WUM2	WUM1	WUM0

and WKUP-INT bits) are generated if the corresponding WUPx pending bit is set. More precisely, if WUMx=1 and WUPx=1 then:

- If ID1S=1 and WKUP-INT=1 then an interrupt on channel INTD1 and a wake-up event are generated.
- If ID1S=1 and WKUP-INT=0 only an interrupt on channel INTD1 is generated.

If WUMx is reset, no wake-up events can be generated.

WAKE-UP TRIGGER REGISTER HIGH (WUTRH)

R252 - Read/Write
Register Page: 57
Reset Value: 0000 0000 (00h)

7							0
WUT15	WUT14	WUT13	WUT12	WUT11	WUT10	WUT9	WUT8

Bit 7:0 = **WUT[15:8]:** *Wake-Up Trigger Polarity Bits*
These bits are set and cleared by software.

0: The corresponding WUPx pending bit will be set on the falling edge of the input wake-up line.

1: The corresponding WUPx pending bit will be set on the rising edge of the input wake-up line.

WAKE-UP TRIGGER REGISTER LOW (WUTRL)

R253 - Read/Write
Register Page: 57
Reset Value: 0000 0000 (00h)

7							0
WUT7	WUT6	WUT5	WUT4	WUT3	WUT2	WUT1	WUT0

Bit 7:0 = **WUT[7:0]:** *Wake-Up Trigger Polarity Bits*
These bits are set and cleared by software.

0: The corresponding WUPx pending bit will be set on the falling edge of the input wake-up line.

1: The corresponding WUPx pending bit will be set on the rising edge of the input wake-up line.

Warning

1. As the external wake-up lines are edge triggered, no glitches must be generated on these lines.
2. If either a rising or a falling edge on the external wake-up lines occurs while writing the WUTRLH or WUTRL registers, the pending bit will not be set.

$\overline{DS2}$ is released in high-impedance during bus acknowledge cycle or under processor control by setting the HIMP bit (MODER.0, r235).

The behavior of this signal is also affected by the DS2EN bit in the EMR1 register. Refer to the Register description.

12.2.5 PORT 0

If Port 0 is used as a bit programmable parallel I/O port, it has the same features as a regular port. When set as an Alternate Function, it is used as the External Memory interface: it outputs the multiplexed Address (8 LSB: A[7:0]) / Data bus D[7:0].

12.2.6 PORT 1

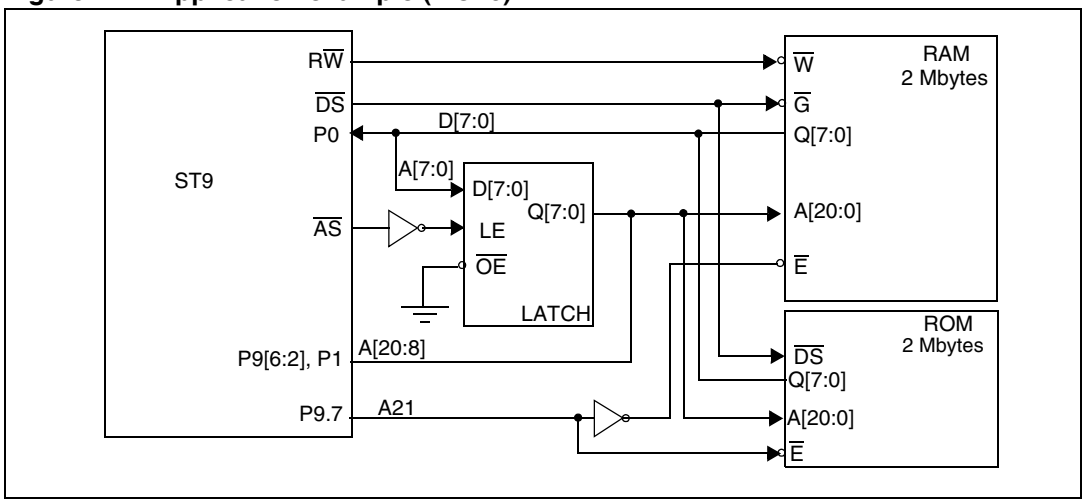
If Port 1 is used as a bit programmable parallel I/O port, it has the same features as a regular port. When set as an Alternate Function, it is used as the external memory interface to provide the address bits A[15:8].

12.2.7 PORT 9 [7:2]

If Port 9 is available and used as a bit programmable I/O port, it has the same features as a regular port. If the MMU is available on the device and Port 9 is set as an Alternate Function, Port 9[7:2] is used as the external memory interface to provide the 6 MSB of the address (A[21:16]).

Note: For the ST92F250 device, since A[18:17] share the same pins as SDA1 and SCL1 of I²C_1, these address bits are not available when the I²C_1 is in use (when I2CCR.PE bit is set).

Figure 74. Application example (MC=0)



Gated input mode

This mode can be used for pulse width measurement. The Timer is clocked by INTCLK/4, and is started and stopped by means of the input pin and the ST_SP bit. When the input pin is high, the Timer counts. When it is low, counting stops. The maximum input pin frequency is equivalent to INTCLK/8.

Triggerable input mode

The Timer (clocked internally by INTCLK/4) is started by the following sequence:

- setting the Start-Stop bit, followed by
- a High to Low transition on the input pin.

To stop the Timer, reset the ST_SP bit.

Retriggerable input mode

In this mode, the Timer (clocked internally by INTCLK/4) is started by setting the ST_SP bit. A High to Low transition on the input pin causes counting to restart from the initial value. When the Timer is stopped (ST_SP bit reset), a High to Low transition of the input pin has no effect.

Timer/counter output modes

Output modes are selected by means of the OUTEN (Output Enable) and OUTMD (Output Mode) bits of the WDTCR register.

No output mode
(OUTEN = “0”)

The output is disabled and the corresponding pin is set high, in order to allow other alternate functions to use the I/O pin.

Square wave output mode
(OUTEN = “1”, OUTMD = “0”)

The Timer outputs a signal with a frequency equal to half the End of Count repetition rate on the WDOUT pin. With an INTCLK frequency of 20MHz, this allows a square wave signal to be generated whose period can range from 400ns to 6.7 seconds.

Pulse width modulated output mode
(OUTEN = “1”, OUTMD = “1”)

The state of the WROUT bit is transferred to the output pin (WDOUT) at the End of Count, and is held until the next End of Count condition. The user can thus generate PWM signals by modifying the status of the WROUT pin between End of Count events, based on software counters decremented by the Timer Watchdog interrupt.

14.1.3 Watchdog timer operation

This mode is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence of operation. The Watchdog, when enabled, resets the MCU, unless the program executes the correct write sequence before expiry of the programmed time period. The application program must be designed so as to correctly write to the WDTLR Watchdog register at regular intervals during all phases of normal operation.

WDTCR: Timer/Watchdog Control Register

Three additional control bits are mapped in the following registers on Page 0:

Watchdog Mode Enable, (WCR.6)

Top Level Interrupt Selection, (EIVR.2)

Interrupt A0 Channel Selection, (EIVR.1)

Note: The registers containing these bits also contain other functions. Only the bits relevant to the operation of the Timer/Watchdog are shown here.

Counter Register

This 16-bit register (WDTLR, WDTHR) is used to load the 16-bit counter value. The registers can be read or written “on the fly”.

TIMER/WATCHDOG HIGH REGISTER (WDTHR)
R248 - Read/Write
Register Page: 0
Reset value: 1111 1111 (FFh)

7							0
R15	R14	R13	R12	R11	R10	R9	R8

Bits 7:0 = **R[15:8]** *Counter Most Significant Bits*.

TIMER/WATCHDOG LOW REGISTER (WDTLR)
R249 - Read/Write
Register Page: 0
Reset value: 1111 1111b (FFh)

7							0
R7	R6	R5	R4	R3	R2	R1	R0

Bits 7:0 = **R[7:0]** *Counter Least Significant Bits.*

TIMER/WATCHDOG PRESCALER REGISTER (WDTPR)
R250 - Read/Write
Register Page: 0
Reset value: 1111 1111 (FFh)

7							0
PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0

Bits 7:0 = **PR[7:0]** *Prescaler value.*
A programmable value from 1 (00h) to 256 (FFh).

Note: *Bit 5 = **DCTS**: DMA capture transfer source.*
This bit is set and cleared by software. It selects the source of the DMA operation related to the channel associated with the Capture 0.
The I/O port source is available only on specific devices.

0: REG0R register

1: I/O port.

Bit 4 = **DCTD**: DMA compare transfer destination.
This bit is set and cleared by software. It selects the destination of the DMA operation related to the channel associated with Compare 0.
The I/O port destination is available only on specific devices.

0: CMP0R register

1: I/O port

Bit 3 = **SWEN**: *Swap function enable*.
This bit is set and cleared by software.

0: Disable Swap mode

1: Enable Swap mode for both DMA channels.

Bits 2:0 = **PL[2:0]:** *Interrupt/DMA priority level*.
With these three bits it is possible to select the Interrupt and DMA priority level of each timer, as one of eight levels (see Interrupt/DMA chapter).

I/O CONNECTION REGISTER (IOCR)

R248 - Read/Write
Register Page: 9
Reset value: 1111 1100 (FCh)

7							0
						SC1	SC0

Bits 7:2 = not used.

Bit 1 = **SC1**: *Select connection odd.*
This bit is set and cleared by software. It selects if the TxOUTA and TxINA pins for Timer 1 and Timer 3 are connected on-chip or not.

0: T1OUTA / T1INA and T3OUTA/ T3INA unconnected

1: T1OUTA connected internally to T1INA and T3OUTA connected internally to T3INA

Bit 0 = **SC0**: *Select connection even.*
This bit is set and cleared by software. It selects if the TxOUTA and TxINA pins for Timer 0 and Timer 2 are connected on-chip or not.

Bit 0 = **TXDI**: *Transmitter Data Interrupt Mask*.

0: Disable Transmitter Buffer Register Empty, Transmitter Shift Register Empty, or Transmitter End of Block interrupts (TXBEM, TXSEM, and TXEOB bits in the S_ISR register).

1: Enable Transmitter Buffer Register Empty, Transmitter Shift Register Empty, or Transmitter End of Block interrupts.

Note: TXDI has no effect on DMA transfers.

INTERRUPT STATUS REGISTER (S_ISR)

R247 - Read/Write

Reset value: undefined

7							0
OE	FE	PE	RXAP	RXBP	RXDP	TXBEM	TXSEM

Bit 7 = **OE**: *Overrun Error Pending*.
This bit is set by hardware if the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register (the previous data is lost).
0: No Overrun Error.
1: Overrun Error occurred.

Bit 6 = **FE**: *Framing Error Pending bit*.
This bit is set by hardware if the received data word did not have a valid stop bit.
0: No Framing Error.
1: Framing Error occurred.

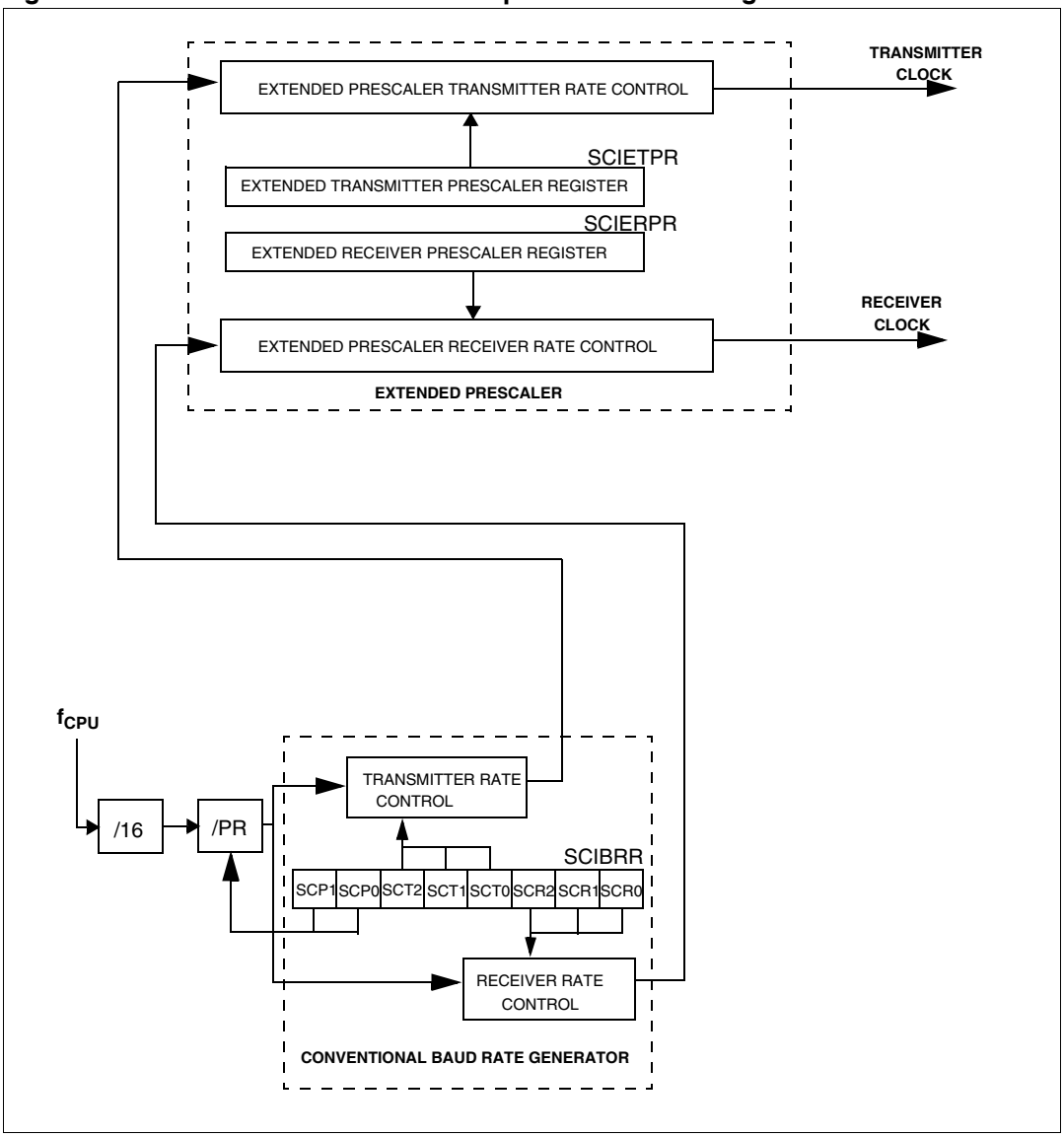
Note: In the case where a framing error occurs when the SCI is programmed in address mode and is monitoring an address, the interrupt is asserted and the corrupted data element is transferred to the Receiver Buffer Register.

Bit 5 = **PE**: *Parity Error Pending*.
This bit is set by hardware if the received word did not have the correct even or odd parity bit.
0: No Parity Error.
1: Parity Error occurred.

Bit 4 = **RXAP**: *Receiver Address Pending*.
RXAP is set by hardware after an interrupt acknowledged in the address mode.
0: No interrupt in address mode.
1: Interrupt in address mode occurred.

Note: The source of this interrupt is given by the couple of bits (AMEN, AM) as detailed in the IDPR register description.

Figure 133. SCI baud rate and extended prescaler block diagram



Conventional baud rate generation

The baud rate for the receiver and transmitter (Rx and Tx) are set independently and calculated as follows:

$$Tx = \frac{f_{CPU}}{(16*PR)*TR} \qquad Rx = \frac{f_{CPU}}{(16*PR)*RR}$$

with:

PR = 1, 3, 4 or 13 (see SCP[1:0] bits)

TR = 1, 2, 4, 8, 16, 32, 64,128

(see SCT[2:0] bits)

RR = 1, 2, 4, 8, 16, 32, 64,128

Note: Data will not be transferred to the shift register as long as the TDRE bit is not reset.

Bit 6 = TC *Transmission complete.*
This bit is set by hardware when transmission of a frame containing Data, a Preamble or a Break is complete. An interrupt is generated if TCIE=1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a write to the SCIDR register).

0: Transmission is not complete

1: Transmission is complete

Bit 5 = RDRF *Received data ready flag.*
This bit is set by hardware when the content of the RDR register has been transferred into the SCIDR register. An interrupt is generated if RIE=1 in the SCICR2 register. It is cleared by hardware when RE=0 or by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).

0: Data is not received

1: Received data is ready to be read

Bit 4 = IDLE *Idle line detect.*
This bit is set by hardware when a Idle Line is detected. An interrupt is generated if the ILIE=1 in the SCICR2 register. It is cleared by hardware when RE=0 by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).

0: No Idle Line is detected

1: Idle Line is detected

Note: The IDLE bit will not be set again until the RDRF bit has been set itself (i.e. a new idle line occurs). This bit is not set by an idle line when the receiver wakes up from wake-up mode.

Bit 3 = **OR** *Overrun error.*
This bit is set by hardware when the word currently being received in the shift register is ready to be transferred into the RDR register while RDRF=1. An interrupt is generated if RIE=1 in the SCICR2 register. It is cleared by hardware when RE=0 by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).

0: No Overrun error

1: Overrun error is detected

Note: When this bit is set RDR register content will not be lost but the shift register will be overwritten.

Bit 2 = NF *Noise flag.*
This bit is set by hardware when noise is detected on a received frame. It is cleared by hardware when RE=0 by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).

0: No noise is detected

Bit 1 = **IFD** *Invalid Frame Detect*
The IFD bit gets set when the following conditions are detected from the filtered VPWI pin:

- An SOF symbol is received after an EOD minimum, but before an EOF minimum.
- An SOF symbol is received when expecting data bits.
- If NFL = 0 and a message frame greater than 12 bytes (i.e. 12 bytes plus one bit) has been received in one frame.
- An EOD minimum time has elapsed when data bits are expected.
- A logic 0 or 1 symbol is received (active for Tv1 or Tv2) when an SOF was expected.
- The second EODM symbol received in a frame is NOT followed directly by an EOFM symbol.

IFD errors are inhibited if the JBLPD peripheral is in the “sleep or filter and NOT presently transmitting” mode. An IFD error occurs once for a frame. Afterwards, the receiver is disabled until an EOFM symbol is received, and queued transmits for the present frame are cancelled (but the TRA bit is not set). IFD is cleared when ERROR is read. It is also cleared while the CONTROL.JE bit is reset or while the CONTROL.JDIS bit is set or on reset.

0: No invalid frame detected

1: Invalid frame detected

Bit 0 = **IBD** *Invalid Bit Detect.*
The IBD bit gets set whenever the receiver detects that the filtered VPWI pin was not fixed in a state long enough to reach the minimum valid symbol time of Tv1 (or 35 µs). Any timing event less than 35 µs (and, of course, > 7 µs since the VPWI digital filter will not allow pulses less than this through its filter) is considered as noise and sets the IBD accordingly. At this point the JBLPD peripheral will cease transmitting and receiving any information until a valid EOF symbol is received.
IBD errors are inhibited if the JBLPD peripheral is in the “sleep or filter and NOT presently transmitting” mode. An IBD error occurs once for a frame. Afterwards, the receiver is disabled until an EOFM symbol is received, and queued transmits for the present frame are cancelled (but the TRA bit is not set).
IBD is cleared when ERROR is read. Note that if an invalid bit is detected during a bus idle condition, the IBD flag gets set and a new EOFmin must be seen after the invalid bit before commencing to receive again. IBD is also cleared while the CONTROL.JE bit is reset or while the CONTROL.JDIS bit is set and on reset.

0: No invalid bit detected

1: Invalid bit detected

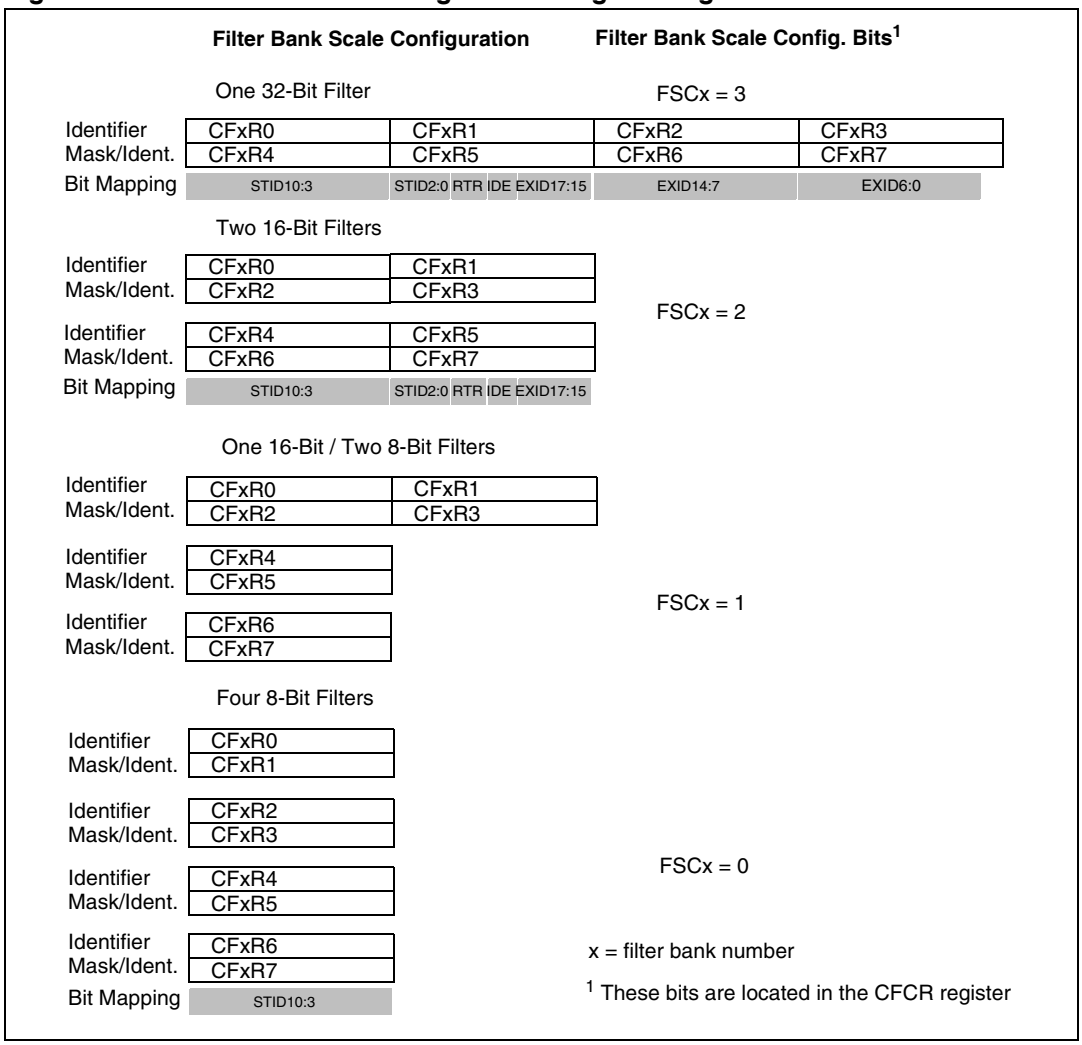
JBLPD INTERRUPT VECTOR REGISTER (IVR)

R248- Read/Write (except bits 2:1)
Register Page: 23
Reset Value: xxxx xxx0 (xxh)

7							0
V7	V6	V5	V4	V3	EV2	EV1	-

Bit 7:3 = **V[7:3]** *Interrupt Vector Base Address.*
User programmable interrupt vector bits.

Figure 163. Filter bank scale configuration - register organization



Filter Bank Scale and Mode Configuration

The filter banks are configured by means of the corresponding CFCRx register. To configure a filter bank it must be deactivated by clearing the FACT bit in the CFCR register. The filter scale is configured by means of the FSC[1:0] bits in the corresponding CFCR register, refer to *Figure 163*. The **identifier list** or **identifier mask** mode for the corresponding Mask/Identifier registers is configured by means of the FMCLx and FMCHx bits in the CFMR register. The FMCLx bit defines the mode for the two least significant bytes, and the FMCHx bit the mode for the two most significant bytes of filter bank x. Examples:

- If filter bank 1 is configured as two 16-bit filters, then the FMCL1 bit defines the mode of the CF1R2 and CF1R3 registers and the FMCH1 bit defines the mode of the CF1R6 and CF1R7 registers.
- If filter bank 2 is configured as four 8-bit filters, then the FMCL2 bit defines the mode of the CF2R1 and CF2R3 registers and the FMCH2 bit defines the mode of the CF2R5 and CF2R7 registers.

Note: In 32-bit configuration, the FMCLx and FMCHx bits must have the same value to ensure that the four Mask/Identifier registers are in the same mode.

CAN MASTER STATUS REGISTER (CMSR)

Note: Reset Value: 0000 0010 (02h)

7							0
0	0	REC	TRAN	WKUI	ERRI	SLAK	INAK

To clear a bit of this register the software must write this bit with a one.

Bit 7:4 = Reserved. Forced to 0 by hardware.

Bit 5 = **REC** *Receive*
- Read
The CAN hardware is currently receiver.

Bit 4 = **TRAN** *Transmit*
- Read
The CAN hardware is currently transmitter.

Bit 3 = **WKUI** *Wake-Up Interrupt*
- Read/Clear
This bit is set by hardware to signal that a SOF bit has been detected while the CAN hardware was in sleep mode. Setting this bit generates a status change interrupt if the WKUIE bit in the CIER register is set.

This bit is cleared by software.

Bit 2 = **ERRI** *Error Interrupt*
- Read/Clear
This bit is set by hardware when a bit of the CESR has been set on error detection and the corresponding interrupt in the CEIER is enabled. Setting this bit generates a status change interrupt if the ERRIE bit in the CIER register is set.

This bit is cleared by software.

Bit 1 = **SLAK** *Sleep Acknowledge*
- Read
This bit is set by hardware and indicates to the software that the CAN hardware is now in sleep mode. This bit acknowledges the sleep mode request from the software (set SLEEP bit in CMCR register).

This bit is cleared by hardware when the CAN hardware has left sleep mode. Sleep mode is left when the SLEEP bit in the CMCR register is cleared. Please refer to the AWUM bit of the CMCR register description for detailed information for clearing SLEEP bit.

Bit 0 = **INAK** *Initialization Acknowledge*
- Read

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be improved to prevent unrecoverable errors occurring (see application note AN1015).

Table 114. Susceptibilty tests

Symbol	Parameter	Conditions	Level	Unit
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5V, T_A=+25°C, f_{OSC}=4MHz conforms to IEC 1000-4-2	>1.5	kV
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{DD} pins to induce a functional disturbance	V_{DD}=5V, T_A=+25°C, f_{OSC}=8MHz conforms to IEC 1000-4-4	>1.5	kV

Electro Magnetic Interference (EMI)

Based on a simple application running on the product, the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 115. Emission test

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{OSC}/f_{CPU}]	Unit
				4/10MHz	
S_{EMI}	Peak level	V_{DD}=5V, T_A=+25°C, PQFP100 14x20 package conforming to SAE J 1752/3	0.1MHz to 30MHz	13	dBµV
			30MHz to 130MHz	25	
			130MHz to 1GHz	24	
			SAE EMI Level	3.5	-

Note: Data based on characterization results, not tested in production.

Absolute Maximum Ratings (Electrical Sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electro-Static Discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard.

17.8.9 SCI-A wrong break duration

Description

A single break character is sent by setting and resetting the SBK bit in the SCICR2 register. In some cases, the break character may have a longer duration than expected:

- 20 bits instead of 10 bits if M=0

- 22 bits instead of 11 bits if M=1.

In the same way, as long as the SBK bit is set, break characters are sent to the TDO pin. This may lead to generate one break more than expected.

Occurrence

The occurrence of the problem is random and proportional to the baudrate. With a transmit frequency of 19200 baud (f_{CPU}=8MHz and SCIBRR=0xC9), the wrong break duration occurrence is around 1%.

Workaround

If this wrong duration is not compliant with the communication protocol in the application, software can request that an Idle line be generated before the break character. In this case, the break duration is always correct assuming the application is not doing anything between the idle and the break. This can be ensured by temporarily disabling interrupts.

The exact sequence is:

- Disable interrupts

- Reset and Set TE (IDLE request)

- Set and Reset SBK (Break Request)

- Re-enable interrupts

LIN mode (if available)

If the LINE bit in the SCICR3 is set and the M bit in the SCICR1 register is reset, the SCI-A is in LIN master mode. A single break character is sent by setting and resetting the SBK bit in the SCICR2 register. In some cases, the break character may have a longer duration than expected:

- 24 bits instead of 13 bits

Occurrence

The occurrence of the problem is random and proportional to the baudrate. With a transmit frequency of 19200 baud (fCPU=8MHz and SCIBRR=0xC9), the wrong break duration occurrence is around 1%.

Analysis

The LIN protocol specifies a minimum of 13 bits for the break duration, but there is no maximum value. Nevertheless, the maximum length of the header is specified as (14+10+10+1)x1.4=49 bits. This is composed of:

- the synch break field (14 bits),

- the synch field (10 bits),

18 Revision history

Table 146. Document revision history

Date	Revision	Changes
28-Oct-2004	3	Revision number incremented from 1.5 to 3.0 due to Internal Document Management System change Changed document status: Datasheet instead of Preliminary Data Added 2EFT for TQFP64 devices Changed description in *Section 2.2 on page 28* Replaced 1 by DPR1 in Page 21 column (*Figure 26 on page 66*) Removed references to sector 2 (mirrored) in *Figure 30 on page 75*, *Table 9 on page 77* and *Figure 41 on page 98* Removed formula in the description of I2CCCR on *page 350* and added *Table 133 on page 493* Removed “mask option” in the description of ETO bit on *page 191* Changed “INTCLK range” table (FREQ[2:0] bits) on *page 351* Replaced RX by REC and TX by TRAN in CMSR register on *page 428* Changed *Section 14.11 on page 451* (added divider/2) and *Table 107 on page 468* Changed *Flash / E3 TM specifications on page 476* Changed I_{IO} values in *DC electrical characteristics on page 472* Added *Table 122: BOOTROM timing on page 481* Changed ACD Accuracy table on *page 495* Changed *Table 139 on page 501* Added *Section 17 on page 502*
19-Nov-2004	4	Changed *Table 107 on page 468*
16-Nov-2006	5	Replaced TQFP by LQFP Modified reset state and WPU columns for Port 1[7:3] in *Table on page 41* Modified silicon revision list in *Section 17 on page 502* Added *Table 140 on page 502* Added *Section 17.7 on page 513* Removed P1 I/O port characteristics section in *Emulation chip limitations on page 516*: limitation now described in *Section 17.8.1 on page 516* and changed according to modifications made to *Table on page 41* Added two part numbers: ST92F124R1C6 (128K/LQFP64) and ST92F124V1Q6 (128K/LQFP100)
01-Dec-2008	6	Added *Soldering and glueability information on page 500*
12-Jul-2012	7	Added footnote (2) to *Table 138: STMicroelectronics development tools*.