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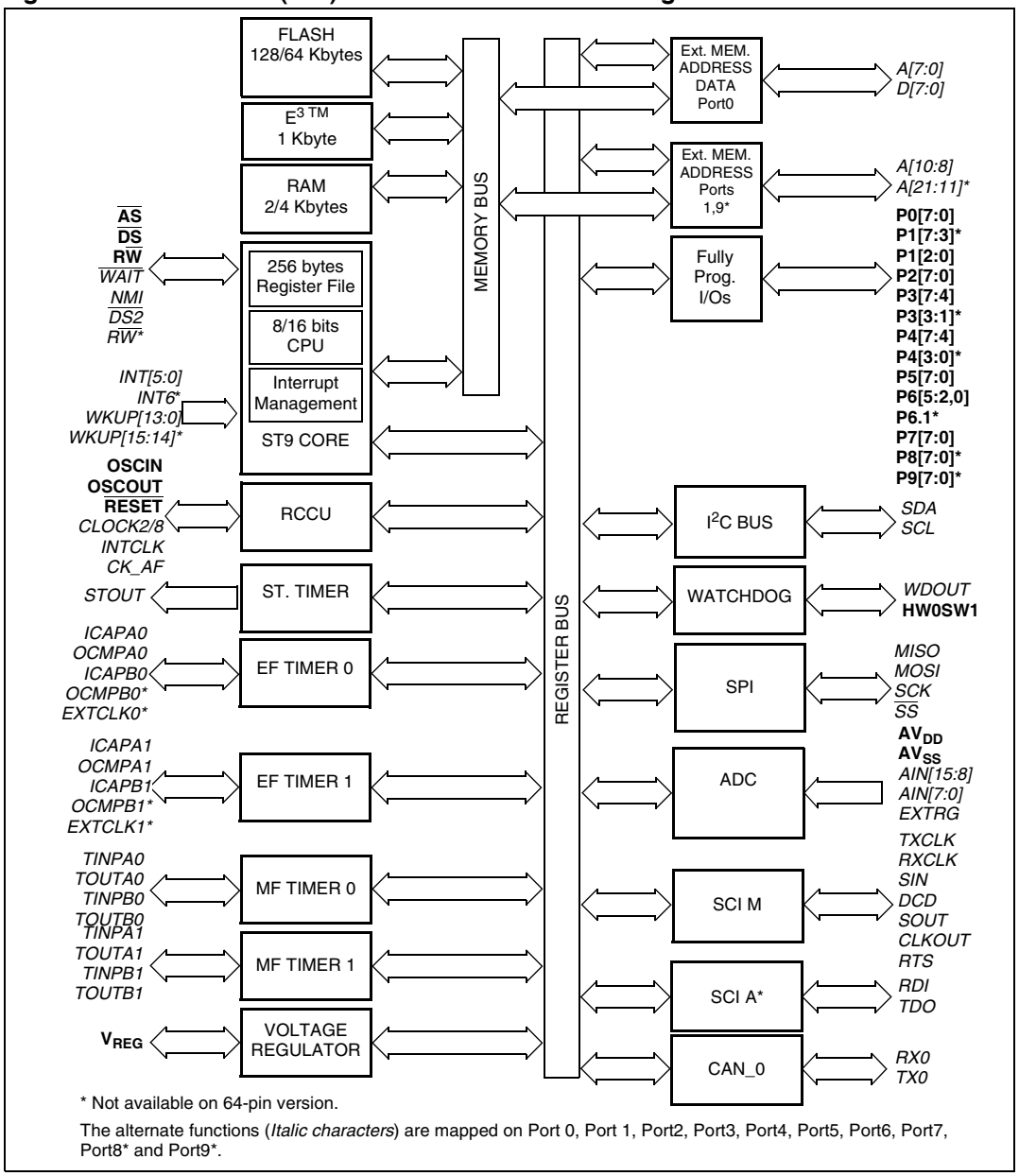
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST9
Core Size	8/16-Bit
Speed	24MHz
Connectivity	EBI/EMI, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	77
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st92f124v1tb

Figure 3. ST92F150C(R/V)1/9: Architectural block diagram



* Not available on 64-pin version.

The alternate functions (*Italic characters*) are mapped on Port 0, Port 1, Port2, Port3, Port4, Port5, Port6, Port7, Port8* and Port9*.

2 Pinout and pin description

$\overline{AS}$. Address Strobe (output, active low, 3-state). Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write ($R\overline{W}$), and Data signals are valid for memory transfers.

$\overline{DS}$. Data Strobe (output, active low, 3-state). Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST9 accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle.

$\overline{RESET}$. Reset (input, active low). The ST9 is initialized by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

R$\overline{W}$. Read/Write (output, 3-state). Read/Write determines the direction of data transfer for external memory transactions. $R\overline{W}$ is low when writing to external memory, and high for all other transactions.

OSCIN, OSCOUT. Oscillator (input and output). These pins connect a parallel-resonant crystal, or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter; OSCOUT is the output of the oscillator inverter.

HW0SW1. When connected to V_{DD} through a 1K pull-up resistor, the software watchdog option is selected. When connected to V_{SS} through a 1K pull-down resistor, the hardware watchdog option is selected.

VPWO. This pin is the output line of the J1850 peripheral (JBLPD). It is available only on some devices.

RX1/WKUP6. Receive Data input of CAN1 and Wake-up line 6. Available only on some devices. When the CAN1 peripheral is disabled, a pull-up resistor is connected internally to this pin.

TX1. Transmit Data output of CAN1. Available on some devices.

P0[7:0], P1[7:0] or P9[7:2] *(Input/Output, TTL or CMOS compatible)*. 11 lines (64-pin devices) or 22 lines (100-pin devices) providing the external memory interface for addressing 2K or 4M bytes of external memory.

P0[7:0], P1[2:0], P2[7:0], P3[7:4], P4.[7:4], P5[7:0], P6[5:2,0], P7[7:0] *I/O Port Lines (Input/Output, TTL or CMOS compatible)*. I/O lines grouped into I/O ports of 8 bits, bit programmable under software control as general purpose I/O or as alternate functions.

P1[7:3], P3[3:1], P4[3:0], P6.1, P8[7:0], P9[7:0] *Additional I/O Port Lines available on 100-pin versions only.*

P3.0, P6[7:6] *Additional I/O Port Lines available on ST92F250 version only.*

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter (common for ADC 0 and ADC 1). AVDD can be switched off when the ADC is not in use.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter (common for ADC 0 and ADC 1).

V_{DD}. Main Power Supply Voltage. Four pins are available on 100-pin versions, two on 64-pin versions. The pins are internally connected.

Table 20. Detailed register map

Page (Dec)	Block	Reg. no.	Register name	Description	Reset value Hex.	Doc. page
N/A	Core	R230	CICR	Central Interrupt Control Register	87	*54*
		R231	FLAGR	Flag Register	00	*55*
		R232	RP0	Pointer 0 Register	xx	*57*
		R233	RP1	Pointer 1 Register	xx	*58*
		R234	PPR	Page Pointer Register	xx	*61*
		R235	MODER	Mode Register	E0	*61*
		R236	USPHR	User Stack Pointer High Register	xx	*64*
		R237	USPLR	User Stack Pointer Low Register	xx	*64*
		R238	SSPHR	System Stack Pointer High Reg.	xx	*64*
		R239	SSPLR	System Stack Pointer Low Reg.	xx	*64*
	I/O Port 0:5	R224	P0DR	Port 0 Data Register	FF	*195*
		R225	P1DR	Port 1 Data Register	FF	
		R226	P2DR	Port 2 Data Register	FF	
		R227	P3DR	Port 3 Data Register	1111 111x	
		R228	P4DR	Port 4 Data Register	FF	
		R229	P5DR	Port 5 Data Register	FF	
0	INT	R242	EITR	External Interrupt Trigger Register	00	*140*
		R243	EIPR	External Interrupt Pending Reg.	00	*140*
		R244	EIMR	External Interrupt Mask-bit Reg.	00	*141*
		R245	EIPLR	External Interrupt Priority Level Reg.	FF	*141*
		R246	EIVR	External Interrupt Vector Register	x6	*212*
		R247	NICR	Nested Interrupt Control	00	*143*
	WDT	R248	WDTHR	Watchdog Timer High Register	FF	*210*
		R249	WDTLR	Watchdog Timer Low Register	FF	*210*
		R250	WDTPR	Watchdog Timer Prescaler Reg.	FF	*210*
		R251	WDTCR	Watchdog Timer Control Register	12	*211*
		R252	WCR	Wait Control Register	7F	*212*

Table 20. Detailed register map (continued)

Page (Dec)	Block	Reg. no.	Register name	Description	Reset value Hex.	Doc. page
37	CAN1* Receive FIFO 0	R240	MFMI	Mailbox Filter Match Index	00	439
		R241	MDLC	Mailbox Data Length Control Register	xx	440
		R242	MIDR0	Mailbox Identifier Register 0	xx	439
		R243	MIDR1	Mailbox Identifier Register 1	xx	439
		R244	MIDR2	Mailbox Identifier Register 2	xx	439
		R245	MIDR3	Mailbox Identifier Register 3	xx	439
		R246	MDAR0	Mailbox Data Register 0	xx	440
		R247	MDAR1	Mailbox Data Register 1	xx	440
		R248	MDAR2	Mailbox Data Register 2	xx	440
		R249	MDAR3	Mailbox Data Register 3	xx	440
		R250	MDAR4	Mailbox Data Register 4	xx	440
		R251	MDAR5	Mailbox Data Register 5	xx	440
		R252	MDAR6	Mailbox Data Register 6	xx	440
		R253	MDAR7	Mailbox Data Register 7	xx	440
		R254	MTSLR	Mailbox Time Stamp Low Register	xx	441
		R255	MTSHR	Mailbox Time Stamp High Register	xx	441
38	CAN1* Receive FIFO 1	R240	MFMI	Mailbox Filter Match Index	00	439
		R241	MDLC	Mailbox Data Length Control Register	xx	440
		R242	MIDR0	Mailbox Identifier Register 0	xx	439
		R243	MIDR1	Mailbox Identifier Register 1	xx	439
		R244	MIDR2	Mailbox Identifier Register 2	xx	439
		R245	MIDR3	Mailbox Identifier Register 3	xx	439
		R246	MDAR0	Mailbox Data Register 0	xx	440
		R247	MDAR1	Mailbox Data Register 1	xx	440
		R248	MDAR2	Mailbox Data Register 2	xx	440
		R249	MDAR3	Mailbox Data Register 3	xx	440
		R250	MDAR4	Mailbox Data Register 4	xx	440
		R251	MDAR5	Mailbox Data Register 5	xx	440
		R252	MDAR6	Mailbox Data Register 6	xx	440
		R253	MDAR7	Mailbox Data Register 7	xx	440
		R254	MTSLR	Mailbox Time Stamp Low Register	xx	441
		R255	MTSHR	Mailbox Time Stamp High Register	xx	441

Table 20. Detailed register map (continued)

Page (Dec)	Block	Reg. no.	Register name	Description	Reset value Hex.	Doc. page
41	CAN1 * Tx Mailbox 2	R240	MCSR	Mailbox Control Status Register	00	*437*
		R241	MDLC	Mailbox Data Length Control Register	x0	*440*
		R242	MIDR0	Mailbox Identifier Register 0	xx	*439*
		R243	MIDR1	Mailbox Identifier Register 1	xx	*439*
		R244	MIDR2	Mailbox Identifier Register 2	xx	*439*
		R245	MIDR3	Mailbox Identifier Register 3	xx	*439*
		R246	MDAR0	Mailbox Data Register 0	xx	*440*
		R247	MDAR1	Mailbox Data Register 1	xx	*440*
		R248	MDAR2	Mailbox Data Register 2	xx	*440*
		R249	MDAR3	Mailbox Data Register 3	xx	*440*
		R250	MDAR4	Mailbox Data Register 4	xx	*440*
		R251	MDAR5	Mailbox Data Register 5	xx	*440*
		R252	MDAR6	Mailbox Data Register 6	xx	*440*
		R253	MDAR7	Mailbox Data Register 7	xx	*440*
		R254	MTSLR	Mailbox Time Stamp Low Register	xx	*441*
		R255	MTSHR	Mailbox Time Stamp High Register	xx	*441*
42	CAN1 * Filters	See *Page mapping for CAN 0 / CAN 1 on page 448*		Filter Configuration Acceptance Filters 7:0 (5 register pages)		
43	I/O Port 8 *	R248	P8C0	Port 8 Configuration Register 0	03	*195*
		R249	P8C1	Port 8 Configuration Register 1	00	
		R250	P8C2	Port 8 Configuration Register 2	00	
		R251	P8DR	Port 8 Data Register	FF	
	I/O Port 9 *	R252	P9C0	Port 9 Configuration Register 0	00	
		R253	P9C1	Port 9 Configuration Register 1	00	
		R254	P9C2	Port 9 Configuration Register 2	00	
		R255	P9DR	Port 9 Data Register	FF	

Table 20. Detailed register map (continued)

Page (Dec)	Block	Reg. no.	Register name	Description	Reset value Hex.	Doc. page
50	CAN0* Receive FIFO 1	R240	MFMI	Mailbox Filter Match Index	00	439
		R241	MDLC	Mailbox Data Length Control Register	xx	440
		R242	MIDR0	Mailbox Identifier Register 0	xx	439
		R243	MIDR1	Mailbox Identifier Register 1	xx	439
		R244	MIDR2	Mailbox Identifier Register 2	xx	439
		R245	MIDR3	Mailbox Identifier Register 3	xx	439
		R246	MDAR0	Mailbox Data Register 0	xx	440
		R247	MDAR1	Mailbox Data Register 1	xx	440
		R248	MDAR2	Mailbox Data Register 2	xx	440
		R249	MDAR3	Mailbox Data Register 3	xx	440
		R250	MDAR4	Mailbox Data Register 4	xx	440
		R251	MDAR5	Mailbox Data Register 5	xx	440
		R252	MDAR6	Mailbox Data Register 6	xx	440
		R253	MDAR7	Mailbox Data Register 7	xx	440
		R254	MTSLR	Mailbox Time Stamp Low Register	xx	441
		R255	MTSHR	Mailbox Time Stamp High Register	xx	441
51	CAN0* Tx Mailbox 0	R240	MCSR	Mailbox Control Status Register	00	437
		R241	MDLC	Mailbox Data Length Control Register	xx	440
		R242	MIDR0	Mailbox Identifier Register 0	xx	439
		R243	MIDR1	Mailbox Identifier Register 1	xx	439
		R244	MIDR2	Mailbox Identifier Register 2	xx	439
		R245	MIDR3	Mailbox Identifier Register 3	xx	439
		R246	MDAR0	Mailbox Data Register 0	xx	440
		R247	MDAR1	Mailbox Data Register 1	xx	440
		R248	MDAR2	Mailbox Data Register 2	xx	440
		R249	MDAR3	Mailbox Data Register 3	xx	440
		R250	MDAR4	Mailbox Data Register 4	xx	440
		R251	MDAR5	Mailbox Data Register 5	xx	440
		R252	MDAR6	Mailbox Data Register 6	xx	440
		R253	MDAR7	Mailbox Data Register 7	xx	440
		R254	MTSLR	Mailbox Time Stamp Low Register	xx	441
		R255	MTSHR	Mailbox Time Stamp High Register	xx	441

10.6 DMA registers

As each peripheral DMA channel has its own specific control registers, the following register list should be considered as a general example. The names and register bit allocations shown here may be different from those found in the peripheral chapters.

DMA COUNTER POINTER REGISTER (DCPR)
Read/Write
Address set by Peripheral
Reset value: undefined

7							0
C7	C6	C5	C4	C3	C2	C1	RM

Bit 7:1 = **C[7:1]**: *DMA Transaction Counter Pointer.*

Software should write the pointer to the DMA Transaction Counter in these bits.

Bit 0 = **RM**: *Register File/Memory Selector.*
This bit is set and cleared by software.

0: DMA transactions are with memory (see also DAPR.DP)

1: DMA transactions are with the Register File

GENERIC EXTERNAL PERIPHERAL INTERRUPT AND DMA CONTROL (IDCR)
Read/Write
Address set by Peripheral
Reset value: undefined

7							0
		IP	DM	IM	PRL2	PRL1	PRL0

Bit 5 = **IP**: *Interrupt Pending*.

This bit is set by hardware when the Trigger Event occurs. It is cleared by hardware when the request is acknowledged. It can be set/cleared by software in order to generate/cancel a pending request.

0: No interrupt pending

1: Interrupt pending

Bit 4 = **DM**: *DMA Request Mask*.

This bit is set and cleared by software. It is also cleared when the transaction counter reaches zero (unless SWAP mode is active).

0: No DMA request is generated when IP is set.

1: DMA request is generated when IP is set

Bit 3 = **IM**: *End of block Interrupt Mask*.
This bit is set and cleared by software.

$\overline{DS2}$ is released in high-impedance during bus acknowledge cycle or under processor control by setting the HIMP bit (MODER.0, r235).

The behavior of this signal is also affected by the DS2EN bit in the EMR1 register. Refer to the Register description.

12.2.5 PORT 0

If Port 0 is used as a bit programmable parallel I/O port, it has the same features as a regular port. When set as an Alternate Function, it is used as the External Memory interface: it outputs the multiplexed Address (8 LSB: A[7:0]) / Data bus D[7:0].

12.2.6 PORT 1

If Port 1 is used as a bit programmable parallel I/O port, it has the same features as a regular port. When set as an Alternate Function, it is used as the external memory interface to provide the address bits A[15:8].

12.2.7 PORT 9 [7:2]

If Port 9 is available and used as a bit programmable I/O port, it has the same features as a regular port. If the MMU is available on the device and Port 9 is set as an Alternate Function, Port 9[7:2] is used as the external memory interface to provide the 6 MSB of the address (A[21:16]).

Note: For the ST92F250 device, since A[18:17] share the same pins as SDA1 and SCL1 of I²C_1, these address bits are not available when the I²C_1 is in use (when I2CCR.PE bit is set).

Figure 74. Application example (MC=0)

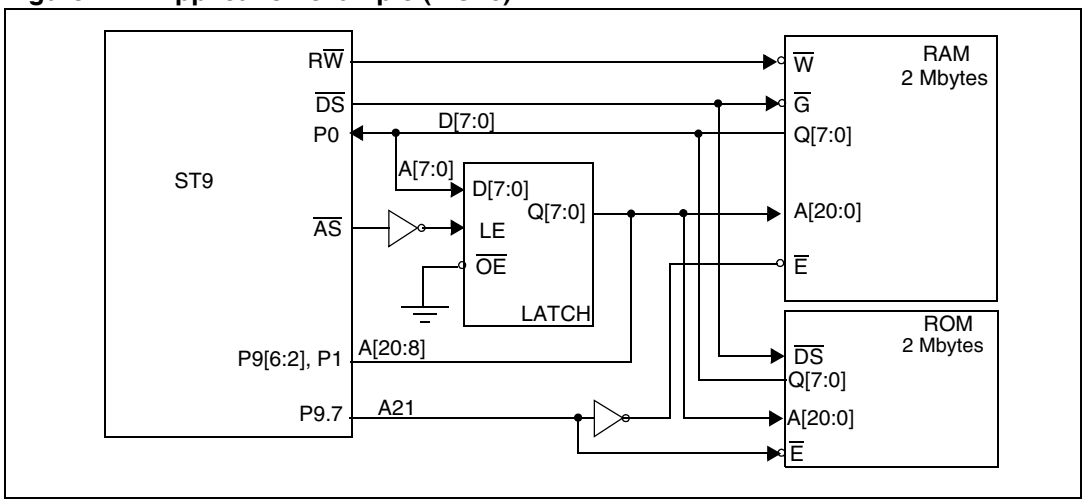


Figure 87. Interrupt sources

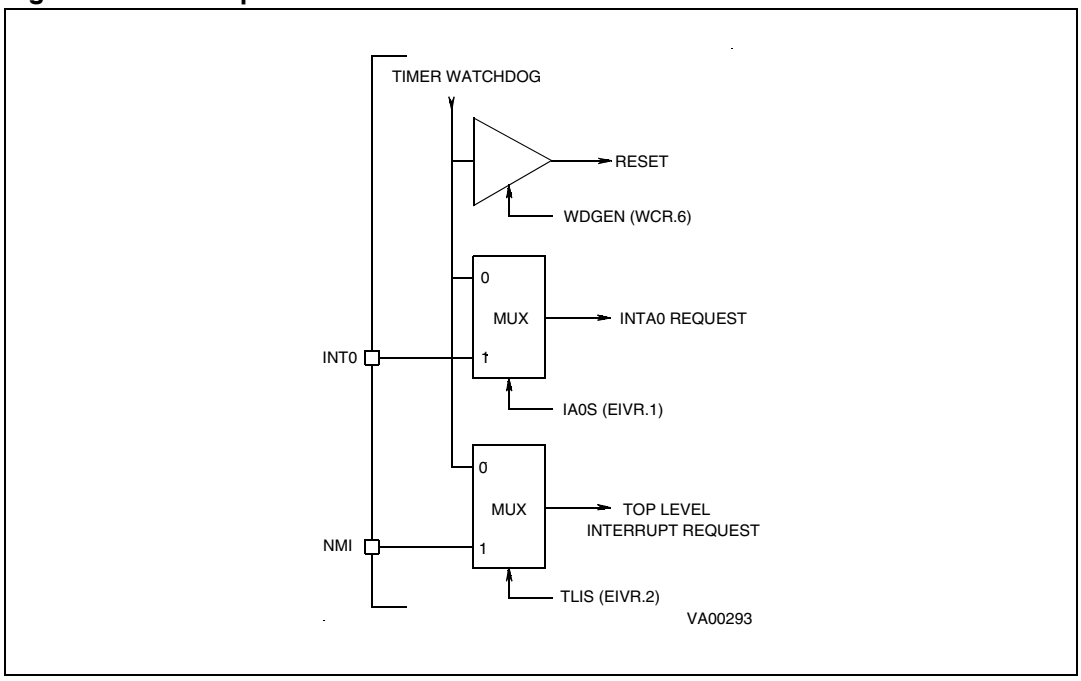


Table 45. Interrupt configuration

Control bits			Enabled sources			Operating mode
WDGEN	IA0S	TLIS	Reset	INTA0	Top level	
0	0	0	WDG/Ext Reset	SW TRAP	SW TRAP	Watchdog
0	0	1	WDG/Ext Reset	SW TRAP	Ext Pin	Watchdog
0	1	0	WDG/Ext Reset	Ext Pin	SW TRAP	Watchdog
0	1	1	WDG/Ext Reset	Ext Pin	Ext Pin	Watchdog
1	0	0	Ext Reset	Timer	Timer	Timer
1	0	1	Ext Reset	Timer	Ext Pin	Timer
1	1	0	Ext Reset	Ext Pin	Timer	Timer
1	1	1	Ext Reset	Ext Pin	Ext Pin	Timer

Legend:
WDG = Watchdog function
SW TRAP = Software Trap

Note: If IA0S and TLIS = 0 (enabling the Watchdog EOC as interrupt source for both Top Level and INTA0 interrupts), only the INTA0 interrupt is taken into account.

14.1.5 Register description

The Timer/Watchdog is associated with 4 registers mapped into Group F, Page 0 of the Register File.

WDTHR: Timer/Watchdog High Register

WDTLR: Timer/Watchdog Low Register

WDTPR: Timer/Watchdog Prescaler Register

When a match is found:

- The OCF*i* bit is set.
- The OCMP*i* pin takes the OLVL*i* bit value (the OCMP*i* pin latch is forced low during reset and stays low until a valid compare changes it to the OLVL*i* level).
- A timer interrupt is generated under the following two conditions:

1. If the OCIE bit (for both OCMP1 & OCMP2) and the EFTIS bit are set.

Note: If the OCIE bit is set, the status of the OC1IE/OC2IE bits in the CR3 register is not significant.

2. If the OCIE bit is reset and the OC1IE and /or OC2IE bits are set and the EFTIS bit is set. Otherwise, the interrupt remains pending until the related enable bits are set.

Clearing the output compare interrupt request is done by:

- An access (read or write) to the SR register while the OCF*i* bit is set.
- An access (read or write) to the OC*i*LR register.

Note: After a write access to the OCiHR register, the output compare function is inhibited until the OCiLR register is also written.

If the OC*i*E bit is not set, the OCMP*i* pin is a general I/O port and the OLVL*i* bit will not appear when match is found but an interrupt could be generated if the OCIE bit is set.

The value in the 16-bit OC*i*R register and the OLVL*i* bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed timeout.

The OC*i*R register value required for a specific timing application can be calculated using the following formula:

$$\Delta \text{OC}i\text{R} = \frac{\Delta t * \text{INTCLK}}{(\text{CC1.CC0})}$$

Where:

Δt = Desired output compare period (in seconds)

INTCLK = Internal clock frequency

CC[1:0] = Timer clock prescaler

The following procedure is recommended to prevent the OCF*i* bit from being set between the time it is read and the write to the OC*i*R register:

- Write to the OC*i*HR register (further compares are inhibited).
- Read the SR register (first step of the clearance of the OCF*i* bit, which may be already set).
- Write to the OC*i*LR register (enables the output compare function and clears the OCF*i* bit).

Bits 3:2 = **CC[1:0]** *Clock Control.*

The value of the timer clock depends on these bits:

Table 50. Clock control bits

CC1	CC0	Timer clock
0	0	INTCLK / 4
0	1	INTCLK / 2
1	0	INTCLK / 8
1	1	External Clock

Bit 1 = **IEDG2** *Input Edge 2.*
This bit determines which type of level transition on the ICAP2 pin will trigger the capture.

0: A falling edge triggers the capture.

1: A rising edge triggers the capture.

Bit 0 = **EXEDG** *External Clock Edge.*
This bit determines which type of level transition on the external clock pin EXTCLK will trigger the free running counter.

0: A falling edge triggers the free running counter.

1: A rising edge triggers the free running counter.

STATUS REGISTER (SR)

R254 - Read Only
Register Page: 28
Reset Value: 0000 0000 (00h)

The three least significant bits are not used.

7							0
ICF1	OCF1	TOF	ICF2	OCF2	0	0	0

Bit 7 = **ICF1** *Input Capture Flag 1.*

0: No input capture (reset value).

1: An input capture has occurred. To clear this bit, first read the SR register, then read or write the low byte of the IC1R (IC1LR) register.

Bit 6 = **OCF1** *Output Compare Flag 1.*

0: No match (reset value).

1: The content of the free running counter has matched the content of the OC1R register. To clear this bit, first read the SR register, then read or write the low byte of the OC1R (OC1LR) register.

Note: For proper operation of the External Input pins, the following must be observed:

- the minimum external clock/trigger pulse width must not be less than the system clock (INTCLK) period if the input pin is programmed as rising or falling edge sensitive.
- the minimum external clock/trigger pulse width must not be less than the prescaler clock period (INTCLK/3) if the input pin is programmed as rising and falling edge sensitive (valid also in Auto discrimination mode).
- the minimum delay between two clock/trigger pulse active edges must be greater than the prescaler clock period (INTCLK/3), while the minimum delay between two consecutive clock/trigger pulses must be greater than the system clock (INTCLK) period.
- the minimum gate pulse width must be at least twice the prescaler clock period (INTCLK/3).
- in Autodiscrimination mode, the minimum delay between the input pin A pulse edge and the edge of the input pin B pulse, must be at least equal to the system clock (INTCLK) period.
- if a number, N, of external pulses must be counted using a Compare Register in External Clock mode, then the Compare Register must be loaded with the value [X +/- (N-1)], where X is the starting counter value and the sign is chosen depending on whether Up or Down count mode is selected.

TxINA = I/O - TxINB = I/O

Input pins A and B are not used by the Timer. The counter clock is internally generated and the up/down selection may be made only by software via the UDC (Software Up/Down) bit in the TCR register.

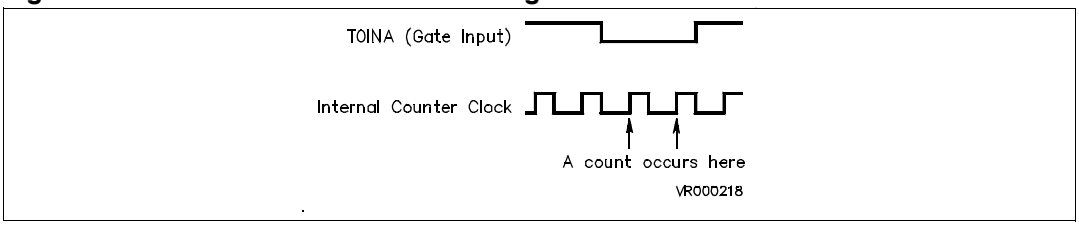
TxINA = I/O - TxINB = Trigger

The signal applied to input pin B acts as a trigger signal on REG1R register. The prescaler clock is internally generated and the up/down selection may be made only by software via the UDC (Software Up/Down) bit in the TCR register.

TxINA = Gate - TxINB = I/O

The signal applied to input pin A acts as a gate signal for the internal clock (i.e. the counter runs only when the gate signal is at a low level). The counter clock is internally generated and the up/down control may be made only by software via the UDC (Software Up/Down) bit in the TCR register.

Figure 105. TxINA = Gate - TxINB = I/O signal

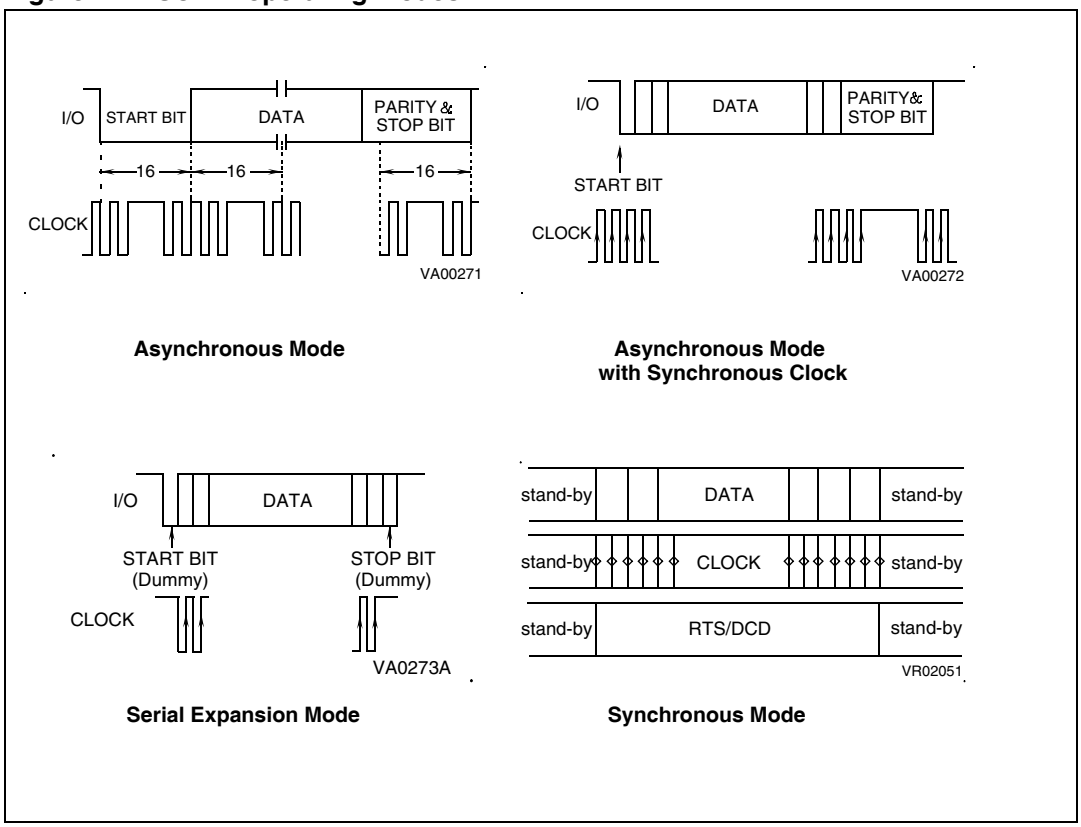


TxINA = Gate - TxINB = Trigger

Both input pins A and B are connected to the timer, with the resulting effect of combining the actions relating to the previously described configurations.

The data word is programmable from 5 to 8 bits, as for the other modes; parity, address/9th, stop bits and break cannot be inserted into the transmitted frame. Programming of the related bits of the SCI control registers is irrelevant in Synchronous Mode: all the corresponding interrupt requests must, in any case, be masked in order to avoid incorrect operation during data reception.

Figure 124. SCI -M operating modes



Note: In all operating modes, the Least Significant Bit is transmitted/received first.

14.5.5 Serial frame format

Characters sent or received by the SCI can have some or all of the features in the following format, depending on the operating mode:

START: the START bit indicates the beginning of a data frame in Asynchronous modes. The START condition is detected as a high to low transition.
A dummy START bit is generated in Serial Expansion mode. The START bit is not generated in Synchronous mode.

DATA: the DATA word length is programmable from 5 to 8 bits, for both Synchronous and Asynchronous modes. LSB are transmitted first.

PARITY: The Parity Bit (not available in Serial Expansion mode and Synchronous mode) is optional, and can be used with any word length. It is used for error checking and is set so as to make the total number of high bits in DATA plus PARITY odd or even, depending on the number of “1”s in the DATA field.

Transmitter

The transmitter can send data words of either 8 or 9 bits depending on the M bit status. When the M bit is set, word length is 9 bits and the 9th bit (the MSB) has to be stored in the T8 bit in the SCICR1 register.

Character transmission
During an SCI transmission, data shifts out least significant bit first on the TDO pin. In this mode, the SCIDR register consists of a buffer (TDR) between the internal bus and the transmit shift register (see *Figure 131*).

Procedure

- Select the M bit to define the word length.
- Select the desired baud rate using the SCIBRR and the SCIETPR registers.
- Set the TE bit to send an idle frame as first transmission.
- Access the SCISR register and write the data to send in the SCIDR register (this sequence clears the TDRE bit). Repeat this sequence for each data to be transmitted.

Clearing the TDRE bit is always performed by the following software sequence:

1. An access to the SCISR register
2. A write to the SCIDR register

The TDRE bit is set by hardware and it indicates:

- The TDR register is empty.
- The data transfer is beginning.
- The next data can be written in the SCIDR register without overwriting the previous data.

This flag generates an interrupt if the TIE bit is set in the SCICR2 register and the IMI0 bit is set in the SIMRH register.

When a transmission is taking place, a write instruction to the SCIDR register stores the data in the TDR register and which is copied in the shift register at the end of the current transmission.

When no transmission is taking place, a write instruction to the SCIDR register places the data directly in the shift register, the data transmission starts, and the TDRE bit is immediately set.

When a frame transmission is complete (after the stop bit or after the break frame) the TC bit is set and an interrupt is generated if the TCIE is set and the IMI0 bit is set in the SIMRH register.

Clearing the TC bit is performed by the following software sequence:

1. An access to the SCISR register
2. A write to the SCIDR register

Note: The TDRE and TC bits are cleared by the same software sequence.

LIN transmission

The same procedure has to be applied with the following differences:

- Clear the M bit to configure 8-bit word length
- Set the LINE bit to enter LIN Master mode. In this case, setting the SBK bit will send 13 low bits.

INTCLK/(n1*n2*n3) where n1= PRS[2:0]+1, n2 is the value defined by the SPR[1:0] bits (refer to *Table 84* and *Table 85*), n3 = 1 if DIV2=1 and n3= 2 if DIV2=0. Refer to *Figure 135*.

These bits have no effect in slave mode.

Table 85. Prescaler baud rate

Prescaler division factor	PRS2	PRS1	PRS0
1 (no division)	0	0	0
2	0	0	1
...			
8	1	1	1

14.8 I^2C bus interface

14.8.1 Introduction

The I^2C bus Interface serves as an interface between the microcontroller and the serial I^2C bus. It provides both multimaster and slave functions with both 7-bit and 10-bit address modes; it controls all I^2C bus-specific sequencing, protocol, arbitration, timing and supports both standard (100KHz) and fast I^2C modes (400KHz).
Using DMA, data can be transferred with minimum use of CPU time.

The peripheral uses two external lines to perform the protocols: SDA, SCL.

14.8.2 Main features

- Parallel-bus/I^2C protocol converter
- Multi-master capability
- 7-bit/10-bit Addressing
- Standard I^2C mode/Fast I^2C mode
- Transmitter/Receiver flag
- End-of-byte transmission flag
- Transfer problem detection
- Interrupt generation on error conditions
- Interrupt generation on transfer request and on data received

I^2C master features:

- Start bit detection flag
- Clock generation
- I^2C bus busy flag
- Arbitration Lost flag
- End of byte transmission flag
- Transmitter/Receiver flag
- Stop/Start generation

Note: This bit has no effect on DMA transfer.

Table 87. I²C bus register map and reset values

Address (Hex.)	Register name	7	6	5	4	3	2	1	0
F0h	I2CCR Reset Value	- 0	- 0	PE 0	ENGC 0	START 0	ACK 0	STOP 0	ITE 0
F1h	I2CSR1 Reset Value	EVF 0	ADD10 0	TRA 0	BUSY 0	BTF 0	ADSL 0	M/SL 0	SB 0
F2h	I2CSR2 Reset Value	- 0	0 0	ADDTX 0	AF 0	STOPF 0	ARLO 0	BERR 0	GCAL 0
F3h	I2CCCR Reset Value	FM/SM 0	CC6 0	CC5 0	CC4 0	CC3 0	CC2 0	CC1 0	CC0 0
F4h	I2COAR1 Reset Value	ADD7 0	ADD6 0	ADD5 0	ADD4 0	ADD3 0	ADD2 0	ADD1 0	ADD0 0
F5h	I2COAR2 Reset Value	FREQ1 0	FREQ0 0	EN10BIT 0	FREQ2 0	0 0	ADD9 0	ADD8 0	0 0
F6h	I2CDR Reset Value	DR7 0	DR6 0	DR5 0	DR4 0	DR3 0	DR2 0	DR1 0	DR0 0
F7h	I2CADR Reset Value	ADR7 1	ADR6 0	ADR5 1	ADR4 0	ADR3 0	ADR2 0	ADR1 0	ADR0 0
F8h	I2CISR Reset Value	DMASTOP 1	PRL2 X	PRL1 X	PRL0 X	X	IERRP X	IRXP X	ITXP X
F9h	I2CIVR Reset Value	V7 X	V6 X	V5 X	V4 X	V3 X	EV2 X	EV1 X	0 0
FAh	I2CRDAP Reset Value	RA7 X	RA6 X	RA5 X	RA4 X	RA3 X	RA2 X	RA1 X	RPS X
FBh	I2CRDC Reset Value	RC7 X	RC6 X	RC5 X	RC4 X	RC3 X	RC2 X	RC1 X	RF/MEM X
FCh	I2CTDAP Reset Value	TA7 X	TA6 X	TA5 X	TA4 X	TA3 X	TA2 X	TA1 X	TPS X

Table 92. JBLPD internal priority levels

Priority Level	Interrupt Source
Higher	ERROR, TLA
	EODM, EOFM
	RDRF, REOB
Lower	TRDY, TEOB

The user can program the most significant bits of the interrupt vectors by writing the V[7:3] bits of the IVR register. Starting from the value stored by the user, the JBLPD sets the three least significant bits of the IVR register to produce four interrupt vectors that are associated with interrupt sources as shown in *Table 93*.

Table 93. JBLPD interrupt vectors

Interrupt Vector	Interrupt Source
V[7:3] 000b	ERROR, TLA
V[7:3] 010b	EODM, EOFM
V[7:3] 100b	RDRF, REOB
V[7:3] 110b	TRDY, TEOB

Each interrupt source has a pending bit in the STATUS register, except the DMA interrupt sources that have the interrupt pending bits located in the PRLR register.
These bits are set by hardware when the corresponding interrupt event occurs. An interrupt request is performed only if the related mask bits are set in the IMR register and the JBLPD has priority.
The pending bits have to be reset by the user software. Note that until the pending bits are set (while the corresponding mask bits are set), the JBLPD processes interrupt requests. So, if at the end of an interrupt routine the related pending bit is not reset, another interrupt request is performed.
To reset the pending bits, different actions have to be done, depending on each bit: see the description of the STATUS and PRLR registers.

14.9.6 DMA features

The JBLPD can use the ST9 on-chip Direct Memory Access (DMA) channels to provide high-speed data transactions between the JBLPD and contiguous locations of Register File and Memory. The transactions can occur from and toward the JBLPD. The maximum number of transactions that each DMA channel can perform is 222 with Register File or 65536 with Memory. Control of the DMA features is performed using registers located in the JBLPD register page (IVR, PRLR, IMR, RDAPR, RDCPR, TDAPR, TDCPR).

The priority level of the DMA features of the JBLPD with respect to the other ST9 peripherals and the CPU is the same as programmed in the PRLR register for the interrupt sources. In the internal priority level order of the JBLPD, depending on the value of the DMASUSP bit in the OPTIONS register, the DMA may or may not have a higher priority than the interrupt sources.
Refer to the Interrupt and DMA chapters of the datasheet for details on priority levels.

Bit 7 = **TTO** *Transmitter Timeout Flag*
The TTO bit is set when the VPWO pin has been in a logic one (or active) state for longer than 1 ms. This flag is the output of a diagnostic circuit based on the prescaled system clock input. If the 4X bit is not set, the TTO will trip if the VPWO is constantly active for 1000 prescaled clock cycles. If the 4X bit is set, then the TTO will timeout at 4000 prescaled clock cycles. When the TTO flag is set then the diagnostic circuit will disable the VPWO signal, and disable the JBLPD peripheral. The user program must then clear the JE bit to remove the TTO error. It can then retry the block by setting the JE bit again.
The TTO bit can be used to determine if the external J1850 bus is shorted low. Since the transmitter looks for proper edges returned at the VPWI pin for its timing, a lack of edges seen at VPWI when trying to transmit (assuming the RBRK does not get set) would indicate a constant low condition. The user program can take appropriate actions to test the J1850 bus circuit when a TTO occurs.

Note: A transmit attempt must occur to detect a bus shorted low condition.
The TTO bit is cleared while the CONTROL.JE bit is reset or while the CONTROL.JDIS bit is set. TTO is cleared on reset.

0: VPWO line at 1 for less than 1 ms

1: VPWO line at 1 for longer than 1 ms

Bit 6 = **TDUF** *Transmitter Data Underflow.*
The TDUF will be set to a logic one if the transmitter expects more information to be transmitted, but a TXOP write has not occurred in time (by the end of transmission of the last bit).
The transmitter knows to expect more information from the user program when transmitting messages or type 3 IFRs only. If an opcode is written to TXOP that does not include appending a CRC byte, then the JBLPD peripheral assumes more data is to be written. When the JBLPD peripheral has shifted out the data byte it must have the next data byte in time to place it directly next to it. If the user program does not place new data in the TXDATA register and write the TXOP register with a proper opcode, then the CRC byte which is being kept tabulated by the transmitter is logically inverted and transmitted out the VPWO pin. This will ensure that listeners will detect this message as an error. In this case the TDUF bit is set to a logic one.
TDUF is cleared by reading the ERROR register with TDUF set. TDUF is also cleared on reset, while the CONTROL.JE bit is reset or while the CONTROL.JDIS bit is set.

0: No transmitter data underflow condition occurred

1: Transmitter data underflow condition occurred

Bit 5 = **RDOF** *Receiver Data Overflow*
The RDOF gets set to a logic one if the data in the RXDATA register has not been read and new data is ready to be transferred to the RXDATA register. The old RXDATA information is lost since it is overwritten with new data.
RDOF is cleared by reading the ERROR register with RDOF set, while the CONTROL.JE bit is reset or while the CONTROL.JDIS bit is set, or on reset.

0: No receiver data overflow condition occurred

1: Receiver data overflow condition occurred

Reception

- Two receive FIFOs with three stages
- Eight scalable filter banks
- Identifier list feature
- Configurable FIFO overrun
- Time Stamp on SOF reception

Time Triggered Communication Option

- Disable automatic retransmission mode
- 16-bit free running timer
- Configurable timer resolution
- Time Stamp sent in last two data bytes

Management

- Maskable interrupts
- Software-efficient mailbox mapping at a unique address space

14.10.3 General description

In today's CAN applications, the number of nodes in a network is increasing and often several networks are linked together via gateways. Typically the number of messages in the system (and thus to be handled by each node) has significantly increased. In addition to the application messages, Network Management and Diagnostic messages have been introduced.

- An enhanced filtering mechanism is required to handle each type of message.

Furthermore, application tasks require more CPU time, therefore real-time constraints caused by message reception have to be reduced.

- A receive FIFO scheme allows the CPU to be dedicated to application tasks for a long time period without losing messages.

The standard HLP (Higher Layer Protocol) based on standard CAN drivers requires an efficient interface to the CAN controller.

- All mailboxes and registers are organized in 16-byte pages mapped at the same address and selected via a page select register.

Figure 155. CAN network topology