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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST9
Core Size	8/16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	77
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st92f150cv9tb

The SPI is a synchronous serial interface for Master and Slave device communication. It supports single master and multimaster systems.

A J1850 Byte Level Protocol Decoder is available (ST92F150JDV1 device only) for communicating with a J1850 network.

The bxCAN (basic extended) interface (two in the ST92F150JDV1 device) supports 2.0B Active protocol. It has 3 transmit mailboxes, 2 independent receive FIFOs and 8 filters.

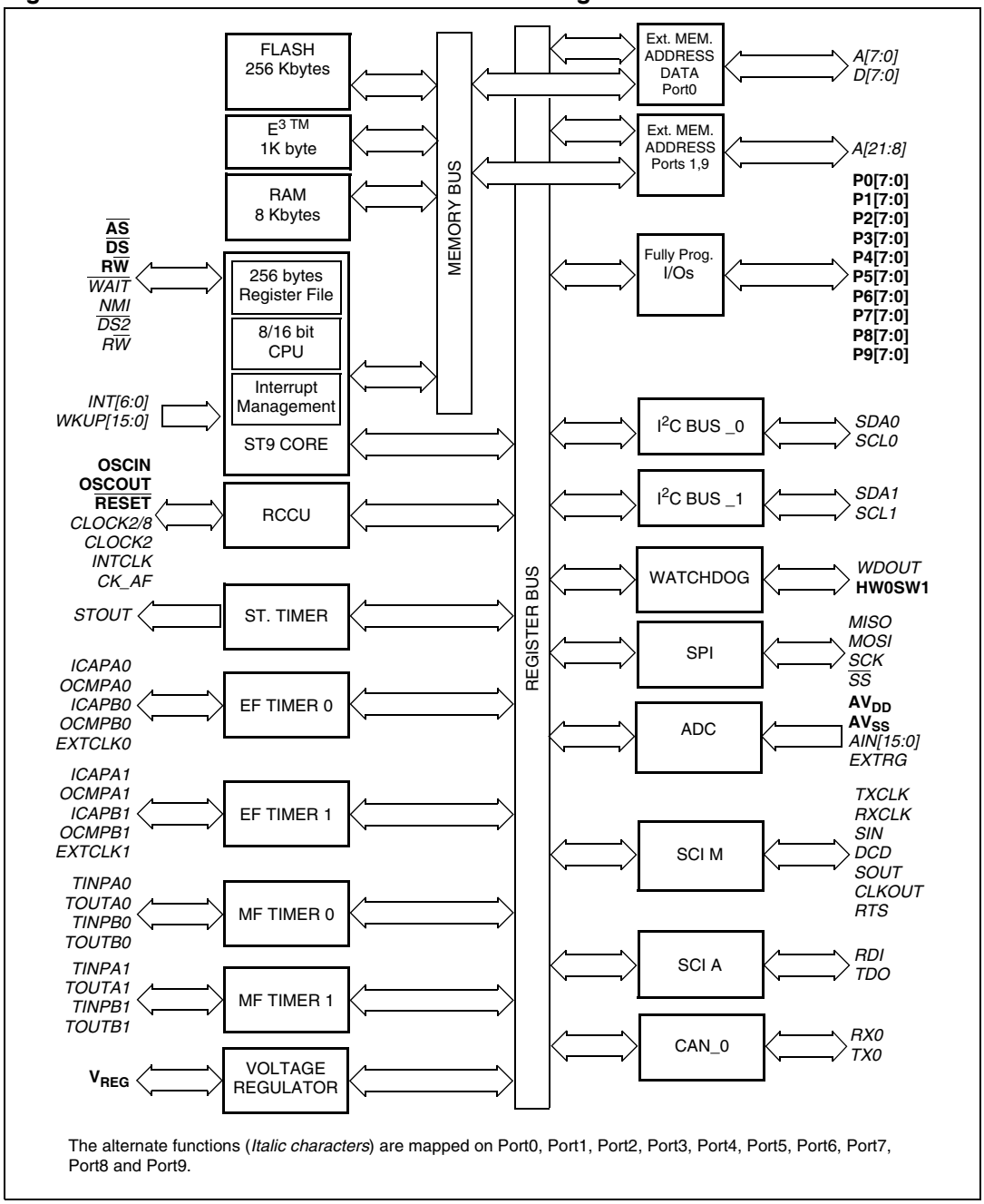
In addition, there is a 16 channel Analog to Digital Converter with integral sample and hold, fast conversion time and 10-bit resolution.

There is one Multiprotocol Serial Communications Interface with an integral generator, asynchronous and synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

On 100-pin devices, there is an additional asynchronous Serial Communications interface with 13-bit LIN Synch Break generation capability.

Finally, a programmable PLL Clock Generator allows the usage of standard 3 to 5 MHz crystals to obtain a large range of internal frequencies up to 24 MHz. Low power Run (SLOW), Wait For Interrupt, low power Wait For Interrupt, STOP and HALT modes are also available.

Figure 5. ST92F250CV2: Architectural block diagram



The alternate functions (*Italic characters*) are mapped on Port0, Port1, Port2, Port3, Port4, Port5, Port6, Port7, Port8 and Port9.

Register Group: E (System)
Reset Value: xxxx xx00 (xxh)

7							0
RG4	RG3	RG2	RG1	RG0	RPS	0	0

Bits 7:3 = **RG[4:0]**: *Register Group number.*
These bits contain the number (in the range 0 to 31) of the register block specified in the `srp0` or `srp` instructions. In single 16-register mode the number indicates the lower of the two 8-register blocks to which the 16 working registers are to be mapped, while in twin 8-register mode it indicates the 8-register block to which `r0` to `r7` are to be mapped.

Bit 2 = **RPS**: *Register Pointer Selector.*
This bit is set by the instructions `srp0` and `srp1` to indicate that the twin register pointing mode is selected. The bit is reset by the `srp` instruction to indicate that the single register pointing mode is selected.

0: Single register pointing mode

1: Twin register pointing mode

Bits 1:0: Reserved. Forced by hardware to zero.

POINTER 1 REGISTER (RP1)
R233 - Read/Write
Register Group: E (System)
Reset Value: xxxx xx00 (xxh)

7							0
RG4	RG3	RG2	RG1	RG0	RPS	0	0

This register is only used in the twin register pointing mode. When using the single register pointing mode, or when using only one of the twin register groups, the RP1 register must be considered as RESERVED and may NOT be used as a general purpose register.

Bits 7:3 = **RG[4:0]:** *Register Group number.* These bits contain the number (in the range 0 to 31) of the 8-register block specified in the `srp1` instruction, to which `r8` to `r15` are to be mapped.

Bit 2 = **RPS**: *Register Pointer Selector.*
This bit is set by the `srp0` and `srp1` instructions to indicate that the twin register pointing mode is selected. The bit is reset by the `srp` instruction to indicate that the single register pointing mode is selected.

0: Single register pointing mode

1: Twin register pointing mode

Bits 1:0: Reserved. Forced by hardware to zero.

Figure 43. ST92F250 internal memory map (256K version)

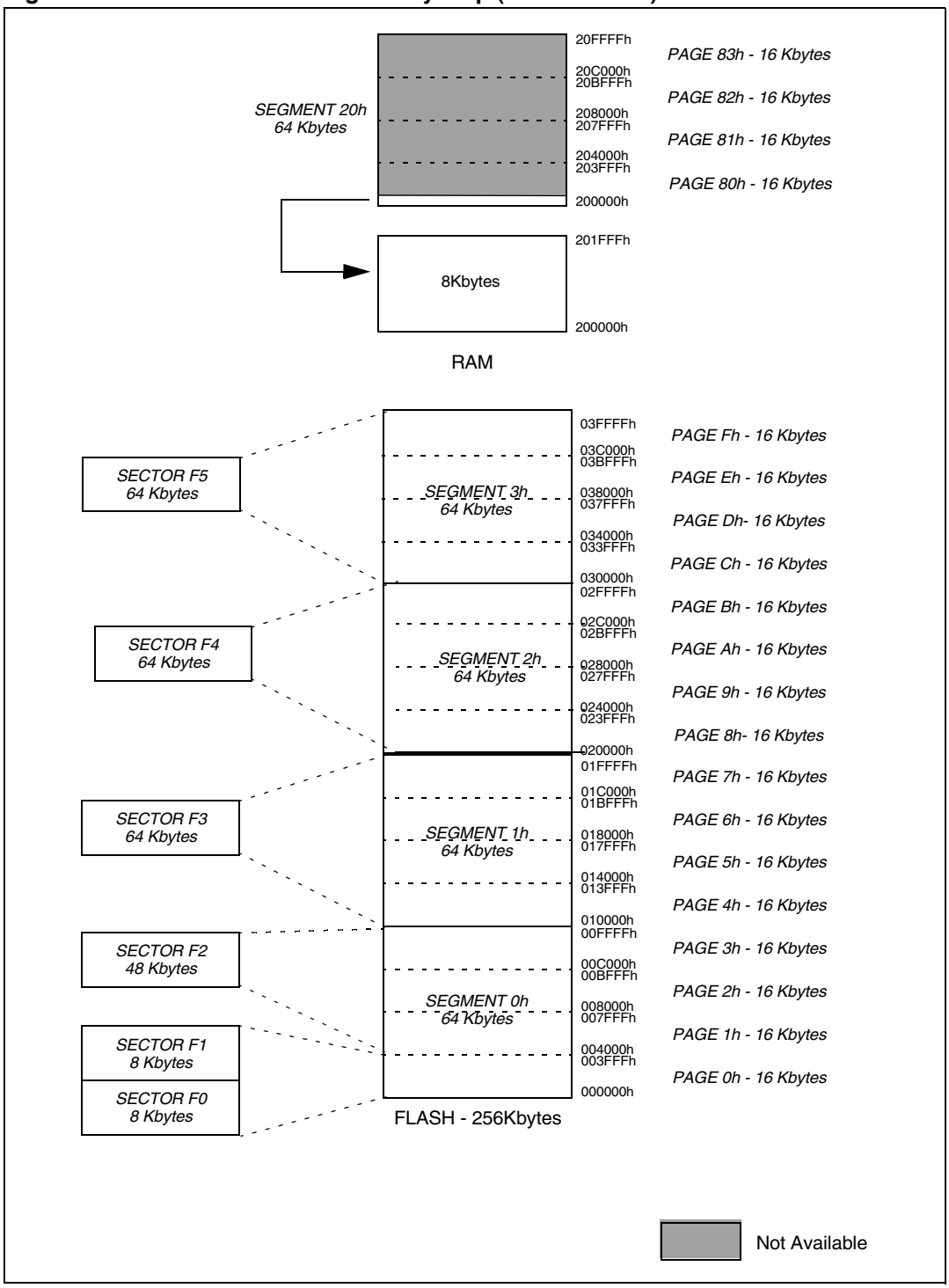


Table 19. Group F pages register map (41 to 63)

Reg.	Page															
	41	42	43	48	49	50	51	52	53	54	55	57	60	61	62	63
R255	CAN_1*	CAN_1*	Port 9*	CAN_0*	CAN_0*	CAN_0*	CAN_0*	CAN_0*	CAN_0*	CAN_0*	Res.	WUIMU	STANDARD INTERRUPT CHANNELS	AD10	AD10 Res	AD10
R254																
R253																
R252																
R251			Port 8*													
R250																
R249																
R248												Res.				
R247			Res.								RCCU		Res			
R246																
R245																
R244																
R243																
R242																
R241																
R240																

* Available on some devices only

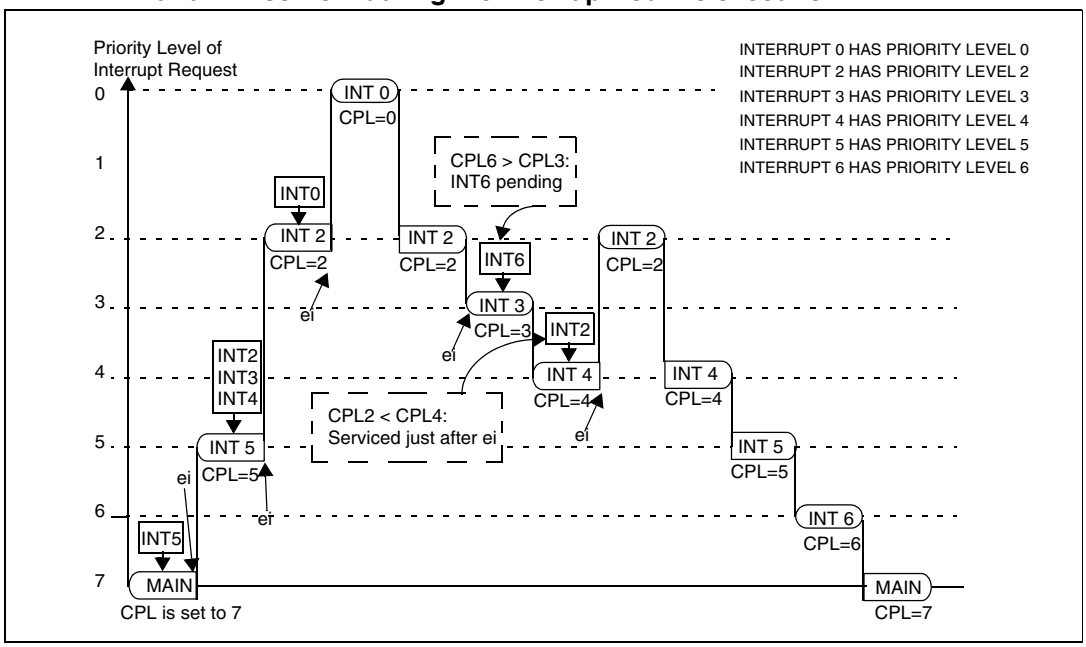
Table 20. Detailed register map (continued)

Page (Dec)	Block	Reg. no.	Register name	Description	Reset value Hex.	Doc. page
48	CAN0* Control/Status	R240	CMCR	CAN Master Control Register	02	426
		R241	CMSR	CAN Master Status Register	02	428
		R242	CTSR	CAN Transmit Control Register	00	429
		R243	CTPR	CAN Transmit Priority Register	00	430
		R244	CRFR0	CAN Receive FIFO Register 0	00	431
		R245	CRFR1	CAN Receive FIFO Register 1	00	431
		R246	CIER	CAN Interrupt Enable Register	00	432
		R247	CESR	CAN Error Status Register	00	433
		R248	CEIER	CAN Error Interrupt Enable Register	00	434
		R249	TECR	Transmit Error Counter Register	00	435
		R250	RECR	Receive Error Counter Register	00	435
		R251	CDGR	CAN Diagnosis Register	00	435
		R252	CBTR0	CAN Bit Timing Register 0	00	436
		R253	CBTR1	CAN Bit Timing Register 1	23	436
		R255	CFPSR	Filter page Select Register	00	437
49	CAN0* Receive FIFO 0	R240	MFMI	Mailbox Filter Match Index	00	439
		R241	MDLC	Mailbox Data Length Control Register	xx	440
		R242	MIDR0	Mailbox Identifier Register 0	xx	439
		R243	MIDR1	Mailbox Identifier Register 1	xx	439
		R244	MIDR2	Mailbox Identifier Register 2	xx	439
		R245	MIDR3	Mailbox Identifier Register 3	xx	439
		R246	MDAR0	Mailbox Data Register 0	xx	440
		R247	MDAR1	Mailbox Data Register 1	xx	440
		R248	MDAR2	Mailbox Data Register 2	xx	440
		R249	MDAR3	Mailbox Data Register 3	xx	440
		R250	MDAR4	Mailbox Data Register 4	xx	440
		R251	MDAR5	Mailbox Data Register 5	xx	440
		R252	MDAR6	Mailbox Data Register 6	xx	440
		R253	MDAR7	Mailbox Data Register 7	xx	440
		R254	MTSLR	Mailbox Time Stamp Low Register	xx	441
		R255	MTSHR	Mailbox Time Stamp High Register	xx	441

Table 20. Detailed register map (continued)

Page (Dec)	Block	Reg. no.	Register name	Description	Reset value Hex.	Doc. page
61	ADC	R240	D0HR	Channel 0 Data High Register	xx	456
		R241	D0LR	Channel 0 Data Low Register	x0	456
		R242	D1HR	Channel 1 Data High Register	xx	457
		R243	D1LR	Channel 1 Data Low Register	x0	457
		R244	D2HR	Channel 2 Data High Register	xx	457
		R245	D2LR	Channel 2 Data Low Register	x0	457
		R246	D3HR	Channel 3 Data High Register	xx	457
		R247	D3LR	Channel 3 Data Low Register	x0	458
		R248	D4HR	Channel 4 Data High Register	xx	458
		R249	D4LR	Channel 4 Data Low Register	x0	458
		R250	D5HR	Channel 5 Data High Register	xx	458
		R251	D5LR	Channel 5 Data Low Register	x0	459
		R252	D6HR	Channel 6 Data High Register	xx	459
		R253	D6LR	Channel 6 Data Low Register	x0	459
		R254	D7HR	Channel 7 Data High Register	xx	459
		R255	D7LR	Channel 7 Data Low Register	x0	459
62		R240	D8HR	Channel 8 Data High Register	xx	460
		R241	D8LR	Channel 8 Data Low Register	x0	460
		R242	D9HR	Channel 9 Data High Register	xx	460
		R243	D9LR	Channel 9 Data Low Register	x0	460
		R244	D10HR	Channel 10 Data High Register	xx	461
		R245	D10LR	Channel 10 Data Low Register	x0	461
		R246	D11HR	Channel 11 Data High Register	xx	461
		R247	D11LR	Channel 11 Data Low Register	x0	461
		R248	D12HR	Channel 12 Data High Register	xx	462
		R249	D12LR	Channel 12 Data Low Register	x0	462
		R250	D13HR	Channel 13 Data High Register	xx	462
		R251	D13LR	Channel 13 Data Low Register	x0	462
		R252	D14HR	Channel 14 Data High Register	xx	463
		R253	D14LR	Channel 14 Data Low Register	x0	463
		R254	D15HR	Channel 15 Data High Register	xx	463
		R255	D15LR	Channel 15 Data Low Register	x0	463

Figure 49. Complex example of a sequence of interrupt requests with Nested mode and IEN set to 1 during the interrupt routine execution



9.6 External interrupts

The ST9 core contains 8 external interrupt sources grouped into four pairs.

Table 23. External interrupt channel grouping

External interrupt	Channel	I/O port pin
WKUP[0:15]	INTD1	P8[1:0] P7[7:5] P6[7,5] P5[7:5, 2:0] P4[7,4]
INT6 INT5 INT4 INT3 INT2 INT1 INT0	INTD0 INTC1 INTC0 INTB1 INTB0 INTA1 INTA0	P6.1 P6.3 P6.2 P6.3 P6.2 P6.0 P6.0

Each source has a trigger control bit TEA0,..TED1 (R242,EITR.0,..,7 Page 0) to select triggering on the rising or falling edge of the external pin. If the Trigger control bit is set to “1”, the corresponding pending bit IPA0,..,IPD1 (R243,EIPR.0,..,7 Page 0) is set on the input pin rising edge, if it is cleared, the pending bit is set on the falling edge of the input pin. Each source can be individually masked through the corresponding control bit IMA0,..,IMD1 (EIMR.7,..,0). See *Figure 51*.

10.6 DMA registers

As each peripheral DMA channel has its own specific control registers, the following register list should be considered as a general example. The names and register bit allocations shown here may be different from those found in the peripheral chapters.

DMA COUNTER POINTER REGISTER (DCPR)
Read/Write
Address set by Peripheral
Reset value: undefined

7							0
C7	C6	C5	C4	C3	C2	C1	RM

Bit 7:1 = **C[7:1]**: *DMA Transaction Counter Pointer.*

Software should write the pointer to the DMA Transaction Counter in these bits.

Bit 0 = **RM**: *Register File/Memory Selector.*
This bit is set and cleared by software.

0: DMA transactions are with memory (see also DAPR.DP)

1: DMA transactions are with the Register File

GENERIC EXTERNAL PERIPHERAL INTERRUPT AND DMA CONTROL (IDCR)
Read/Write
Address set by Peripheral
Reset value: undefined

7							0
		IP	DM	IM	PRL2	PRL1	PRL0

Bit 5 = **IP**: *Interrupt Pending*.

This bit is set by hardware when the Trigger Event occurs. It is cleared by hardware when the request is acknowledged. It can be set/cleared by software in order to generate/cancel a pending request.

0: No interrupt pending

1: Interrupt pending

Bit 4 = **DM**: *DMA Request Mask*.

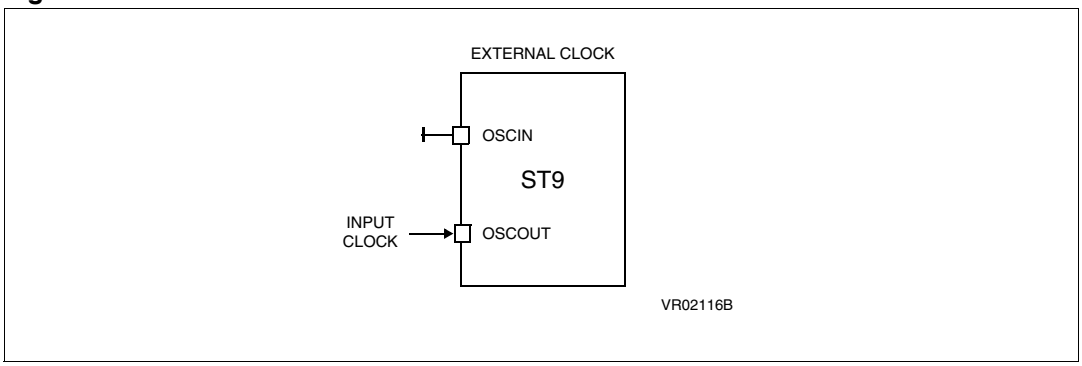
This bit is set and cleared by software. It is also cleared when the transaction counter reaches zero (unless SWAP mode is active).

0: No DMA request is generated when IP is set.

1: DMA request is generated when IP is set

Bit 3 = **IM**: *End of block Interrupt Mask*.
This bit is set and cleared by software.

Figure 68. External clock



Ceramic resonators

Murata Electronics CERALOCK resonators have been tested with the ST92F150 at 3, 3.68, 4 and 5 MHz. These recommended resonators have built-in capacitors (see *Table 40*).

The test circuit is shown in *Figure 69*.

Figure 69. Test circuit

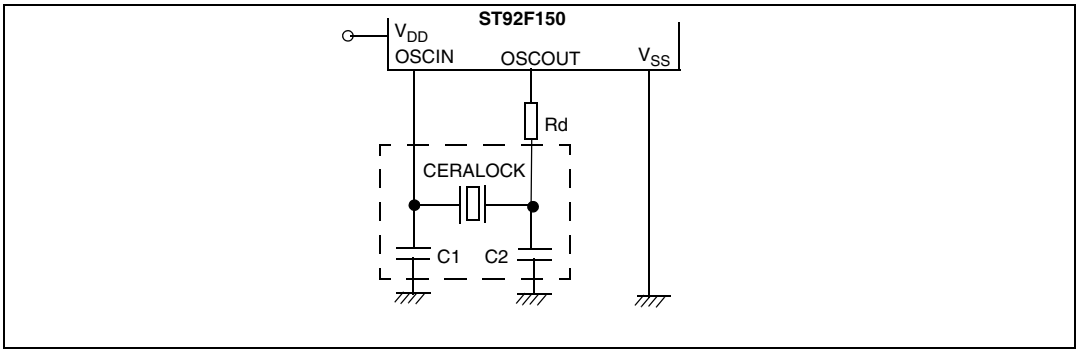


Table 40 shows the recommended conditions at different frequencies.

Table 40. Obtained results

Freq. (MHz)	Parts number	C1 (pF)	C2 (pF)	Rd (Ohm)
5	CSTCR5M00G55A-R0	39	39	0
	CSTCC5M00G56A-R0	47	47	0
4	CSTCR4M00G55A-R0	39	39	0
	CSTCC4M00G56A-R0	47	47	0
3	CSTCC3M00G56A-R0	47	47	0
3.68	CSTCC3M68G56A-R0	47	47	0

Advantages of using ceramic resonators:

CSTCR and CSTCC types have built-in loading capacitors.

Smallest loading capacitor resonators are recommended for standard applications.

Independently of the chosen configuration, when the user addresses the port as the destination register of an instruction, the port is written to and the data is transferred from the internal Data Bus to the Output Master Latches. When the port is addressed as the source register of an instruction, the port is read and the data (stored in the Input Latch) is transferred to the internal Data Bus.

When Px.n is programmed as an Input:
(See *Figure 80*).

- The Output Buffer is forced tristate.
- The data present on the I/O pin is sampled into the Input Latch at the beginning of each instruction execution.
- The data stored in the Output Master Latch is copied into the Output Slave Latch at the end of the execution of each instruction. Thus, if bit Px.n is reconfigured as an Output or Bidirectional, the data stored in the Output Slave Latch will be reflected on the I/O pin.

Table 42. Control bits

	Bit 7			Bit n				Bit 0
PxC2	PxC27			PxC2n				PxC20
PxC1	PxC17			PxC1n				PxC10
PxC0	PxC07			PxC0n				PxC00

Table 43. Port bit configuration table (n = 0, 1... 7; X = port number)

	General Purpose I/O Pins								A/D Pins
PXC2n	0	1	0	1	0	1	0	1	1
PXC1n	0	0	1	1	0	0	1	1	1
PXC0n	0	0	0	0	1	1	1	1	1
PXn Configuration	BID	BID	OUT	OUT	IN	IN	AF OUT	AF OUT	AF IN
PXn Output Type	WP OD	OD	PP	OD	HI-Z	HI-Z	PP	OD	HI-Z (1)
PXn Input Type	TTL (or Schmitt Trigger)	TTL (or Schmitt Trigger)	TTL (or Schmitt Trigger)	TTL (or Schmitt Trigger)	CMOS (or Schmitt Trigger)	TTL (or Schmitt Trigger)	TTL (or Schmitt Trigger)	TTL (or Schmitt Trigger)	Analog Input

1. For A/D Converter inputs.

Legend:
X = Port
n = Bit
AF = Alternate Function
BID = Bidirectional
CMOS= CMOS Standard Input Levels
HI-Z = High Impedance
IN = Input
OD = Open Drain
OUT = Output
PP = Push-Pull
TTL = TTL Standard Input Levels
WP = Weak Pull-up

Bit 2 = **OUTMD**: *Output Mode.*

This bit is set and cleared by software.

0: The output is toggled at every End of Count

1: The value of the WROUT bit is transferred to the output pin on every End Of Count if OUTEN=1.

Bit 1 = **WROUT**: *Write Out*.
The status of this bit is transferred to the Output pin when OUTMD is set; it is user definable to allow PWM output (on Reset WROUT is set).

Bit 0 = **OUTEN**: *Output Enable bit*.
This bit is set and cleared by software.

0: Disable output

1: Enable output

WAIT CONTROL REGISTER (WCR)
R252 - Read/Write
Register Page: 0
Reset value: 0111 1111 (7Fh)

7							0
x	WDGEN	x	x	x	x	x	x

Bit 6 = **WDGEN**: *Watchdog Enable* (active low).
Resetting this bit via software enters the Watchdog mode. Once reset, it cannot be set any more by the user program. At System Reset, the Watchdog mode is disabled.

Note: This bit is ignored if the Hardware Watchdog option is enabled by pin HW0SW1 (if available).

EXTERNAL INTERRUPT VECTOR REGISTER (EIVR)
R246 - Read/Write
Register Page: 0
Reset value: xxxx 0110 (x6h)

7							0
x	x	x	x	x	TLIS	IA0S	x

Bit 2 = **TLIS**: *Top Level Input Selection*.
This bit is set and cleared by software.

0: Watchdog End of Count is TL interrupt source

1: NMI is TL interrupt source

Bit 5 = **TOF** *Timer Overflow.*

0: No timer overflow (reset value).

1:The free running counter rolled over from FFFFh to 0000h. To clear this bit, first read the SR register, then read or write the low byte of the CR (CLR) register.

Note: Reading or writing the ACLR register does not clear TOF.

Bit 4 = **ICF2** *Input Capture Flag 2.*

0: No input capture (reset value).

1: An input capture has occurred. To clear this bit, first read the SR register, then read or write the low byte of the IC2R (IC2LR) register.

Bit 3 = **OCF2** *Output Compare Flag 2.*

0: No match (reset value).

1: The content of the free running counter has matched the content of the OC2R register. To clear this bit, first read the SR register, then read or write the low byte of the OC2R (OC2LR) register.

Bit 2:0 = Reserved, forced by hardware to 0.

CONTROL REGISTER 3 (CR3)

R255 - Read/Write
Register Page: 28
Reset Value: 0000 0000 (00h)

7							0
IC1IE	OC1IE	IC2IE	OC2IE	0	0	0	EFTIS

Bit 7 = **IC1IE** *Input Capture1 interrupt enable*

This bit is not significant if the ICIE bit in the CR1 register is set.

0: ICAP1 interrupt disabled

1: ICAP1 interrupt enabled

Bit 6 = **OC1IE** *output compare 1 interrupt enable*

This bit is not significant if the OCIE bit in the CR1 register is set.

0: OCMP1 interrupt disabled

1: OCMP1 interrupt enabled

Bit 5 = **IC2IE** *input capture 2 interrupt enable*

If an interrupt request (CM0 or CP0) is present before the corresponding pending bit is reset, an overrun condition occurs. This condition is flagged in two dedicated overrun bits, relating to the Comp0 and Capt0 sources, in the Timer Flag Register (T_FLAGR).

Timer DMA

Two Independent DMA channels, associated with Comp0 and Capt0 respectively, allow DMA transfers from Register File or Memory to the Comp0 Register, and from the Capt0 Register to Register File or Memory). If DMA is enabled, the Capt0 and Comp0 interrupts are generated by the corresponding DMA End of Block event. Their priority is set by hardware as follows:

- Compare 0 Destination — Lower Priority
- Capture 0 Source — Higher Priority

The two DMA request sources are independently maskable by the CP0D and CM0D DMA Mask bits in the IDMR register.

The two DMA End of Block interrupts are independently enabled by the CP0I and CM0I Interrupt mask bits in the IDMR register.

DMA pointers

The 6 programmable most significant bits of the DMA Counter Pointer Register (DCPR) and of the DMA Address Pointer Register (DAPR) are common to both channels (Comp0 and Capt0). The Comp0 and Capt0 Address Pointers are mapped as a pair in the Register File, as are the Comp0 and Capt0 DMA Counter pair.

In order to specify either the Capt0 or the Comp0 pointers, according to the channel being serviced, the Timer resets address bit 1 for CAPT0 and sets it for COMP0, when the D0 bit in the DCPR register is equal to zero (Word address in Register File). In this case (transfers between peripheral registers and memory), the pointers are split into two groups of adjacent Address and Counter pairs respectively.

For peripheral register to register transfers (selected by programming “1” into bit 0 of the DCPR register), only one pair of pointers is required, and the pointers are mapped into one group of adjacent positions.

The DMA Address Pointer Register (DAPR) is not used in this case, but must be considered reserved.

14.6.2 Main features

- Full duplex, asynchronous communications
- NRZ standard format (Mark/Space)
- Dual baud rate generator systems
- Independently programmable transmit and receive baud rates up to 700K baud.
- Programmable data word length (8 or 9 bits)
- Receive buffer full, Transmit buffer empty and End of Transmission flags
- Two receiver wake-up modes:
  - Address bit (MSB)
  - Idle line
- Muting function for multiprocessor configurations
- Separate enable bits for Transmitter and Receiver
- Three error detection flags:
  - Overrun error
  - Noise error
  - Frame error
- Five interrupt sources with flags:
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Idle line received
  - Overrun error detected
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Reduced power consumption mode
- LIN Master: 13-bit LIN Synch Break generation capability

14.6.3 General description

The interface is externally connected to another device by two pins (see *Figure 132*):

- TDO: Transmit Data Output. When the transmitter is disabled, the output pin is in high impedance. When the transmitter is enabled and nothing is to be transmitted, the TDO pin is at high level.
- RDI: Receive Data Input is the serial data input. Oversampling techniques are used for data recovery by discriminating between valid incoming data and noise.

Through these pins, serial data is transmitted and received as frames comprising:

- An Idle Line prior to transmission or reception
- A start bit
- A data word (8 or 9 bits) least significant bit first
- A Stop bit indicating that the frame is complete.

CPHA Bit is Set

The second edge on the SCK pin (falling edge if the CPOL bit is reset, rising edge if the CPOL bit is set) is the MSBit capture strobe. Data is latched on the occurrence of the first clock transition.

No write collision should occur even if the $\overline{SS}$ pin stays low during a transfer of several bytes (see *Figure 136*).

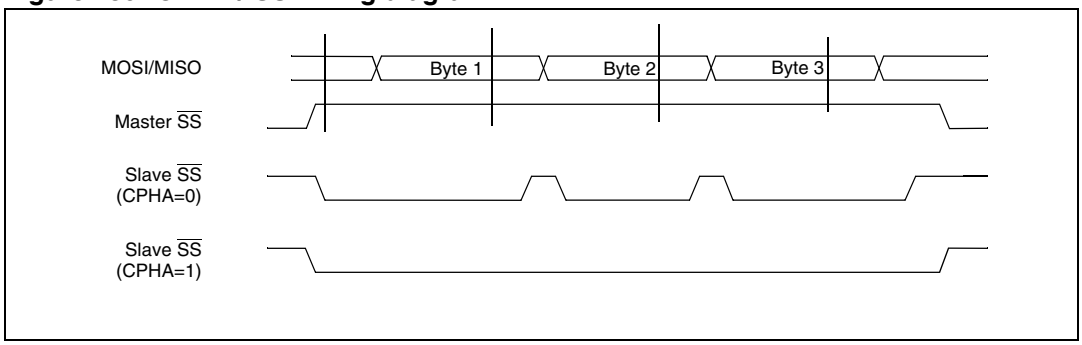
CPHA Bit is Reset

The first edge on the SCK pin (falling edge if CPOL bit is set, rising edge if CPOL bit is reset) is the MSBit capture strobe. Data is latched on the occurrence of the second clock transition.

This pin must be toggled high and low between each byte transmitted (see *Figure 136*).

To protect the transmission from a write collision a low value on the $\overline{SS}$ pin of a slave device freezes the data in its SPDR register and does not allow it to be altered. Therefore the $\overline{SS}$ pin must be high to write a new data byte in the SPDR without producing a write collision.

Figure 136. CPHA / $\overline{SS}$ timing diagram



Note: This bit has no effect on DMA transfer.

Table 87. I²C bus register map and reset values

Address (Hex.)	Register name	7	6	5	4	3	2	1	0
F0h	I2CCR Reset Value	- 0	- 0	PE 0	ENGC 0	START 0	ACK 0	STOP 0	ITE 0
F1h	I2CSR1 Reset Value	EVF 0	ADD10 0	TRA 0	BUSY 0	BTF 0	ADSL 0	M/SL 0	SB 0
F2h	I2CSR2 Reset Value	- 0	0 0	ADDTX 0	AF 0	STOPF 0	ARLO 0	BERR 0	GCAL 0
F3h	I2CCCR Reset Value	FM/SM 0	CC6 0	CC5 0	CC4 0	CC3 0	CC2 0	CC1 0	CC0 0
F4h	I2COAR1 Reset Value	ADD7 0	ADD6 0	ADD5 0	ADD4 0	ADD3 0	ADD2 0	ADD1 0	ADD0 0
F5h	I2COAR2 Reset Value	FREQ1 0	FREQ0 0	EN10BIT 0	FREQ2 0	0 0	ADD9 0	ADD8 0	0 0
F6h	I2CDR Reset Value	DR7 0	DR6 0	DR5 0	DR4 0	DR3 0	DR2 0	DR1 0	DR0 0
F7h	I2CADR Reset Value	ADR7 1	ADR6 0	ADR5 1	ADR4 0	ADR3 0	ADR2 0	ADR1 0	ADR0 0
F8h	I2CISR Reset Value	DMASTOP 1	PRL2 X	PRL1 X	PRL0 X	X	IERRP X	IRXP X	ITXP X
F9h	I2CIVR Reset Value	V7 X	V6 X	V5 X	V4 X	V3 X	EV2 X	EV1 X	0 0
FAh	I2CRDAP Reset Value	RA7 X	RA6 X	RA5 X	RA4 X	RA3 X	RA2 X	RA1 X	RPS X
FBh	I2CRDC Reset Value	RC7 X	RC6 X	RC5 X	RC4 X	RC3 X	RC2 X	RC1 X	RF/MEM X
FCh	I2CTDAP Reset Value	TA7 X	TA6 X	TA5 X	TA4 X	TA3 X	TA2 X	TA1 X	TPS X

transmitted out the VPWO pin. It then transmits the byte contained in the TXDATA register, then the computed CRC byte is transmitted. VPWO is then set to a passive state. If the J1850 bus is not idle and the J1850 transmitter has not been locked out by loss of arbitration, then the TXDATA byte is transferred to the serial output shift register for transmission immediately on completion of any previously transmitted data. After completion of the TXDATA byte the computed CRC byte is transferred out the VPWO pin and then the VPWO pin is set passive to time an EOD symbol.
Special Conditions for MSG+CRC Transmit:

- 1) A MSG+CRC opcode cannot be queued on top of an executing IFR3 opcode. If so, then TRA is set, and TDUF will get set because the transmit state machine will be expecting more data, then the inverted CRC is appended to this frame. Also, no message byte will be sent on the next frame.
- 2) If NFL=0, a MSG+CRC can only be queued if Received Byte Count for this frame <=10 otherwise the TRA will get set, and TDUF will get set because the state machine will be expecting more data, so the transmit machine will send the inverted CRC after the byte which is presently transmitting. Also, no message byte will be sent on the next frame.

Caution: Caution should be taken when TRA gets set in these cases because the TDUF error sequence may engage before the user program has a chance to rewrite the TXOP register with the correct opcode. If a TDUF error occurs, a subsequent MSG+CRC write to the TXOP register will be used as the first byte of the next frame.

IFR1, In-Frame Response Type 1 opcode.
The In-frame Response Type 1 (IFR 1) opcode is written if the user program wants to transmit a physical address byte (contained in the PADDR register) in response to a message that is currently being received.
The user program decides to set up an IFR1 upon receiving a certain portion of the data byte string of an incoming message. No write of the TXDATA register is required. The IFR1 gets its data byte from the PADDR register.
The JBLPD block will enable the transmission of the IFR1 on these conditions:

- 1) The CRC check is valid (otherwise the CRCE is set)
- 2) The received message length is valid if enabled (otherwise the TRA is set)
- 3) A valid EOD minimum symbol is received (otherwise the IFD may eventually get set due to byte synchronization errors)
- 4) If NFL = 0 & Received Byte Count for this frame <=11 (otherwise TRA is set)
- 5) If not presently executing an MSG, IFR3, opcode (otherwise TRA is set, and TDUF will get set because the transmit state machine will be expecting more data, so the inverted CRC will be appended to this frame)
- 6) If not presently executing an IFR1, IFR2, or IFR3+CRC opcode otherwise TRA is set (but no TDUF)
- 7) If not presently receiving an IFR portion of a frame, otherwise TRA is set.

The IFR1 byte is then attempted according to the procedure described in section “Transmitting a type 1 IFR”.

Note: If an IFR1 opcode is written, a queued MSG or MSG+CRC is overridden by the IFR1.

IFR2, In-Frame Response Type 2 opcode.
The In-frame Response Type 2 (IFR2) opcode is set if the user program wants to transmit a physical address byte (contained in the PADDR register) in response to a message that is currently being received.

Bit 7:0 = **DATA[7:0]** *Data*
A data byte of the message. A message can contain from 0 to 8 data bytes.

MAILBOX TIME STAMP LOW REGISTER (MTSLR)

Read / Write
Reset Value: xxxx xxxx (xxh)

7							0
TIME7	TIME6	TIME5	TIME4	TIME3	TIME2	TIME1	TIME0

Bit 7:0 = **TIME[7:0]** *Message Time Stamp Low*
This fields contains the low byte of the 16-bit timer value captured at the SOF detection.

MAILBOX TIME STAMP HIGH REGISTER (MTSHR)

Read / Write
Reset Value: xxxx xxxx (xxh)

7							0
TIME15	TIME14	TIME13	TIME12	TIME11	TIME10	TIME9	TIME8

Bit 7:0 = **TIME[15:8]** *Message Time Stamp High*
This field contains the high byte of the 16-bit timer value captured at the SOF detection.

CAN Filter Registers

CAN FILTER CONFIGURATION REG.0 (CFCR0)

All bits of this register are set and cleared by software.
Read / Write
Reset Value: 0000 0000 (00h)

7							0
FFA1	FSC11	FSC10	FACT1	FFA0	FSC01	FSC00	FACT0

Note: To modify the FFAx and FSCx bits, the bxCAN must be in INIT mode.

Bit 7 = **FFA1** *Filter FIFO Assignment for Filter 1*
The message passing through this filter will be stored in the specified FIFO.
0: Filter assigned to FIFO 0
1: Filter assigned to FIFO 1

Bit 6:5 = **FSC1[1:0]** *Filter Scale Configuration*
These bits define the scale configuration of Filter 1.

Bit 4 = **FACT1** *Filter Active*
The software sets this bit to activate Filter 1. To modify the Filter 1 registers (CF1R[7:0]), the FACT1 bit must be cleared.

Figure 207. Workaround 2 in assembler

```
asm ("                          /*                              Bytes/cycles            */
       spp #48                  /*  set CAN0_CTRL page          2/4                     */
                                /*  Use spp #36 for CAN1
       ld     r0, R244          /*  For FIFO 0                  2/4                     */
                                /*  NB: Replace R244 with R245 for FIFO 1               */
       and    r0, #3            /*                              3/6                     */
       cp     r0, #2            /*                              3/6                     */
       jxnz   _release          /*  (JRNE instruction)          2/6                     */
                                /*  if FMP is not 2 then FIFO                           */
                                /*  release can be done                                 */

       pushw  RR232             /*  push working group          2/8 or 10               */
       srp    #31               /*  set group F as working group 2/4                    */
       btjf   r1.5, _release    /*  REC bit of CMSR register    3/6 or 10 if jmp        */

       btjf   r12.3, _release   /*  sample RX bit for 8 bit time 3/6 or 10 if jmp       */
       btjf   r12.3, _release   /*  ie. 11 btjf instructions    3/6 or 10 if jmp        */
       btjf   r12.3, _release   /*                              3/6 or 10 if jmp        */
       btjf   r12.3, _release   /*                              3/6 or 10 if jmp        */
       btjf   r12.3, _release   /*                              3/6 or 10 if jmp        */
       btjf   r12.3, _release   /*                              3/6 or 10 if jmp        */
       btjf   r12.3, _release   /*                              3/6 or 10 if jmp        */
       btjf   r12.3, _release   /*                              3/6 or 10 if jmp        */
       btjf   r12.3, _release   /*                              3/6 or 10 if jmp        */
       btjf   r12.3, _release   /*                              3/6 or 10 if jmp        */
       btjf   r12.3, _release   /*                              3/6 or 10 if jmp        */

_release:    or R244, #32        /*  set RFOM bit of CRFR0 register  3/6                 */
                                /*  NB: Replace R244 with R245 for FIFO 1               */
       popw   RR232             /*  restore previous working group  2/10                */
");
```

17.7 MFT DMA mask bit reset when MFT0 DMA priority level is set to 0

Introduction

The MultiFunction Timer is a 16-bit timer with Input Capture and Output Compare modes. In Input Capture mode, the timer value is saved when an external event occurs. In Output Compare mode, the timer changes an I/O pin level when it reaches the Compare Register value.

In these two modes the event (Input Capture or Output Compare) may generate an interrupt or request a Direct Memory Access.

- In interrupt Input Capture mode (or Output Compare mode), the interrupt routine saves the counter in the RAM or the Register File (or updates the compare register from a location in RAM or in the Register File).
- In DMA mode these transfers are done automatically.

The choice between Interrupt or DMA modes is defined by the CP0D and CM0D bits (bit 6 and bit 3 in the IDMR register, R255 page 10/8).

CP0D: Capture 0 DMA Mask. Capture on REG0R DMA is enabled when CP0D = 1.

CM0D: Compare 0 DMA Mask. Compare on CMP0R DMA is enabled when CM0D = 1.

In DMA mode a DMA counter register and a DMA address register define the location and the size of the memory block (RAM or Reg. File) involved in these transfers.