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Details	
Product Status	Obsolete
Number of LABs/CLBs	11024
Number of Logic Elements/Cells	99216
Total RAM Bits	8183808
Number of I/O	1040
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1704-BBGA, FCBGA
Supplier Device Package	1704-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp100-6ff1704c

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/13/02	2.0	New Virtex-II Pro family members. New timing parameters per speedsfile **v1.62**.
09/03/02	2.1	Updates to Table 1 and Table 3. Processor Block information added to Table 4.
09/27/02	2.2	In Table 1, correct max number of XC2VP30 I/Os to 644.
11/20/02	2.3	Add bullet items for 3.3V I/O features.
01/20/03	2.4	• In Table 3, add FG676 package option for XC2VP20, XC2VP30, and XC2VP40. • Remove FF1517 package option for XC2VP40.
03/24/03	2.4.1	• Correct number of single-ended I/O standards from 19 to 22. • Correct minimum RocketIO serial speed from 622 Mbps to 600 Mbps.
08/25/03	2.4.2	• Add footnote referring to XAPP659 to callout for 3.3V I/O standards on page 4.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Table 1: Corrected number of RocketIO transceiver blocks for XC2VP40. • Section Virtex-II Pro Platform FPGA Technology (All Devices): Updated number of differential standards supported from six to ten. • Section Input/Output Blocks (IOBs): Added text stating that differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards. • Figure 1: Added note stating that -7 devices are not available in Industrial grade.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/30/04	4.0	Merged in DS110-1 (Module 1 of Virtex-II Pro X data sheet). Added information on available Pb-free packages.
11/17/04	4.1	*No changes in Module 1 for this revision.*
03/01/05	4.2	Table 3: Corrected number of RocketIO transceivers for XC2VP7-FG456.
06/20/05	4.3	*No changes in Module 1 for this revision.*
09/15/05	4.4	• Changed all instances of 10.3125 Gb/s (RocketIO transceiver maximum bit rate) to 6.25 Gb/s. • Changed all instances of 412.5 Gb/s (RocketIO X transceiver maximum multi-channel raw data transfer rate) to 250 Gb/s.
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s. • Changed maximum performance for -7 Virtex-II Pro X MGT (Table 4) to N/A.
03/05/07	4.6	*No changes in Module 1 for this revision.*
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner.

Table 15: **SelectIO-Ultra Differential Buffers With On-Chip Termination**

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
LVDS 2.5V	LVDS_25	LVDS_25_DCI
LVDS Extended 2.5V	LVDSEXT_25	LVDSEXT_25_DCI

Figure 28 provides examples illustrating the use of the HSTL_I_DCI, HSTL_II_DCI, HSTL_III_DCI, and HSTL_IV_DCI I/O standards. For a complete list, see the ***Virtex-II Pro Platform FPGA User Guide***.

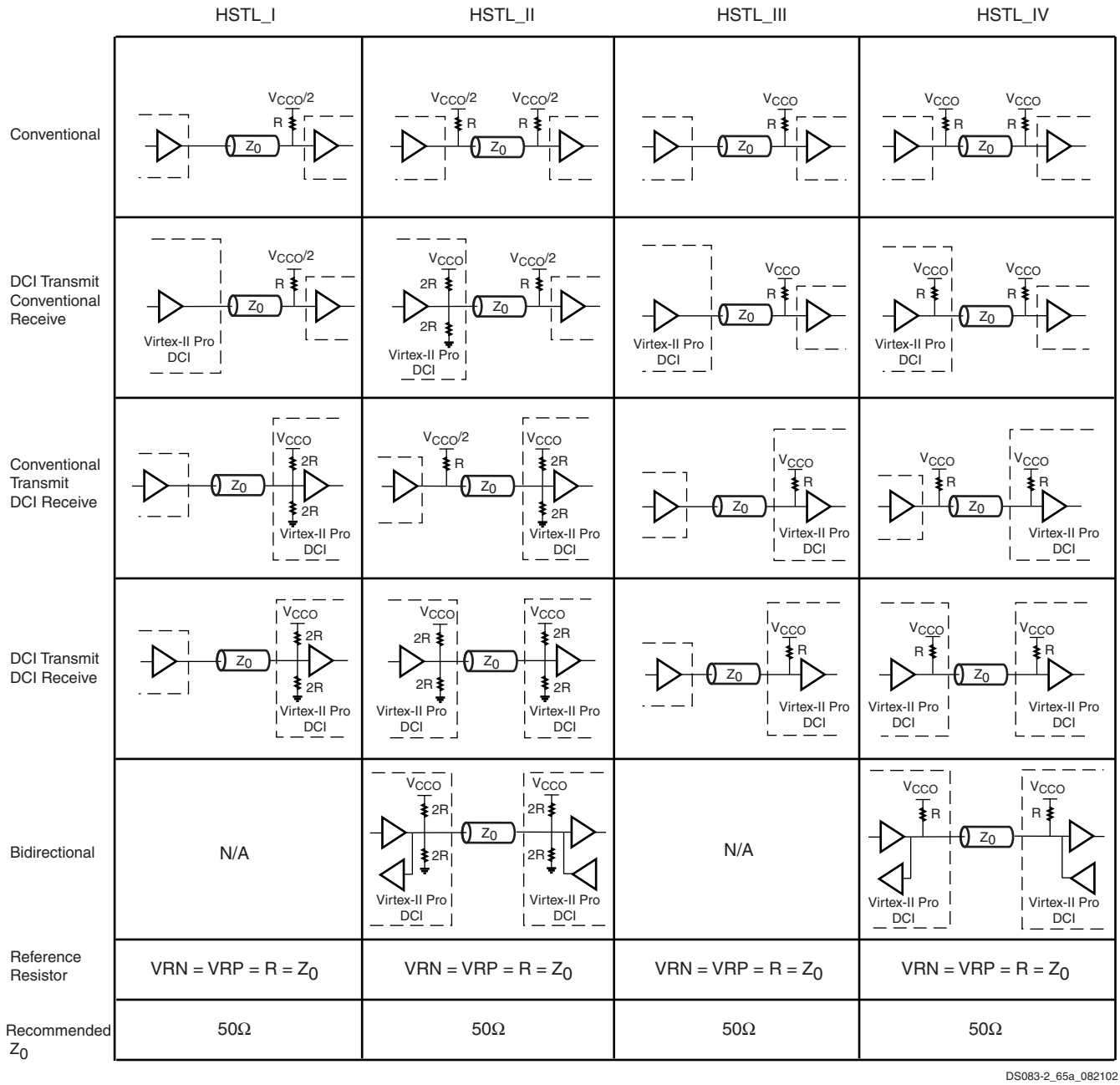


Figure 28: **HSTL DCI Usage Examples**

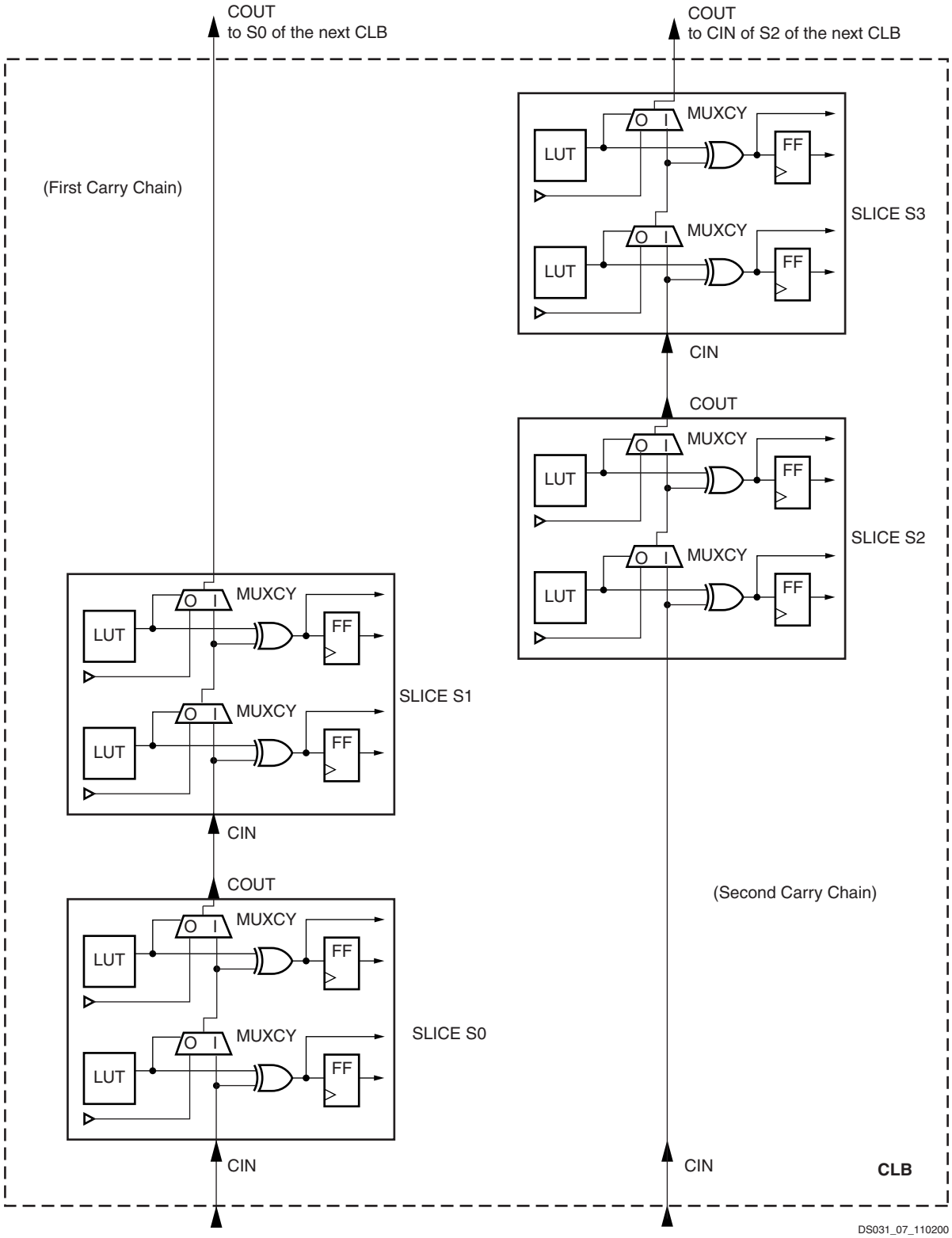


Figure 42: **Fast Carry Logic Path**

Each block SelectRAM+ cell is a fully synchronous memory, as illustrated in Figure 48. The two ports have independent inputs and outputs and are independently clocked.

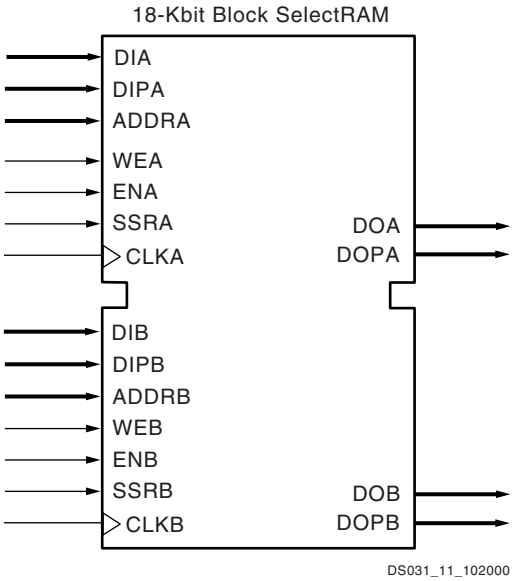


Figure 48: **18 Kb Block SelectRAM+ in Dual-Port Mode**

Port Aspect Ratios

Table 23 shows the depth and the width aspect ratios for the 18 Kb block SelectRAM+ resource. Virtex-II Pro block SelectRAM+ also includes dedicated routing resources to provide an efficient interface with CLBs, block SelectRAM+, and multipliers.

Table 23: **18 Kb Block SelectRAM+ Port Aspect Ratio**

Width	Depth	Address Bus	Data Bus	Parity Bus
1	16,384	ADDR[13:0]	DATA[0]	N/A
2	8,192	ADDR[12:0]	DATA[1:0]	N/A
4	4,096	ADDR[11:0]	DATA[3:0]	N/A
9	2,048	ADDR[10:0]	DATA[7:0]	Parity[0]
18	1,024	ADDR[9:0]	DATA[15:0]	Parity[1:0]
36	512	ADDR[8:0]	DATA[31:0]	Parity[3:0]

Read/Write Operations

The Virtex-II Pro block SelectRAM+ read operation is fully synchronous. An address is presented, and the read operation is enabled by control signal ENA or ENB. Then, depending on clock polarity, a rising or falling clock edge causes the stored data to be loaded into output registers.

The write operation is also fully synchronous. Data and address are presented, and the write operation is enabled by control signals WEA and WEB in addition to ENA or ENB. Then, again depending on the clock input mode, a rising or falling clock edge causes the data to be loaded into the memory cell addressed.

A write operation performs a simultaneous read operation. Three different options are available, selected by configuration:

1. **WRITE_FIRST**

   The WRITE_FIRST option is a transparent mode. The same clock edge that writes the data input (DI) into the memory also transfers DI into the output registers DO, as shown in Figure 49.

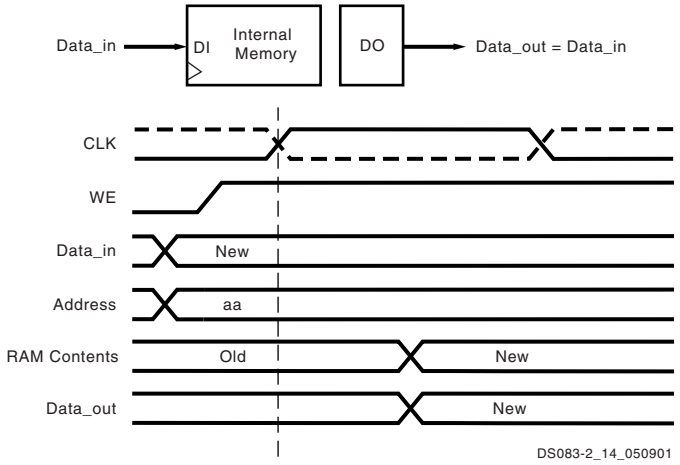


Figure 49: **WRITE_FIRST Mode**

2. **READ_FIRST**

The READ_FIRST option is a read-before-write mode.

The same clock edge that writes data input (DI) into the memory also transfers the prior content of the memory cell addressed into the data output registers DO, as shown in Figure 50.

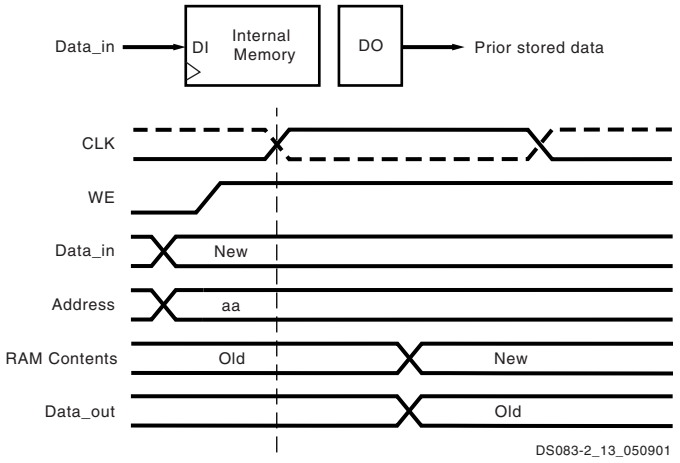


Figure 50: **READ_FIRST Mode**

Table 17: **Processor Block Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (CPMC405CLOCK)					
Device Control Register Bus control inputs	$T_{PCCK\_}DCR/T_{PCKC\_}DCR$	0.38/–0.18	0.44/–0.20	0.48/–0.23	ns, min
Device Control Register Bus data inputs	$T_{PDCK\_}DCR/T_{PCKD\_}DCR$	0.65/–0.01	0.75/–0.01	0.82/–0.02	ns, min
Clock and Power Management control inputs	$T_{PCCK\_}CPM/T_{PCKC\_}CPM$	0.16/ 0.03	0.19/ 0.03	0.20/ 0.03	ns, min
Reset control inputs	$T_{PCCK\_}RST/T_{PCKC\_}RST$	0.16/ 0.03	0.19/ 0.03	0.20/ 0.03	ns, min
Debug control inputs	$T_{PCCK\_}DBG/T_{PCKC\_}DBG$	0.27/ 0.30	0.31/ 0.35	0.34/ 0.38	ns, min
Trace control inputs	$T_{PCCK\_}TRC/T_{PCKC\_}TRC$	1.37/–0.41	1.57/–0.48	1.73/–0.52	ns, min
External Interrupt Controller control inputs	$T_{PCCK\_}EIC/T_{PCKC\_}EIC$	0.57/–0.22	0.66/–0.25	0.72/–0.27	ns, min
Clock to Out					
Device Control Register Bus control outputs	$T_{PCKCO\_}DCR$	1.32	1.52	1.67	ns, max
Device Control Register Bus address outputs	$T_{PCKAO\_}DCR$	1.72	1.98	2.17	ns, max
Device Control Register Bus data outputs	$T_{PCKDO\_}DCR$	1.76	2.02	2.22	ns, max
Clock and Power Management control outputs	$T_{PCKCO\_}CPM$	1.26	1.45	1.59	ns, max
Reset control outputs	$T_{PCKCO\_}RST$	1.32	1.51	1.66	ns, max
Debug control outputs	$T_{PCKCO\_}DBG$	1.94	2.22	2.44	ns, max
Trace control outputs	$T_{PCKCO\_}TRC$	1.35	1.56	1.71	ns, max
Clock					
CPMC405CLOCK minimum pulse width, high	T_{CPWH}	1.25	1.42	1.66	ns, min
CPMC405CLOCK minimum pulse width, low	T_{CPWL}	1.25	1.42	1.66	ns, min

Table 18: **Processor Block PLB Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (PLBCLK)					
Processor Local Bus(ICU/DCU) control inputs	$T_{PCCK\_}PLB/T_{PCKC\_}PLB$	0.98/ 0.18	1.12/ 0.21	1.23/ 0.23	ns, min
Processor Local Bus (ICU/DCU) data inputs	$T_{PDCK\_}PLB/T_{PCKD\_}PLB$	0.62/ 0.16	0.71/ 0.18	0.78/ 0.20	ns, min
Clock to Out					
Processor Local Bus(ICU/DCU) control outputs	$T_{PCKCO\_}PLB$	1.34	1.54	1.69	ns, max
Processor Local Bus(ICU/DCU) address bus outputs	$T_{PCKAO\_}PLB$	1.16	1.34	1.47	ns, max
Processor Local Bus(ICU/DCU) data bus outputs	$T_{PCKDO\_}PLB$	1.44	1.65	1.81	ns, max

IOB Input Switching Characteristics Standard Adjustments

Table 36 gives all standard-specific data input delay adjustments.

Table 36: **IOB Input Switching Characteristics Standard Adjustments**

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	T_{ILVTTL}	0.07	0.08	0.09	ns
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	$T_{ILVCMOS33}$	0.04	0.05	0.05	ns
LVCMOS, 2.5V	LVCMOS25	$T_{ILVCMOS25}$	0.00	0.00	0.00	ns
LVCMOS, 1.8V	LVCMOS18	$T_{ILVCMOS18}$	0.29	0.33	0.36	ns
LVCMOS, 1.5V	LVCMOS15	$T_{ILVCMOS15}$	0.36	0.41	0.45	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{ILVDS_25}	0.31	0.36	0.40	ns
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	$T_{ILVDSEXT\_25}$	0.33	0.37	0.41	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{IULVDS_25}	0.31	0.36	0.40	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{IBLVDS_25}	0.00	0.00	0.00	ns
LDT (HyperTransport), 2.5V	LDT_25	T_{ILDT_25}	0.31	0.36	0.40	ns
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	$T_{ILVPECL\_25}$	0.69	0.80	0.88	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{IPCI33_3}	0.14	0.16	0.18	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{IPCI66_3}	0.15	0.17	0.19	ns
PCI-X, 133 MHz, 3.3V	PCIX	T_{IPCIX}	0.12	0.13	0.15	ns
GTL (Gunning Transceiver Logic)	GTL	T_{IGTL}	0.59	0.68	0.74	ns
GTL Plus	GTLP	T_{IGTLP}	0.63	0.72	0.79	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{IHSTL_I}	0.59	0.68	0.75	ns
HSTL, Class II	HSTL_II	T_{IHSTL_II}	0.59	0.68	0.75	ns
HSTL, Class III	HSTL_III	T_{IHSTL_III}	0.57	0.66	0.72	ns
HSTL, Class IV	HSTL_IV	T_{IHSTL_IV}	0.58	0.67	0.74	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{IHSTL\_I\_18}$	0.57	0.65	0.72	ns
HSTL, Class II, 1.8V	HSTL_II_18	$T_{IHSTL\_II\_18}$	0.55	0.63	0.69	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{IHSTL\_III\_18}$	0.56	0.64	0.70	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{IHSTL\_IV\_18}$	0.57	0.65	0.71	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{ISSTL18\_I}$	0.62	0.72	0.79	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{ISSTL18\_II}$	0.64	0.73	0.81	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{ISSTL2_I}	0.62	0.72	0.79	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{ISSTL2_II}	0.64	0.73	0.81	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{ILVDCI_33}	–0.05	–0.05	–0.06	ns
LVDCI, 2.5V	LVDCI_25	T_{ILVDCI_25}	0.00	0.00	0.00	ns
LVDCI, 1.8V	LVDCI_18	T_{ILVDCI_18}	0.07	0.09	0.09	ns
LVDCI, 1.5V	LVDCI_15	T_{ILVDCI_15}	0.13	0.15	0.17	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{ILVDCI\_DV2\_25}$	0.00	0.00	0.00	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{ILVDCI\_DV2\_18}$	0.07	0.09	0.09	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{ILVDCI\_DV2\_15}$	0.13	0.15	0.17	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{IHSLVDCI\_15}$	0.59	0.68	0.75	ns

FG256/FGG256 Fine-Pitch BGA Package

As shown in Table 5, XC2VP2 and XC2VP4 Virtex-II Pro devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in each of these devices are identical. Following this table are the FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
0	IO_L01N_0/VRP_0	C2
0	IO_L01P_0/VRN_0	C3
0	IO_L02N_0	B3
0	IO_L02P_0	C4
0	IO_L03N_0	A2
0	IO_L03P_0/VREF_0	A3
0	IO_L06N_0	D5
0	IO_L06P_0	C5
0	IO_L07P_0	D6
0	IO_L09N_0	E6
0	IO_L09P_0/VREF_0	E7
0	IO_L69N_0	D7
0	IO_L69P_0/VREF_0	C7
0	IO_L74N_0/GCLK7P	D8
0	IO_L74P_0/GCLK6S	C8
0	IO_L75N_0/GCLK5P	B8
0	IO_L75P_0/GCLK4S	A8
1	IO_L75N_1/GCLK3P	A9
1	IO_L75P_1/GCLK2S	B9
1	IO_L74N_1/GCLK1P	C9
1	IO_L74P_1/GCLK0S	D9
1	IO_L69N_1/VREF_1	C10
1	IO_L69P_1	D10
1	IO_L09N_1/VREF_1	E10
1	IO_L09P_1	E11
1	IO_L07N_1	D11
1	IO_L06N_1	C12
1	IO_L06P_1	D12
1	IO_L03N_1/VREF_1	A14
1	IO_L03P_1	A15

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

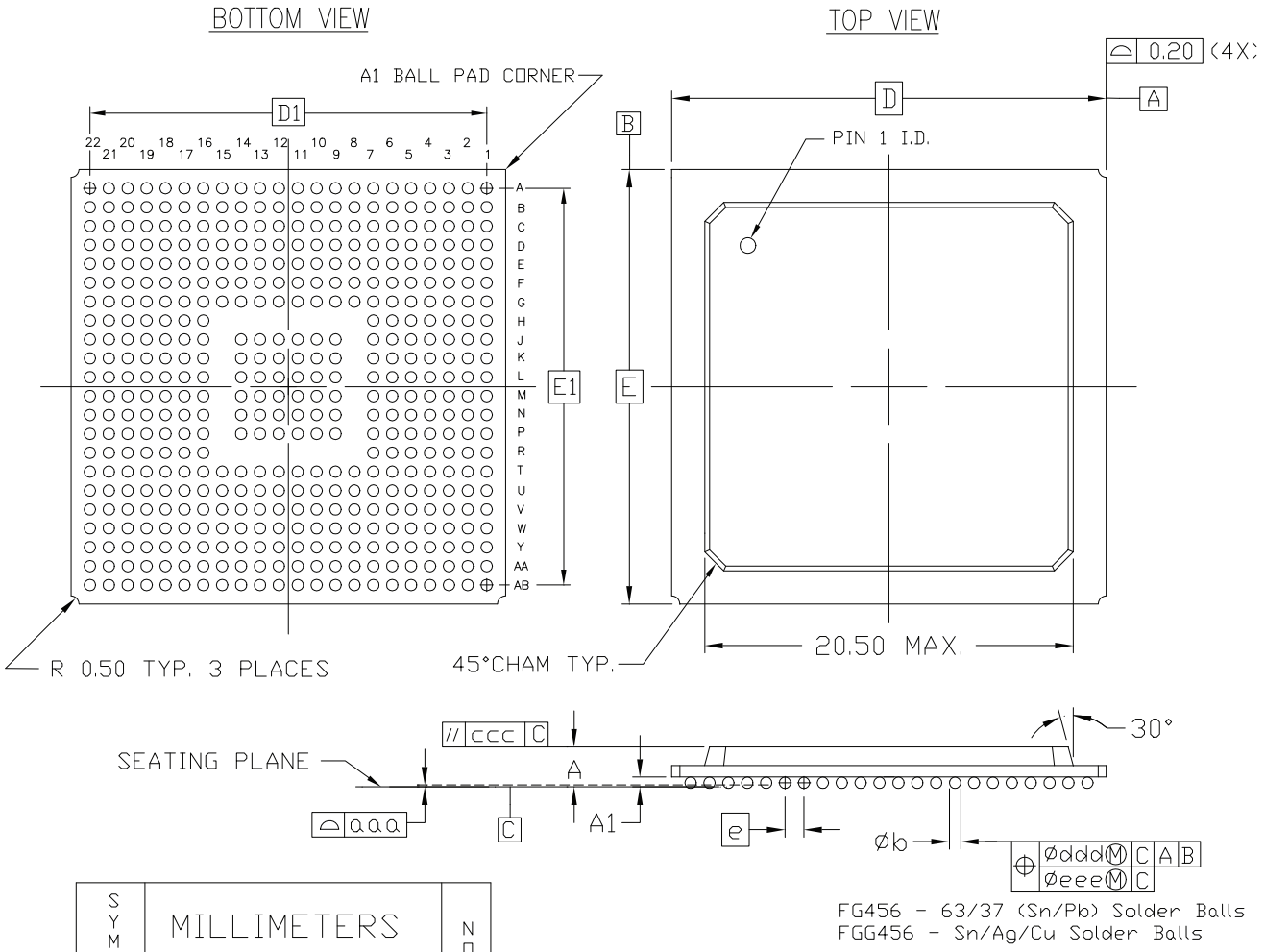
Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L06N_6	V1			
6	IO_L43P_6	U4	NC		
6	IO_L43N_6	U3	NC		
6	IO_L45P_6	U2	NC		
6	IO_L45N_6/VREF_6	U1	NC		
6	IO_L47P_6	U5	NC		
6	IO_L47N_6	T5	NC		
6	IO_L48P_6	T4	NC		
6	IO_L48N_6	T3	NC		
6	IO_L49P_6	T2	NC		
6	IO_L49N_6	T1	NC		
6	IO_L51P_6	R4	NC		
6	IO_L51N_6/VREF_6	R3	NC		
6	IO_L53P_6	R2	NC		
6	IO_L53N_6	R1	NC		
6	IO_L54P_6	R5	NC		
6	IO_L54N_6	P6	NC		
6	IO_L55P_6	P4	NC		
6	IO_L55N_6	P3	NC		
6	IO_L57P_6	P2	NC		
6	IO_L57N_6/VREF_6	P1	NC		
6	IO_L59P_6	P5	NC		
6	IO_L59N_6	N5	NC		
6	IO_L60P_6	N4	NC		
6	IO_L60N_6	N3	NC		
6	IO_L85P_6	N2			
6	IO_L85N_6	N1			
6	IO_L87P_6	N6			
6	IO_L87N_6/VREF_6	M6			
6	IO_L89P_6	M5			
6	IO_L89N_6	M4			
6	IO_L90P_6	M3			
6	IO_L90N_6	M2			
7	IO_L90P_7	L2			
7	IO_L90N_7	L3			
7	IO_L88P_7	L4			

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	GND	L11			
N/A	GND	L10			
N/A	GND	K9			
N/A	GND	K14			
N/A	GND	K13			
N/A	GND	K12			
N/A	GND	K11			
N/A	GND	K10			
N/A	GND	J9			
N/A	GND	J14			
N/A	GND	J13			
N/A	GND	J12			
N/A	GND	J11			
N/A	GND	J10			
N/A	GND	E5			
N/A	GND	E18			
N/A	GND	D4			
N/A	GND	D19			
N/A	GND	C3			
N/A	GND	C20			
N/A	GND	AB22			
N/A	GND	AB12			
N/A	GND	AB1			
N/A	GND	A22			
N/A	GND	A11			
N/A	GND	A1			

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

FG456/FGG456 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A			2.60	3
A_1	0.35	0.50	0.60	
D/E	23.00 BSC			
D_1/E_1	21.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	22			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. NOMINAL 'A' DIMENSION IS TYPICALLY 2.20mm.
4. CONFORMS TO JEDEC MS-034-AAJ-1 (DEPOPULATED)

Figure 2: **FG456/FGG456 Fine-Pitch BGA Package Specifications**

FG676/FGG676 Fine-Pitch BGA Package

As shown in Table 7, XC2VP20, XC2VP30, and XC2VP40 Virtex-II Pro devices are available in the FG676/FGG676 fine-pitch BGA package. The pins in these devices are the same, except for the differences shown in the "No Connects" column. Following this table are the FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
0	IO_L01N_0/VRP_0	E5			
0	IO_L01P_0/VRN_0	D5			
0	IO_L02N_0	E6			
0	IO_L02P_0	D6			
0	IO_L03N_0	G7			
0	IO_L03P_0/VREF_0	F7			
0	IO_L05_0/No_Pair	E7			
0	IO_L06N_0	D7			
0	IO_L06P_0	C7			
0	IO_L07N_0	H8			
0	IO_L07P_0	G8			
0	IO_L09N_0	F8			
0	IO_L09P_0/VREF_0	E8			
0	IO_L37N_0	B8			
0	IO_L37P_0	A8			
0	IO_L39N_0	H9			
0	IO_L39P_0	G9			
0	IO_L43N_0	F9			
0	IO_L43P_0	E9			
0	IO_L45N_0	D9			
0	IO_L45P_0/VREF_0	C9			
0	IO_L46N_0	H10			
0	IO_L46P_0	H11			
0	IO_L48N_0	E10			
0	IO_L48P_0	E11			
0	IO_L49N_0	D10			
0	IO_L49P_0	C10			
0	IO_L50_0/No_Pair	G11			
0	IO_L53_0/No_Pair	F11			
0	IO_L54N_0	J12			
0	IO_L54P_0	H12			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
2	IO_L58N_2/VREF_2	M21			
2	IO_L58P_2	N21			
2	IO_L60N_2	M22			
2	IO_L60P_2	M23			
2	IO_L85N_2	M25			
2	IO_L85P_2	M26			
2	IO_L86N_2	N18			
2	IO_L86P_2	N19			
2	IO_L88N_2/VREF_2	N22			
2	IO_L88P_2	N23			
2	IO_L90N_2	N24			
2	IO_L90P_2	N25			
3	IO_L90N_3	P25			
3	IO_L90P_3	P24			
3	IO_L89N_3	P23			
3	IO_L89P_3	P22			
3	IO_L87N_3/VREF_3	P19			
3	IO_L87P_3	P18			
3	IO_L85N_3	R26			
3	IO_L85P_3	R25			
3	IO_L60N_3	R23			
3	IO_L60P_3	R22			
3	IO_L59N_3	P21			
3	IO_L59P_3	R21			
3	IO_L57N_3/VREF_3	R19			
3	IO_L57P_3	R18			
3	IO_L55N_3	T26			
3	IO_L55P_3	T25			
3	IO_L54N_3	T22			
3	IO_L54P_3	T21			
3	IO_L53N_3	R20			
3	IO_L53P_3	T20			
3	IO_L51N_3/VREF_3	U26			
3	IO_L51P_3	U25			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
3	IO_L48N_3	W1	NC		
3	IO_L48P_3	W2	NC		
3	IO_L47N_3	W3	NC		
3	IO_L47P_3	W4	NC		
3	IO_L46N_3	W5	NC		
3	IO_L46P_3	W6	NC		
3	IO_L45N_3/VREF_3	Y1	NC		
3	IO_L45P_3	AA1	NC		
3	IO_L44N_3	Y3	NC		
3	IO_L44P_3	Y4	NC		
3	IO_L43N_3	Y5	NC		
3	IO_L43P_3	Y6	NC		
3	IO_L42N_3	AA2	NC	NC	NC
3	IO_L42P_3	AA3	NC	NC	NC
3	IO_L41N_3	AA4	NC	NC	NC
3	IO_L41P_3	AA5	NC	NC	NC
3	IO_L39N_3/VREF_3	AB1	NC	NC	NC
3	IO_L39P_3	AB2	NC	NC	NC
3	IO_L06N_3	AB3			
3	IO_L06P_3	AB4			
3	IO_L05N_3	AC1			
3	IO_L05P_3	AC2			
3	IO_L04N_3	AD1			
3	IO_L04P_3	AD2			
3	IO_L03N_3/VREF_3	AE1			
3	IO_L03P_3	AF2			
3	IO_L02N_3	AC3			
3	IO_L02P_3	AD4			
3	IO_L01N_3/VRP_3	AE3			
3	IO_L01P_3/VRN_3	AF3			
4	IO_L01N_4/BUSY/DOUT(1)	AC6			
4	IO_L01P_4/INIT_B	AD6			
4	IO_L02N_4/D0/DIN(1)	AB7			
4	IO_L02P_4/D1	AC7			
4	IO_L03N_4/D2	AA7			
4	IO_L03P_4/D3	AA8			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
1	IO_L37N_1	G13				
1	IO_L37P_1	H13				
1	IO_L27N_1/VREF_1	J13	NC	NC		
1	IO_L27P_1	K13	NC	NC		
1	IO_L26N_1	D8	NC	NC		
1	IO_L26P_1	E8	NC	NC		
1	IO_L25N_1	F12	NC	NC		
1	IO_L25P_1	G12	NC	NC		
1	IO_L21N_1	G11	NC	NC		
1	IO_L21P_1	H11	NC	NC		
1	IO_L20N_1	C7	NC	NC		
1	IO_L20P_1	D7	NC	NC		
1	IO_L19N_1	E11	NC	NC		
1	IO_L19P_1	F11	NC	NC		
1	IO_L09N_1/VREF_1	J12				
1	IO_L09P_1	K12				
1	IO_L08N_1	D6				
1	IO_L08P_1	D5				
1	IO_L07N_1	E9				
1	IO_L07P_1	F9				
1	IO_L06N_1	J11				
1	IO_L06P_1	K11				
1	IO_L05_1/No_Pair	J10				
1	IO_L03N_1/VREF_1	G10				
1	IO_L03P_1	H10				
1	IO_L02N_1	G9				
1	IO_L02P_1	H9				
1	IO_L01N_1/VRP_1	E7				
1	IO_L01P_1/VRN_1	E6				
2	IO_L01N_2/VRP_2	D2				
2	IO_L01P_2/VRN_2	D1				
2	IO_L02N_2	F8				
2	IO_L02P_2	F7				
2	IO_L03N_2	E4				
2	IO_L03P_2	E3				
2	IO_L04N_2/VREF_2	E2				
2	IO_L04P_2	E1				

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L53P_6	AB30		
6	IO_L53N_6	AB31		
6	IO_L54P_6	AC38		
6	IO_L54N_6	AC39		
6	IO_L55P_6	AC34		
6	IO_L55N_6	AC35		
6	IO_L56P_6	AA28		
6	IO_L56N_6	AA29		
6	IO_L57P_6	AB38		
6	IO_L57N_6/VREF_6	AB39		
6	IO_L58P_6	AB36		
6	IO_L58N_6	AB37		
6	IO_L59P_6	AA30		
6	IO_L59N_6	AA31		
6	IO_L60P_6	AB34		
6	IO_L60N_6	AB35		
6	IO_L85P_6	AB32		
6	IO_L85N_6	AB33		
6	IO_L86P_6	AA27		
6	IO_L86N_6	Y27		
6	IO_L87P_6	AA36		
6	IO_L87N_6/VREF_6	AA37		
6	IO_L88P_6	AA34		
6	IO_L88N_6	AA35		
6	IO_L89P_6	Y28		
6	IO_L89N_6	Y29		
6	IO_L90P_6	AA32		
6	IO_L90N_6	AA33		
7	IO_L90P_7	Y36		
7	IO_L90N_7	Y37		
7	IO_L89P_7	Y31		
7	IO_L89N_7	W31		
7	IO_L88P_7	Y32		
7	IO_L88N_7/VREF_7	Y33		
7	IO_L87P_7	W36		
7	IO_L87N_7	W37		
7	IO_L86P_7	W27		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L82N_7/VREF_7	G37	NC	
7	IO_L81P_7	G33	NC	
7	IO_L81N_7	G34	NC	
7	IO_L79P_7	F38	NC	
7	IO_L79N_7	F39	NC	
7	IO_L78P_7	F36	NC	
7	IO_L78N_7	F37	NC	
7	IO_L76P_7	G35	NC	
7	IO_L76N_7/VREF_7	F35	NC	
7	IO_L75P_7	E37	NC	
7	IO_L75N_7	E38	NC	
7	IO_L73P_7	D38	NC	
7	IO_L73N_7	D39	NC	
7	IO_L06P_7	F33		
7	IO_L06N_7	E33		
7	IO_L05P_7	J31		
7	IO_L05N_7	H32		
7	IO_L04P_7	E34		
7	IO_L04N_7/VREF_7	D34		
7	IO_L03P_7	D35		
7	IO_L03N_7	C35		
7	IO_L02P_7	H31		
7	IO_L02N_7	G31		
7	IO_L01P_7/VRN_7	D33		
7	IO_L01N_7/VRP_7	C33		
7	VCCO_7	E39		
7	VCCO_7	U37		
7	VCCO_7	N36		
7	VCCO_7	J36		
7	VCCO_7	E36		
7	VCCO_7	Y35		
7	VCCO_7	U33		
7	VCCO_7	N32		
7	VCCO_7	J32		
7	VCCO_7	F32		
7	VCCO_7	U29		
7	VCCO_7	N28		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		V6		
N/A	GND		U25		
N/A	GND		U24		
N/A	GND		U23		
N/A	GND		U22		
N/A	GND		U21		
N/A	GND		U20		
N/A	GND		U19		
N/A	GND		U18		
N/A	GND		T42		
N/A	GND		T1		
N/A	GND		R39		
N/A	GND		R36		
N/A	GND		R7		
N/A	GND		R4		
N/A	GND		M42		
N/A	GND		M1		
N/A	GND		L22		
N/A	GND		L21		
N/A	GND		K39		
N/A	GND		K4		
N/A	GND		J34		
N/A	GND		J9		
N/A	GND		H42		
N/A	GND		H35		
N/A	GND		H22		
N/A	GND		H21		
N/A	GND		H8		
N/A	GND		H1		
N/A	GND		G36		
N/A	GND		G7		
N/A	GND		F37		
N/A	GND		F25		
N/A	GND		F18		
N/A	GND		F6		
N/A	GND		E38		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
4	IO_L58P_4	AW19	
4	IO_L59N_4	AP19	
4	IO_L59P_4	AN19	
4	IO_L60N_4	BB19	
4	IO_L60P_4	BA19	
4	IO_L64N_4	AU20	
4	IO_L64P_4	AT20	
4	IO_L65N_4	AL21	
4	IO_L65P_4	AL20	
4	IO_L66N_4	BA20	
4	IO_L66P_4/VREF_4	AY20	
4	IO_L67N_4	AR21	
4	IO_L67P_4	AP21	
4	IO_L68N_4	AN20	
4	IO_L68P_4	AM20	
4	IO_L69N_4	AU21	
4	IO_L69P_4/VREF_4	AT21	
4	IO_L73N_4	AW21	
4	IO_L73P_4	AV21	
4	IO_L74N_4/GCLK3S	AN21	
4	IO_L74P_4/GCLK2P	AM21	
4	IO_L75N_4/GCLK1S	BA21	
4	IO_L75P_4/GCLK0P	AY21	
5	IO_L75N_5/GCLK7S	AY22	
5	IO_L75P_5/GCLK6P	BA22	
5	IO_L74N_5/GCLK5S	AM22	
5	IO_L74P_5/GCLK4P	AN22	
5	IO_L73N_5	AV22	
5	IO_L73P_5	AW22	
5	IO_L69N_5/VREF_5	AT22	
5	IO_L69P_5	AU22	
5	IO_L68N_5	AM23	
5	IO_L68P_5	AN23	
5	IO_L67N_5	AP22	
5	IO_L67P_5	AR22	
5	IO_L66N_5/VREF_5	AY23	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L26P_7	V31	
7	IO_L26N_7	U31	
7	IO_L25P_7	L41	
7	IO_L25N_7	L42	
7	IO_L24P_7	K40	
7	IO_L24N_7	L40	
7	IO_L23P_7	T34	
7	IO_L23N_7	T35	
7	IO_L22P_7	L38	
7	IO_L22N_7/VREF_7	L39	
7	IO_L21P_7	K36	
7	IO_L21N_7	L36	
7	IO_L20P_7	T32	
7	IO_L20N_7	T33	
7	IO_L19P_7	K41	
7	IO_L19N_7	K42	
7	IO_L18P_7	K37	
7	IO_L18N_7	K38	
7	IO_L17P_7	R34	
7	IO_L17N_7	R35	
7	IO_L16P_7	H42	
7	IO_L16N_7/VREF_7	J41	
7	IO_L15P_7	J39	
7	IO_L15N_7	J40	
7	IO_L14P_7	R32	
7	IO_L14N_7	R33	
7	IO_L13P_7	J36	
7	IO_L13N_7	J37	
7	IO_L12P_7	H40	
7	IO_L12N_7	H41	
7	IO_L11P_7	T31	
7	IO_L11N_7	R31	
7	IO_L10P_7	H38	
7	IO_L10N_7/VREF_7	H39	
7	IO_L09P_7	H36	
7	IO_L09N_7	H37	
7	IO_L08P_7	P34	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCINT	W16	
N/A	VCCINT	V16	
N/A	VCCINT	U16	
N/A	VCCINT	T16	
N/A	VCCINT	R16	
N/A	VCCINT	P16	
N/A	VCCINT	AJ15	
N/A	VCCINT	AH15	
N/A	VCCINT	R15	
N/A	VCCINT	P15	
N/A	VCCINT	AJ14	
N/A	VCCINT	P14	
N/A	VCCINT	AK13	
N/A	VCCINT	N13	
N/A	VCCAUX	BA42	
N/A	VCCAUX	AY42	
N/A	VCCAUX	AL42	
N/A	VCCAUX	AB42	
N/A	VCCAUX	AA42	
N/A	VCCAUX	M42	
N/A	VCCAUX	C42	
N/A	VCCAUX	B42	
N/A	VCCAUX	BB41	
N/A	VCCAUX	A41	
N/A	VCCAUX	BB40	
N/A	VCCAUX	A40	
N/A	VCCAUX	BB31	
N/A	VCCAUX	A31	
N/A	VCCAUX	BB22	
N/A	VCCAUX	A22	
N/A	VCCAUX	BB21	
N/A	VCCAUX	A21	
N/A	VCCAUX	BB12	
N/A	VCCAUX	A12	
N/A	VCCAUX	BB3	
N/A	VCCAUX	A3	
N/A	VCCAUX	BB2	