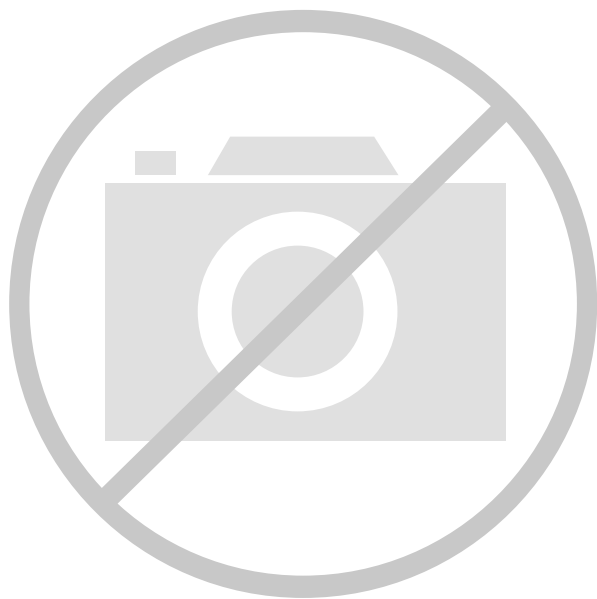




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	11024
Number of Logic Elements/Cells	99216
Total RAM Bits	8183808
Number of I/O	1040
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1704-BBGA, FCBGA
Supplier Device Package	1704-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp100-6ffg1704i

Serializer

The serializer multiplies the reference frequency provided on REFCLK by 20. The multiplication of the clock is achieved by using an embedded PLL.

Data is converted from parallel to serial format and transmitted on the TXP and TXN differential outputs. The electrical connection of TXP and TXN can be interchanged through configuration. This option can be controlled by an input (TXPOLARITY) at the FPGA transmitter interface.

Deserializer

The serial transceiver input is locked to the input data stream through Clock and Data Recovery (CDR), a built-in feature of the RocketIO transceiver. CDR keys off the rising and falling edges of incoming data and derives a clock that is representative of the incoming data rate.

The derived clock, RXRECCLK, is generated and locked to as long as it remains within the specified component range. This clock is presented to the FPGA fabric at $1/20$ the incoming data rate.

A sufficient number of transitions must be present in the data stream for CDR to work properly. CDR requires approximately 5,000 transitions upon power-up to guaran-

tee locking to the incoming data rate. Once lock is achieved, up to 75 missing transitions can be tolerated before lock to the incoming data stream is lost. The CDR circuit is guaranteed to work with 8B/10B encoding.

Another feature of CDR is its ability to accept an external precision reference clock, REFCLK, which either acts to clock incoming data or to assist in synchronizing the derived RXRECCLK.

For further clarity, the TXUSRCLK is used to clock data from the FPGA fabric to the TX FIFO. The FIFO depth accounts for the slight phase difference between these two clocks. If the clocks are locked in frequency, then the FIFO acts much like a pass-through buffer.

The receiver can be configured to reverse the RXP and RXN inputs. This can be useful in the event that printed circuit board traces have been reversed.

Receiver Termination

On-chip termination is provided at the receiver, eliminating the need for external termination. The receiver includes programmable on-chip termination circuitry for 50Ω (default) or 75Ω impedance, as shown in [Figure 11](#).

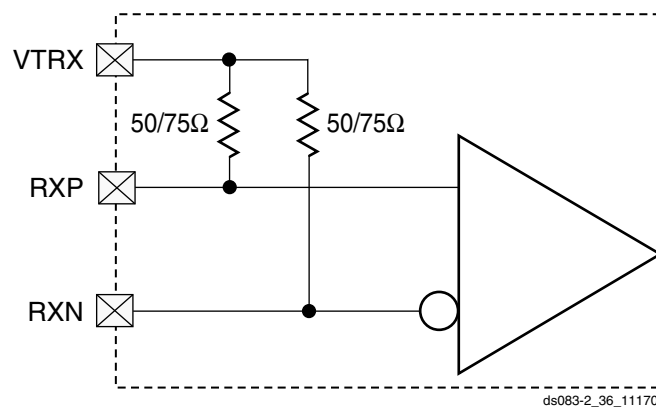


Figure 11: RocketIO Receive Termination

PCS

Fabric Data Interface

Internally, the PCS operates in 2-byte mode (16/20 bits). The FPGA fabric interface can either be 1, 2, or 4 bytes wide. When accompanied by the predefined modes of the PMA, the user thus has a large combination of protocols and data rates from which to choose.

USRCLK2 clocks data on the fabric side, while USRCLK clocks data on the PCS side. This creates distinct USRCLK/USRCLK2 frequency ratios for different combina-

tions of fabric and internal data widths. [Table 5](#) summarizes the USRCLK2 to USRCLK ratios for the three fabric data widths.

No fixed phase relationship is assumed between REFCLK, RXRECCLK, and/or any other clock that is not tied to either of these clocks. When RXUSRCLK and RXUSRCLK2 have different frequencies, each edge of the slower clock is aligned to a falling edge of the faster clock. The same relationships apply to TXUSRCLK and TXUSRCLK2.

Each block SelectRAM+ cell is a fully synchronous memory, as illustrated in Figure 48. The two ports have independent inputs and outputs and are independently clocked.

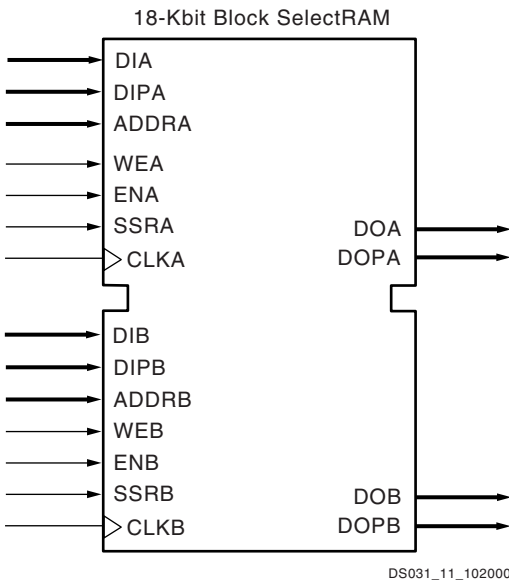


Figure 48: 18 Kb Block SelectRAM+ in Dual-Port Mode

Port Aspect Ratios

Table 23 shows the depth and the width aspect ratios for the 18 Kb block SelectRAM+ resource. Virtex-II Pro block SelectRAM+ also includes dedicated routing resources to provide an efficient interface with CLBs, block SelectRAM+, and multipliers.

Table 23: 18 Kb Block SelectRAM+ Port Aspect Ratio

Width	Depth	Address Bus	Data Bus	Parity Bus
1	16,384	ADDR[13:0]	DATA[0]	N/A
2	8,192	ADDR[12:0]	DATA[1:0]	N/A
4	4,096	ADDR[11:0]	DATA[3:0]	N/A
9	2,048	ADDR[10:0]	DATA[7:0]	Parity[0]
18	1,024	ADDR[9:0]	DATA[15:0]	Parity[1:0]
36	512	ADDR[8:0]	DATA[31:0]	Parity[3:0]

Read/Write Operations

The Virtex-II Pro block SelectRAM+ read operation is fully synchronous. An address is presented, and the read operation is enabled by control signal ENA or ENB. Then, depending on clock polarity, a rising or falling clock edge causes the stored data to be loaded into output registers.

The write operation is also fully synchronous. Data and address are presented, and the write operation is enabled by control signals WEA and WEB in addition to ENA or ENB. Then, again depending on the clock input mode, a rising or falling clock edge causes the data to be loaded into the memory cell addressed.

A write operation performs a simultaneous read operation. Three different options are available, selected by configuration:

1. WRITE_FIRST

The WRITE_FIRST option is a transparent mode. The same clock edge that writes the data input (DI) into the memory also transfers DI into the output registers DO, as shown in Figure 49.

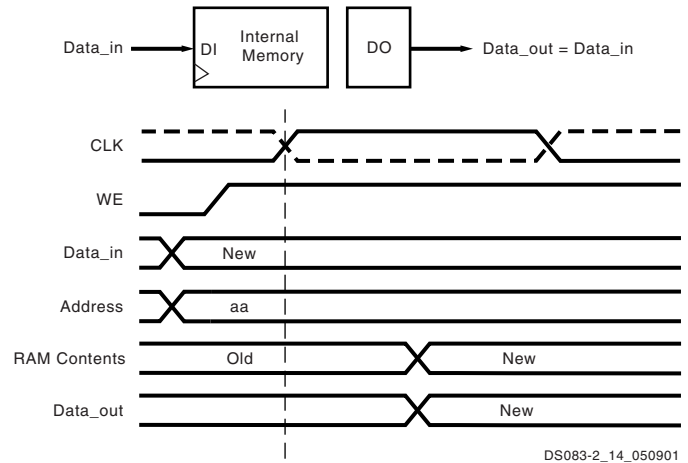


Figure 49: WRITE_FIRST Mode

2. READ_FIRST

The READ_FIRST option is a read-before-write mode.

The same clock edge that writes data input (DI) into the memory also transfers the prior content of the memory cell addressed into the data output registers DO, as shown in Figure 50.

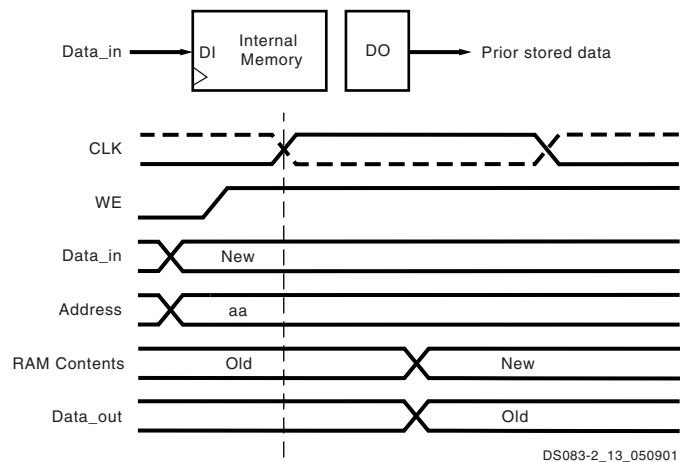


Figure 50: READ_FIRST Mode



Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics

DS083 (v5.0) June 21, 2011

Product Specification

Virtex-II Pro⁽¹⁾ Electrical Characteristics

Virtex™-II Pro devices are provided in -7, -6, and -5 speed grades, with -7 having the highest performance.

Virtex-II Pro DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -6 speed grade industrial device are the same as for a -6 speed grade

commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex-II Pro DC Characteristics

Table 1: Absolute Maximum Ratings

Symbol	Description ⁽¹⁾		Virtex-II Pro X	Virtex-II Pro	Units
V _{CCINT}	Internal supply voltage relative to GND		−0.5 to 1.6		V
V _{CCAUX}	Auxiliary supply voltage relative to GND		−0.5 to 3.0		V
V _{CCO}	Output drivers supply voltage relative to GND		−0.5 to 3.75		V
V _{BATT}	Key memory battery backup supply		−0.5 to 4.05		V
V _{REF}	Input reference voltage		−0.3 to 3.75		V
V _{IN}	3.3V I/O input voltage relative to GND (user and dedicated I/Os)		−0.3 to 4.05 ⁽³⁾		V
	2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)		−0.5 to V _{CCO} + 0.5		V
V _{TS}	Voltage applied to 3-state 3.3V output (user and dedicated I/Os)		−0.3 to 4.05 ⁽³⁾		V
	Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os)		−0.5 to V _{CCO} + 0.5		V
AVCCAUXRX	Receive auxilliary supply voltage relative to GNDA (analog ground)		−0.5 to 2.0	−0.5 to 3.0	V
AVCCAUTX	Transmit auxilliary supply voltage relative to GNDA (analog ground)		−0.5 to 3.0	−0.5 to 3.0	V
V _{TRX}	Terminal receive supply voltage relative to GND		−0.5 to 3.0	−0.5 to 3.0	V
V _{TTX}	Terminal transmit supply voltage relative to GND		−0.5 to 1.6	−0.5 to 3.0	V
T _{STG}	Storage temperature (ambient)		−65 to +150		°C
T _{SOL}	Maximum soldering temperature ⁽²⁾	All regular FG/FF flip-chip packages	+220		°C
		Pb-free FGG256 wire-bond package	N/A	+260	°C
		Pb-free FGG456 and FGG676 wire-bond packages	N/A	+250	°C
T _J	Maximum junction temperature ⁽²⁾		+125		°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- For soldering guidelines and thermal considerations, see the [Device Packaging and Thermal Characteristics Guide](#) information on the Xilinx website.
- 3.3V I/O Absolute Maximum limit applied to DC and AC signals. Refer to [XAPP659](#) for more details.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

Table 35: IOB Input Switching Characteristics (Continued)

			Speed Grade			
Description	Symbol	Device	-7	-6	-5	Units
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOICK}/T_{IOICKP}	All	0.84/–0.61	0.86/–0.63	0.90/–0.67	ns, min
Pad, with delay	$T_{IOICKD}/T_{IOICKPD}$	XC2VP2	2.28/–1.89	2.60/–2.15	2.95/–2.43	ns, max
		XC2VP4	2.55/–2.10	2.87/–2.36	3.21/–2.65	ns, max
		XC2VP7	2.48/–2.05	2.82/–2.32	3.15/–2.60	ns, max
		XC2VP20	2.63/–2.05	3.02/–2.35	3.40/–2.66	ns, max
		XC2VPX20	2.63/–2.05	3.02/–2.35	3.40/–2.66	ns, max
		XC2VP30	2.67/–2.07	3.09/–2.42	3.49/–2.73	ns, max
		XC2VP40	3.28/–2.56	3.61/–2.83	4.01/–3.15	ns, max
		XC2VP50	3.84/–3.02	4.08/–3.21	4.42/–3.48	ns, max
		XC2VP70	3.98/–3.13	4.23/–3.33	4.55/–3.58	ns, max
		XC2VPX70	3.98/–3.13	4.23/–3.33	4.55/–3.58	ns, max
	XC2VP100	N/A	6.48/–5.13	7.04/–5.57	ns, max	
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All	0.39/ 0.01	0.44/ 0.01	0.49/ 0.01	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.52	0.57	0.75	ns, min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	1.13	1.27	1.42	ns, max
GSR to output IQ	T_{GSRQ}	All	5.87	6.75	7.43	ns, max

Notes:

1. Input timing for LVCMOS25 is measured at 1.25V. For other I/O standards, see [Table 39](#).

Table 40: Output Delay Measurement Methodology

Description	IOSTANDARD Attribute	R _{REF} (Ω)	C _{REF} ⁽¹⁾ (pF)	V _{MEAS} (V)	V _{REF} (V)
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V _{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V _{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V _{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V _{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	50	0	V _{REF}	1.2
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	50	0	V _{REF}	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	1M	0	1.2	0
LDT (HyperTransport), 2.5V	LDT_25	50	0	V _{REF}	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	1M	0	1.23	0
LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	1M	0	1.65	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V _{REF}	0.75
HSTL, Class III & IV, with DCI	HSTL_III_DCI, HSTL_IV_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V _{REF}	0.9
HSTL, Class III & IV, 1.8V, with DCI	HSTL_III_DCI_18, HSTL_IV_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termini.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V _{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V _{REF}	1.25
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	50	0	0.8	1.2
GTL Plus with DCI	GTLP_DCI	50	0	1.0	1.5

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Measured as per PCI specification.
3. Measured as per PCI-X specification.

Multiplier Switching Characteristics

Table 45: Multiplier Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Propagation Delay to Output Pin					
Input to Pin35	T _{MULT_P35}	4.08	4.64	5.19	ns, max
Input to Pin34	T _{MULT_P34}	3.99	4.55	5.09	ns, max
Input to Pin33	T _{MULT_P33}	3.90	4.45	4.99	ns, max
Input to Pin32	T _{MULT_P32}	3.80	4.36	4.88	ns, max
Input to Pin31	T _{MULT_P31}	3.71	4.27	4.78	ns, max
Input to Pin30	T _{MULT_P30}	3.62	4.17	4.67	ns, max
Input to Pin29	T _{MULT_P29}	3.53	4.08	4.57	ns, max
Input to Pin28	T _{MULT_P28}	3.43	3.99	4.46	ns, max
Input to Pin27	T _{MULT_P27}	3.34	3.89	4.36	ns, max
Input to Pin26	T _{MULT_P26}	3.25	3.80	4.26	ns, max
Input to Pin25	T _{MULT_P25}	3.16	3.71	4.15	ns, max
Input to Pin24	T _{MULT_P24}	3.06	3.61	4.05	ns, max
Input to Pin23	T _{MULT_P23}	2.97	3.52	3.94	ns, max
Input to Pin22	T _{MULT_P22}	2.88	3.43	3.84	ns, max
Input to Pin21	T _{MULT_P21}	2.79	3.34	3.73	ns, max
Input to Pin20	T _{MULT_P20}	2.70	3.24	3.63	ns, max
Input to Pin19	T _{MULT_P19}	2.60	3.15	3.53	ns, max
Input to Pin18	T _{MULT_P18}	2.51	3.06	3.42	ns, max
Input to Pin17	T _{MULT_P17}	2.42	2.96	3.32	ns, max
Input to Pin16	T _{MULT_P16}	2.34	2.86	3.21	ns, max
Input to Pin15	T _{MULT_P15}	2.27	2.76	3.09	ns, max
Input to Pin14	T _{MULT_P14}	2.19	2.67	2.98	ns, max
Input to Pin13	T _{MULT_P13}	2.12	2.57	2.87	ns, max
Input to Pin12	T _{MULT_P12}	2.04	2.47	2.76	ns, max
Input to Pin11	T _{MULT_P11}	1.96	2.37	2.65	ns, max
Input to Pin10	T _{MULT_P10}	1.89	2.27	2.54	ns, max
Input to Pin9	T _{MULT_P9}	1.81	2.17	2.43	ns, max
Input to Pin8	T _{MULT_P8}	1.74	2.07	2.32	ns, max
Input to Pin7	T _{MULT_P7}	1.66	1.97	2.21	ns, max
Input to Pin6	T _{MULT_P6}	1.59	1.87	2.09	ns, max
Input to Pin5	T _{MULT_P5}	1.51	1.77	1.98	ns, max
Input to Pin4	T _{MULT_P4}	1.44	1.67	1.87	ns, max
Input to Pin3	T _{MULT_P3}	1.36	1.57	1.76	ns, max
Input to Pin2	T _{MULT_P2}	1.28	1.47	1.65	ns, max
Input to Pin1	T _{MULT_P1}	1.21	1.37	1.54	ns, max
Input to Pin0	T _{MULT_P0}	1.13	1.27	1.43	ns, max

Virtex-II Pro Pin Definitions

This section describes the pinouts for Virtex-II Pro devices in the following packages:

- FG256/FGG256, FG456/FGG456, and FG676/FGG676: wire-bond fine-pitch BGA of 1.00 mm pitch
- FF672, FF896, FF1148, FF1152, FF1517, FF1696, and FF1704: flip-chip fine-pitch BGA of 1.00 mm pitch

All of the devices supported in a particular package are pin-out-compatible and are listed in the same table (one table

per package). Pins that are not available for smaller devices are listed in right-hand columns.

Each device is split into eight I/O banks to allow for flexibility in the choice of I/O standards. Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. **Table 4** provides definitions for all pin types.

All Virtex-II Pro pinout tables are available on the distribution CD-ROM, or on the web (at <http://www.xilinx.com>).

Pin Definitions

Table 4 provides a description of each pin type listed in Virtex-II Pro pinout tables.

Table 4: Virtex-II Pro Pin Definitions

Pin Name	Direction	Description
User I/O Pins:		
IO_LXXY_#	Input/Output/ Bidirectional	All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, LVPECL, or LDT pairs. Each user I/O is labeled "IO_LXXY_#", where: IO indicates a user I/O pin. LXXY indicates a differential pair, with XX a unique pair in the bank and Y = P/N for the positive and negative sides of the differential pair. # indicates the bank number (0 through 7)
Dual-Function Pins:		
IO_LXXY_#/ZZZ		The <i>dual-function pins</i> are labelled "IO_LXXY_#/ZZZ", where "ZZZ" can be one of the following pins: Per Bank - VRP , VRN , or VREF Globally - GCLKX(S/P) , BUSY/DOUT , INIT_B , D0/DIN – D7 , RDWR_B , or CS_B These dual functions are defined in the following section:
"ZZZ" (Dual Function) Definitions:		
D0/DIN, D1, D2, D3, D4, D5, D6, D7	Input/Output	• In <i>SelectMAP</i> mode, D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. • In <i>bit-serial modes</i>, DIN (D0) is the single-data input. This pin becomes a user I/O after configuration.
CS_B	Input	In SelectMAP mode, this is the active-low Chip Select signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
RDWR_B	Input	In SelectMAP mode, this is the active-low Write Enable signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
BUSY/DOUT	Output	• In <i>SelectMAP</i> mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained. • In <i>bit-serial modes</i>, DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. The pin becomes a user I/O after configuration.

FG256/FGG256 Fine-Pitch BGA Package

As shown in [Table 5](#), XC2VP2 and XC2VP4 Virtex-II Pro devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in each of these devices are identical. Following this table are the [FG256/FGG256 Fine-Pitch BGA Package Specifications \(1.00mm pitch\)](#).

Table 5: FG256/FGG256 — XC2VP2 and XC2VP4

Bank	Pin Description	Pin Number
0	IO_L01N_0/VRP_0	C2
0	IO_L01P_0/VRN_0	C3
0	IO_L02N_0	B3
0	IO_L02P_0	C4
0	IO_L03N_0	A2
0	IO_L03P_0/VREF_0	A3
0	IO_L06N_0	D5
0	IO_L06P_0	C5
0	IO_L07P_0	D6
0	IO_L09N_0	E6
0	IO_L09P_0/VREF_0	E7
0	IO_L69N_0	D7
0	IO_L69P_0/VREF_0	C7
0	IO_L74N_0/GCLK7P	D8
0	IO_L74P_0/GCLK6S	C8
0	IO_L75N_0/GCLK5P	B8
0	IO_L75P_0/GCLK4S	A8
1	IO_L75N_1/GCLK3P	A9
1	IO_L75P_1/GCLK2S	B9
1	IO_L74N_1/GCLK1P	C9
1	IO_L74P_1/GCLK0S	D9
1	IO_L69N_1/VREF_1	C10
1	IO_L69P_1	D10
1	IO_L09N_1/VREF_1	E10
1	IO_L09P_1	E11
1	IO_L07N_1	D11
1	IO_L06N_1	C12
1	IO_L06P_1	D12
1	IO_L03N_1/VREF_1	A14
1	IO_L03P_1	A15

FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)

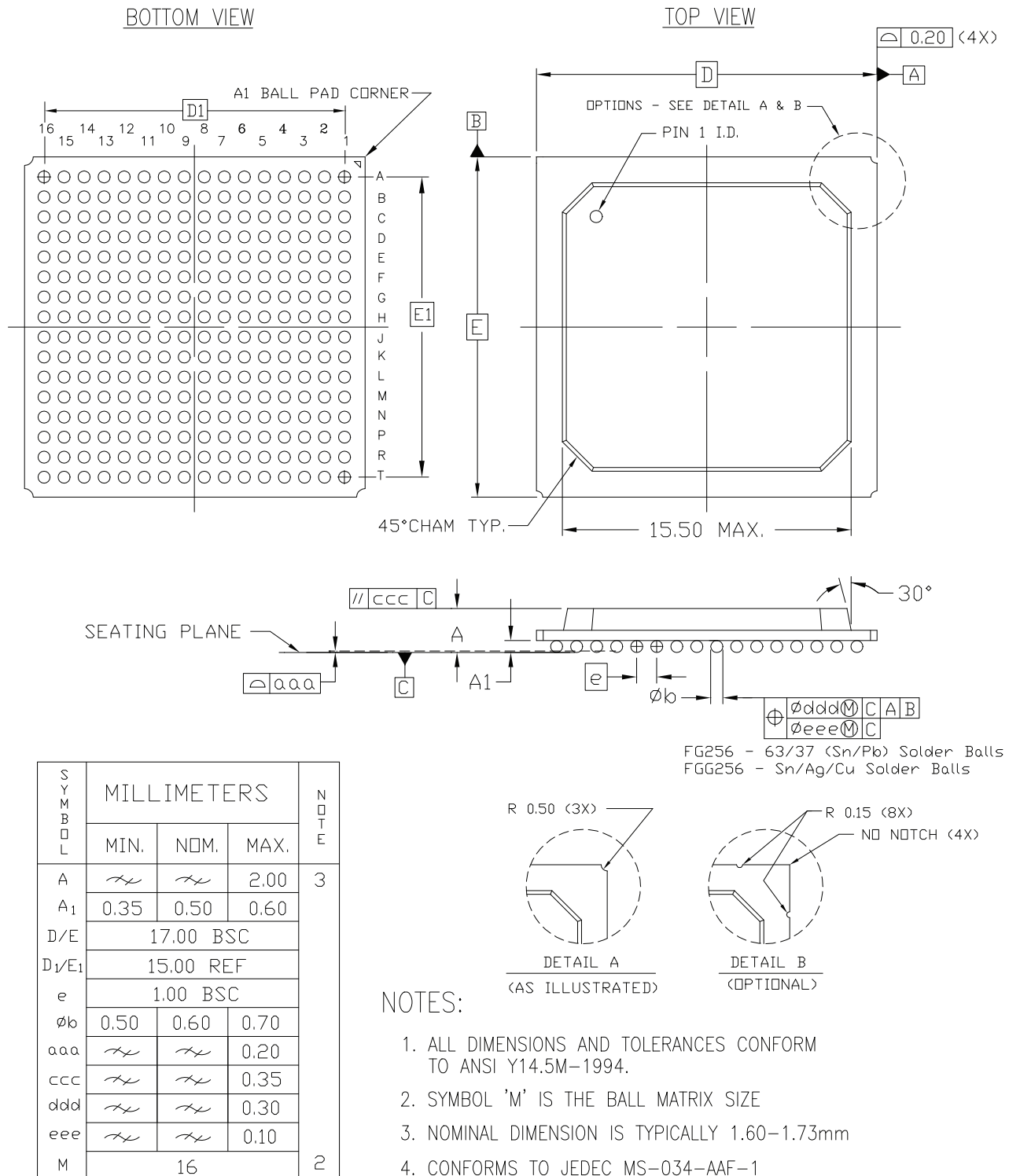


Figure 1: FG256/FGG256 Fine-Pitch BGA Package Specifications

Table 6: FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L06N_6	V1			
6	IO_L43P_6	U4	NC		
6	IO_L43N_6	U3	NC		
6	IO_L45P_6	U2	NC		
6	IO_L45N_6/VREF_6	U1	NC		
6	IO_L47P_6	U5	NC		
6	IO_L47N_6	T5	NC		
6	IO_L48P_6	T4	NC		
6	IO_L48N_6	T3	NC		
6	IO_L49P_6	T2	NC		
6	IO_L49N_6	T1	NC		
6	IO_L51P_6	R4	NC		
6	IO_L51N_6/VREF_6	R3	NC		
6	IO_L53P_6	R2	NC		
6	IO_L53N_6	R1	NC		
6	IO_L54P_6	R5	NC		
6	IO_L54N_6	P6	NC		
6	IO_L55P_6	P4	NC		
6	IO_L55N_6	P3	NC		
6	IO_L57P_6	P2	NC		
6	IO_L57N_6/VREF_6	P1	NC		
6	IO_L59P_6	P5	NC		
6	IO_L59N_6	N5	NC		
6	IO_L60P_6	N4	NC		
6	IO_L60N_6	N3	NC		
6	IO_L85P_6	N2			
6	IO_L85N_6	N1			
6	IO_L87P_6	N6			
6	IO_L87N_6/VREF_6	M6			
6	IO_L89P_6	M5			
6	IO_L89N_6	M4			
6	IO_L90P_6	M3			
6	IO_L90N_6	M2			
7	IO_L90P_7	L2			
7	IO_L90N_7	L3			
7	IO_L88P_7	L4			

Table 8: FF672 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	GND	K15			
N/A	GND	K17			
N/A	GND	L11			
N/A	GND	L12			
N/A	GND	L13			
N/A	GND	L14			
N/A	GND	L15			
N/A	GND	L16			
N/A	GND	M10			
N/A	GND	M11			
N/A	GND	M12			
N/A	GND	M13			
N/A	GND	M14			
N/A	GND	M15			
N/A	GND	M16			
N/A	GND	M17			
N/A	GND	N10			
N/A	GND	N11			
N/A	GND	N12			
N/A	GND	N13			
N/A	GND	N14			
N/A	GND	N15			
N/A	GND	N16			
N/A	GND	N17			
N/A	GND	P10			
N/A	GND	P11			
N/A	GND	P12			
N/A	GND	P13			
N/A	GND	P14			
N/A	GND	P15			
N/A	GND	P16			
N/A	GND	P17			
N/A	GND	R10			
N/A	GND	R11			
N/A	GND	R12			
N/A	GND	R13			
N/A	GND	R14			

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	GND		N17			
N/A	GND		N16			
N/A	GND		N15			
N/A	GND		N14			
N/A	GND		N13			
N/A	GND		N12			
N/A	GND		M19			
N/A	GND		M18			
N/A	GND		M17			
N/A	GND		M16			
N/A	GND		M15			
N/A	GND		M14			
N/A	GND		M13			
N/A	GND		M12			
N/A	GND		L28			
N/A	GND		L25			
N/A	GND		L20			
N/A	GND		L11			
N/A	GND		L6			
N/A	GND		L3			
N/A	GND		H30			
N/A	GND		H1			
N/A	GND		F25			
N/A	GND		F18			
N/A	GND		F13			
N/A	GND		F6			
N/A	GND		E26			
N/A	GND		E5			
N/A	GND		D27			
N/A	GND		D22			
N/A	GND		D19			
N/A	GND		D12			
N/A	GND		D9			
N/A	GND		D4			
N/A	GND		C28			
N/A	GND		C17			

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L05N_2	J8				
2	IO_L05P_2	J7				
2	IO_L06N_2	F5				
2	IO_L06P_2	F4				
2	IO_L15N_2	G4	NC			
2	IO_L15P_2	G3	NC			
2	IO_L16N_2/VREF_2	G6	NC			
2	IO_L16P_2	G5	NC			
2	IO_L17N_2	F2	NC			
2	IO_L17P_2	F1	NC			
2	IO_L18N_2	L10	NC			
2	IO_L18P_2	L9	NC			
2	IO_L19N_2	H6	NC			
2	IO_L19P_2	H5	NC			
2	IO_L20N_2	G2	NC			
2	IO_L20P_2	G1	NC			
2	IO_L21N_2	J6	NC			
2	IO_L21P_2	J5	NC			
2	IO_L22N_2/VREF_2	J4	NC			
2	IO_L22P_2	J3	NC			
2	IO_L23N_2	K8	NC			
2	IO_L23P_2	K7	NC			
2	IO_L24N_2	H4	NC			
2	IO_L24P_2	H3	NC			
2	IO_L31N_2	H2				
2	IO_L31P_2	H1				
2	IO_L32N_2	M10				
2	IO_L32P_2	M9				
2	IO_L33N_2	K5				
2	IO_L33P_2	K4				
2	IO_L34N_2/VREF_2	J2				
2	IO_L34P_2	K2				
2	IO_L35N_2	L8				
2	IO_L35P_2	L7				
2	IO_L36N_2	L6				
2	IO_L36P_2	L5				
2	IO_L37N_2	K1				
2	IO_L37P_2	L1				

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L43N_0	B22		
0	IO_L43P_0	C22		
0	IO_L44N_0	K21		
0	IO_L44P_0	L21		
0	IO_L45N_0	G21		
0	IO_L45P_0/VREF_0	H21		
0	IO_L46N_0	E21		
0	IO_L46P_0	F21		
0	IO_L47N_0	K20		
0	IO_L47P_0	L20		
0	IO_L48N_0	C21		
0	IO_L48P_0	D21		
0	IO_L49N_0	A21		
0	IO_L49P_0	B21		
0	IO_L50_0/No_Pair	G20		
0	IO_L53_0/No_Pair	H19		
0	IO_L54N_0	E20		
0	IO_L54P_0	F20		
0	IO_L55N_0	C20		
0	IO_L55P_0	D19		
0	IO_L56N_0	K19		
0	IO_L56P_0	L19		
0	IO_L57N_0	A20		
0	IO_L57P_0/VREF_0	B20		
0	IO_L66N_0	F19	NC	
0	IO_L66P_0/VREF_0	G19	NC	
0	IO_L67N_0	B19		
0	IO_L67P_0	C19		
0	IO_L68N_0	H18		
0	IO_L68P_0	J18		
0	IO_L69N_0	F18		
0	IO_L69P_0/VREF_0	G18		
0	IO_L73N_0	D18		
0	IO_L73P_0	E18		
0	IO_L74N_0/GCLK7P	K18		
0	IO_L74P_0/GCLK6S	L18		
0	IO_L75N_0/GCLK5P	B18		
0	IO_L75P_0/GCLK4S	C18		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L30N_2	N6		
2	IO_L30P_2	N7		
2	IO_L31N_2	M4		
2	IO_L31P_2	N5		
2	IO_L32N_2	R11		
2	IO_L32P_2	R12		
2	IO_L33N_2	N1		
2	IO_L33P_2	N2		
2	IO_L34N_2/VREF_2	P6		
2	IO_L34P_2	P7		
2	IO_L35N_2	R13		
2	IO_L35P_2	T13		
2	IO_L36N_2	P4		
2	IO_L36P_2	P5		
2	IO_L37N_2	P3		
2	IO_L37P_2	N3		
2	IO_L38N_2	T10		
2	IO_L38P_2	T11		
2	IO_L39N_2	P1		
2	IO_L39P_2	P2		
2	IO_L40N_2/VREF_2	R7		
2	IO_L40P_2	R8		
2	IO_L41N_2	T12		
2	IO_L41P_2	U12		
2	IO_L42N_2	R5		
2	IO_L42P_2	R6		
2	IO_L43N_2	R3		
2	IO_L43P_2	R4		
2	IO_L44N_2	U8		
2	IO_L44P_2	T8		
2	IO_L45N_2	R1		
2	IO_L45P_2	R2		
2	IO_L46N_2/VREF_2	T6		
2	IO_L46P_2	T7		
2	IO_L47N_2	U9		
2	IO_L47P_2	U10		
2	IO_L48N_2	T2		
2	IO_L48P_2	T3		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L04P_6	AR33		
6	IO_L04N_6	AP33		
6	IO_L05P_6	AM32		
6	IO_L05N_6	AL31		
6	IO_L06P_6	AT34		
6	IO_L06N_6	AR34		
6	IO_L73P_6	AU35	NC	
6	IO_L73N_6	AT35	NC	
6	IO_L75P_6	AT38	NC	
6	IO_L75N_6/VREF_6	AT39	NC	
6	IO_L76P_6	AR37	NC	
6	IO_L76N_6	AR38	NC	
6	IO_L78P_6	AP38	NC	
6	IO_L78N_6	AP39	NC	
6	IO_L79P_6	AP36	NC	
6	IO_L79N_6	AP37	NC	
6	IO_L81P_6	AP35	NC	
6	IO_L81N_6/VREF_6	AN35	NC	
6	IO_L82P_6	AN38	NC	
6	IO_L82N_6	AN39	NC	
6	IO_L84P_6	AN36	NC	
6	IO_L84N_6	AN37	NC	
6	IO_L07P_6	AN33		
6	IO_L07N_6	AN34		
6	IO_L08P_6	AK31		
6	IO_L08N_6	AK32		
6	IO_L09P_6	AM37		
6	IO_L09N_6/VREF_6	AM38		
6	IO_L10P_6	AM36		
6	IO_L10N_6	AL35		
6	IO_L11P_6	AJ31		
6	IO_L11N_6	AH30		
6	IO_L12P_6	AM33		
6	IO_L12N_6	AM34		
6	IO_L13P_6	AL38		
6	IO_L13N_6	AL39		
6	IO_L14P_6	AH29		
6	IO_L14N_6	AG29		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GND	W18		
N/A	GND	V18		
N/A	GND	U18		
N/A	GND	T18		
N/A	GND	AD17		
N/A	GND	AC17		
N/A	GND	AB17		
N/A	GND	AA17		
N/A	GND	Y17		
N/A	GND	W17		
N/A	GND	V17		
N/A	GND	U17		
N/A	GND	P20		
N/A	GND	L20		
N/A	GND	G20		
N/A	GND	C20		
N/A	GND	AD19		
N/A	GND	AC19		
N/A	GND	AB19		
N/A	GND	AA19		
N/A	GND	Y19		
N/A	GND	W19		
N/A	GND	V19		
N/A	GND	U19		
N/A	GND	T19		
N/A	GND	AD18		
N/A	GND	AC18		
N/A	GND	U21		
N/A	GND	T21		
N/A	GND	AU20		
N/A	GND	AN20		
N/A	GND	AJ20		
N/A	GND	AF20		
N/A	GND	AD20		
N/A	GND	AC20		
N/A	GND	AB20		
N/A	GND	AA20		
N/A	GND	Y20		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		E22		
N/A	GND		E21		
N/A	GND		E5		
N/A	GND		D39		
N/A	GND		D32		
N/A	GND		D28		
N/A	GND		D15		
N/A	GND		D11		
N/A	GND		D4		
N/A	GND		C42		
N/A	GND		C41		
N/A	GND		C40		
N/A	GND		C3		
N/A	GND		C2		
N/A	GND		C1		
N/A	GND		B42		
N/A	GND		B1		
N/A	GND		N14		
N/A	GND		N29		
N/A	GND		AK14		
N/A	GND		AK29		
N/A	GND		P13		
N/A	GND		P30		
N/A	GND		AJ13		
N/A	GND		AJ30		

Notes:

1. See Table 4 for an explanation of the signals available on this pin.

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
1	IO_L21P_1	H13	
1	IO_L20N_1	L12	
1	IO_L20P_1	K12	
1	IO_L19N_1	B11	
1	IO_L19P_1	A11	
1	IO_L09N_1/VREF_1	E11	
1	IO_L09P_1	D11	
1	IO_L08N_1	J11	
1	IO_L08P_1	H11	
1	IO_L07N_1	G11	
1	IO_L07P_1	F11	
1	IO_L06N_1	B10	
1	IO_L06P_1	A10	
1	IO_L05_1/No_Pair	G10	
1	IO_L03N_1/VREF_1	C10	
1	IO_L03P_1	C11	
1	IO_L02N_1	L11	
1	IO_L02P_1	K11	
1	IO_L01N_1/VRP_1	F10	
1	IO_L01P_1/VRN_1	E10	
2	IO_L01N_2/VRP_2	B8	
2	IO_L01P_2/VRN_2	A8	
2	IO_L02N_2	C9	
2	IO_L02P_2	B9	
2	IO_L03N_2	B7	
2	IO_L03P_2	A7	
2	IO_L04N_2/VREF_2	B6	
2	IO_L04P_2	A6	
2	IO_L05N_2	D8	
2	IO_L05P_2	D9	
2	IO_L06N_2	B4	
2	IO_L06P_2	A4	
2	IO_L73N_2	C7	
2	IO_L73P_2	C8	
2	IO_L74N_2	G9	
2	IO_L74P_2	F9	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L08N_7	N35	
7	IO_L07P_7	G41	
7	IO_L07N_7	G42	
7	IO_L72P_7	G39	
7	IO_L72N_7	G40	
7	IO_L71P_7	P32	
7	IO_L71N_7	P33	
7	IO_L70P_7	F38	
7	IO_L70N_7/VREF_7	G38	
7	IO_L69P_7	F37	
7	IO_L69N_7	G37	
7	IO_L68P_7	N32	
7	IO_L68N_7	N33	
7	IO_L67P_7	G35	
7	IO_L67N_7	G36	
7	IO_L66P_7	F41	
7	IO_L66N_7	F42	
7	IO_L65P_7	P31	
7	IO_L65N_7	N31	
7	IO_L64P_7	E41	
7	IO_L64N_7/VREF_7	F40	
7	IO_L63P_7	E36	
7	IO_L63N_7	F36	
7	IO_L62P_7	M34	
7	IO_L62N_7	M35	
7	IO_L61P_7	E35	
7	IO_L61N_7	F35	
7	IO_L84P_7	D40	
7	IO_L84N_7	E40	
7	IO_L83P_7	L34	
7	IO_L83N_7	L35	
7	IO_L82P_7	D39	
7	IO_L82N_7/VREF_7	E39	
7	IO_L81P_7	D38	
7	IO_L81N_7	E37	
7	IO_L80P_7	K34	
7	IO_L80N_7	J35	