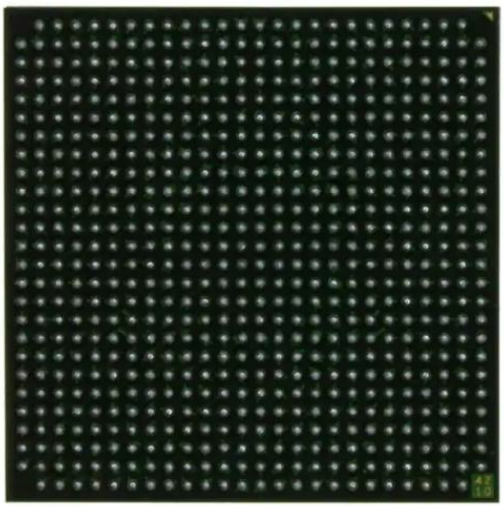

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 352 |
| Number of Logic Elements/Cells | 3168 |
| Total RAM Bits | 221184 |
| Number of I/O | 204 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-BBGA, FCBGA |
| Supplier Device Package | 672-FCBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2vp2-5ff672c |

# Functional Description: RocketIO X Multi-Gigabit Transceiver (MGT)

This section summarizes the features of the RocketIO X multi-gigabit transceiver. For an in-depth discussion of the RocketIO X MGT, including digital and analog design considerations, refer to the **RocketIO X Transceiver User Guide.**

## RocketIO X Overview

Either eight or twenty RocketIO X MGTs are available on the XC2VPX20 and XC2VPX70 devices, respectively. The XC2VPX20 MGT is designed to operate at any baud rate in the range of 2.488 Gb/s to 6.25 Gb/s per channel. This includes specific baud rates used by various standards as listed in Table 1. The XC2VPX70 MGT operates at a fixed 4.25 Gb/s per channel.

The RocketIO X MGT consists of the *Physical Media Attachment* (PMA) and *Physical Coding Sublayer* (PCS). The PMA contains the 6.25 Gb/s serializer/deserializer (SERDES), TX/RX buffers, clock generator, and clock recovery circuitry. The RocketIO X PCS has been significantly updated relative to the RocketIO PCS. In addition to the existing RocketIO PCS features, the RocketIO X PCS features 64B/66B encoder/decoder/scrambler/descrambler and SONET compatibility.

See Table 7, page 17, for a summary of the differences between the RocketIO X PMA/PCS and the RocketIO PMA/PCS.

Figure 4, page 3 shows a high-level block diagram of the RocketIO X transceiver and its FPGA interface signals.

*Table 1:* **Communications Standards Supported by RocketIO X Transceiver**(2)

| Mode | Channels (Lanes)(1) | I/O Bit Rate (Gb/s) |
|---|---|---|
| SONET OC-48 | 1 | 2.488 |
| PCI Express | 1, 2, 4, 8, 16 | 2.5 |
| Infiniband | 1, 4, 12 | 2.5 |
| XAUI (10-Gb Ethernet) | 4 | 3.125 |
| XAUI (10-Gb Fibre Channel) | 4 | 3.1875 |
| Aurora (Xilinx protocol) | 1, 2, 3, 4,... | 2.488 to 6.25 |
| Custom Mode | 1, 2, 3, 4,... | 2.488 to 6.25 |

**Notes:**
1. One channel is considered to be one transceiver.
2. XC2VPX70 operates at a fixed 4.25 Gb/s baud rate.

## PMA

### Transmitter Output

The RocketIO X transceiver is implemented in *Current Mode Logic* (CML). A CML transmitter output consists of transistors configured as shown in Figure 2. CML uses a positive supply and offers easy interface requirements. In this configuration, both legs of the driver, VP and VN, sink current, with one leg always sinking more current than its complement. The CML output consists of a differential pair with 50Ω source resistors. The signal swing is created by switching the current in a common-source differential pair.

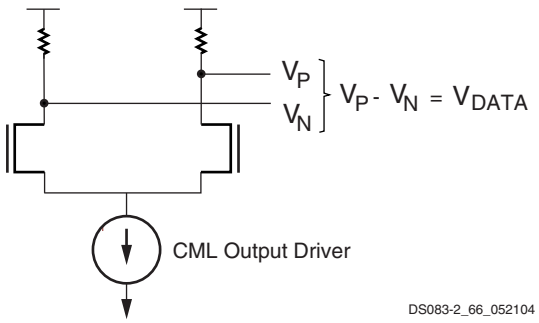


*Figure 2:* **CML Output Configuration**

### Transmitter Termination

On-chip termination is provided at the transmitter, eliminating the need for external termination. The output driver and termination are powered by $V_{TTX}$ at 1.5V. This configuration uses a CML approach with 50Ω termination to TXP and TXN as shown in Figure 3.

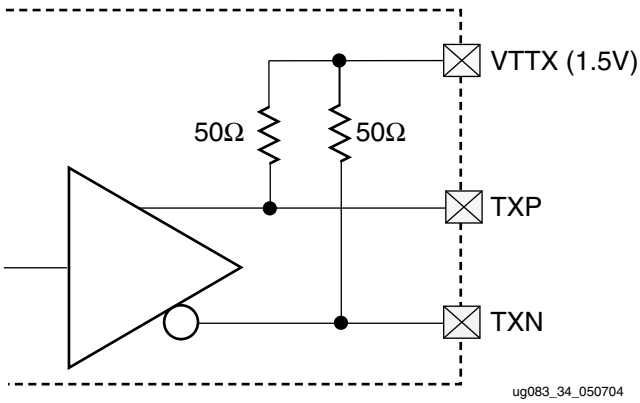


*Figure 3:* **RocketIO X Transmit Termination**

*Table 12:* **Summary of Voltage Supply Requirements for All Input and Output Standards**

| I/O Standard | $V_{CCO}$ | | $V_{REF}$ | Termination Type | |
|---|---|---|---|---|---|
| | Output | Input | Input | Output | Input |
| LVTTL(1) | 3.3 | 3.3 | N/R | N/R | N/R |
| LVCMOS33(1) | | | N/R | N/R | N/R |
| LVDCI_33(1) | | | N/R | Series | N/R |
| PCIX(2) | | | N/R | N/R | N/R |
| PCI33_3(2) | | | N/R | N/R | N/R |
| PCI66_3(2) | | | N/R | N/R | N/R |
| LVDS_25 | 2.5 | Note (3) | N/R | N/R | N/R |
| LVDSEXT_25 | | | N/R | N/R | N/R |
| LDT_25 | | | N/R | N/R | N/R |
| ULVDS_25 | | | N/R | N/R | N/R |
| BLVDS_25 | | | N/R | N/R | N/R |
| LVPECL_25 | | | N/R | N/R | N/R |
| SSTL2_I | | | 1.25 | N/R | N/R |
| SSTL2_II | | | 1.25 | N/R | N/R |
| LVCMOS25 | | 2.5 | N/R | N/R | N/R |
| LVDCI_25 | | | N/R | Series | N/R |
| LVDCI_DV2_25 | | | N/R | Series | N/R |
| LVDS_25_DCI | | | N/R | N/R | Split |
| LVDSEXT_25_DCI | | | N/R | N/R | Split |
| SSTL2_I_DCI | | | 1.25 | N/R | Split |
| SSTL2_II_DCI | | | 1.25 | Split | Split |
| LVDS_25_DT | | | N/R | N/R | N/R |
| LVDSEXT_25_DT | | | N/R | N/R | N/R |
| LDT_25_DT | | | N/R | N/R | N/R |
| ULVDS_25_DT | | | N/R | N/R | N/R |

*Table 12:* **Summary of Voltage Supply Requirements for All Input and Output Standards *(Continued)***

| I/O Standard | $V_{CCO}$ | | $V_{REF}$ | Termination Type | |
|---|---|---|---|---|---|
| | Output | Input | Input | Output | Input |
| HSTL_III_18 | 1.8 | Note (3) | 1.1 | N/R | N/R |
| HSTL_IV_18 | | | 1.1 | N/R | N/R |
| HSTL_I_18 | | | 0.9 | N/R | N/R |
| HSTL_II_18 | | | 0.9 | N/R | N/R |
| SSTL18_I | | | 0.9 | N/R | N/R |
| SSTL18_II | | | 0.9 | N/R | N/R |
| LVCMOS18 | | 1.8 | N/R | N/R | N/R |
| LVDCI_18 | | | N/R | Series | N/R |
| LVDCI_DV2_18 | | | N/R | Series | N/R |
| HSTL_III_DCI_18 | | | 1.1 | N/R | Single |
| HSTL_IV_DCI_18 | | | 1.1 | Single | Single |
| HSTL_I_DCI_18 | | | 0.9 | N/R | Split |
| HSTL_II_DCI_18 | | | 0.9 | Split | Split |
| SSTL18_I_DCI | | | 0.9 | N/R | Split |
| SSTL18_II_DCI | | | 0.9 | Split | Split |
| HSTL_III | 1.5 | Note (3) | 0.9 | N/R | N/R |
| HSTL_IV | | | 0.9 | N/R | N/R |
| HSTL_I | | | 0.75 | N/R | N/R |
| HSTL_II | | | 0.75 | N/R | N/R |
| LVCMOS15 | | 1.5 | N/R | N/R | N/R |
| LVDCI_15 | | | N/R | Series | N/R |
| LVDCI_DV2_15 | | | N/R | Series | N/R |
| GTLP_DCI | | | 1 | Single | Single |
| HSTL_III_DCI | | | 0.9 | N/R | Single |
| HSTL_IV_DCI | | | 0.9 | Single | Single |
| HSTL_I_DCI | | | 0.75 | N/R | Split |
| HSTL_II_DCI | | | 0.75 | Split | Split |
| GTL_DCI | 1.2 | 1.2 | 0.8 | Single | Single |
| GTLP | N/R | Note (3) | 1 | N/R | N/R |
| GTL | | | 0.8 | N/R | N/R |

**Notes:**
1. See application note **XAPP659** for more detailed information.
2. See application note **XAPP653** for more detailed information.
3. Pin voltage must not exceed $V_{CCO}$.
4. N/R = no requirement.

*Table 36:* **IOB Input Switching Characteristics Standard Adjustments *(Continued)***

| Description | IOSTANDARD Attribute | Timing Parameter | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -7 | -6 | -5 | |
| HSLVDCI, 1.8V | HSLVDCI_18 | $T_{IHSLVDCI\_18}$ | 0.59 | 0.68 | 0.75 | ns |
| HSLVDCI, 2.5V | HSLVDCI_25 | $T_{IHSLVDCI\_25}$ | 0.59 | 0.68 | 0.75 | ns |
| HSLVDCI, 3.3V | HSLVDCI_33 | $T_{IHSLVDCI\_33}$ | 0.59 | 0.68 | 0.75 | ns |
| GTL (Gunning Transceiver Logic) with DCI | GTL_DCI | $T_{IGTL\_DCI}$ | 0.49 | 0.57 | 0.62 | ns |
| GTL Plus with DCI | GTLP_DCI | $T_{IGTLP\_DCI}$ | 0.27 | 0.31 | 0.35 | ns |
| HSTL (High-Speed Transceiver Logic), Class I, with DCI | HSTL_I_DCI | $T_{IHSTL\_I\_DCI}$ | 0.27 | 0.31 | 0.35 | ns |
| HSTL, Class II, with DCI | HSTL_II_DCI | $T_{IHSTL\_II\_DCI}$ | 0.27 | 0.31 | 0.35 | ns |
| HSTL, Class III, with DCI | HSTL_III_DCI | $T_{IHSTL\_III\_DCI}$ | 0.27 | 0.31 | 0.35 | ns |
| HSTL, Class IV, with DCI | HSTL_IV_DCI | $T_{IHSTL\_IV\_DCI}$ | 0.27 | 0.31 | 0.35 | ns |
| HSTL, Class I, 1.8V, with DCI | HSTL_I_DCI_18 | $T_{IHSTL\_I\_DCI\_18}$ | 0.27 | 0.31 | 0.35 | ns |
| HSTL, Class II, 1.8V, with DCI | HSTL_II_DCI_18 | $T_{IHSTL\_II\_DCI\_18}$ | 0.27 | 0.31 | 0.35 | ns |
| HSTL, Class III, 1.8V, with DCI | HSTL_III_DCI_18 | $T_{IHSTL\_III\_DCI\_18}$ | 0.27 | 0.31 | 0.35 | ns |
| HSTL, Class IV, 1.8V, with DCI | HSTL_IV_DCI_18 | $T_{IHSTL\_IV\_DCI\_18}$ | 0.27 | 0.31 | 0.35 | ns |
| SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI | SSTL18_I_DCI | $T_{ISSTL18\_I\_DCI}$ | 0.62 | 0.72 | 0.79 | ns |
| SSTL, Class II, 1.8V, with DCI | SSTL18_II_DCI | $T_{ISSTL18\_II\_DCI}$ | 0.64 | 0.73 | 0.81 | ns |
| SSTL, Class I, 2.5V, with DCI | SSTL2_I_DCI | $T_{ISSTL2\_I\_DCI}$ | 0.17 | 0.20 | 0.22 | ns |
| SSTL, Class II, 2.5V, with DCI | SSTL2_II_DCI | $T_{ISSTL2\_II\_DCI}$ | 0.17 | 0.20 | 0.22 | ns |
| LVDS, 2.5V, with DCI | LVDS_25_DCI | $T_{ILVDS\_25\_DCI}$ | 0.31 | 0.36 | 0.40 | ns |
| LVDSEXT, 2.5V, with DCI | LVDSEXT_25_DCI | $T_{ILVDSEXT\_25\_DCI}$ | 0.33 | 0.37 | 0.41 | ns |
| LVDS, 2.5V, with Differential Termination (DT) | LVDS_25_DT | $T_{ILVDS\_25\_DT}$ | 0.31 | 0.36 | 0.40 | ns |
| LVDSEXT, 2.5V, with DT | LVDSEXT_25_DT | $T_{ILVDSEXT\_25\_DT}$ | 0.33 | 0.37 | 0.41 | ns |
| ULVDS, 2.5V, with DT | ULVDS_25_DT | $T_{IULVDS\_25\_DT}$ | 0.31 | 0.36 | 0.40 | ns |
| LDT, 2.5V, with DT | LDT_25_DT | $T_{ILDT\_25\_DT}$ | 0.31 | 0.36 | 0.40 | ns |

## IOB Output Switching Characteristics Standard Adjustments

Table 38 gives all standard-specific adjustments for output delays terminating at pads, based on standard capacitive load, $C_{REF}$. Output delays terminating at a pad are specified for LVCMOS25 with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

*Table 38:* **IOB Output Switching Characteristics Standard Adjustments**

| Description | IOSTANDARD Attribute | Timing Parameter | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -7 | -6 | -5 | |
| LVTTL (Low-Voltage Transistor-Transistor Logic), Slow, 2 mA | LVTTL_S2 | $T_{OLVTTL\_S2}$ | 5.42 | 6.24 | 6.86 | ns |
| LVTTL, Slow, 4 mA | LVTTL_S4 | $T_{OLVTTL\_S4}$ | 3.09 | 3.55 | 3.91 | ns |
| LVTTL, Slow, 6 mA | LVTTL_S6 | $T_{OLVTTL\_S6}$ | 2.26 | 2.60 | 2.86 | ns |
| LVTTL, Slow, 8 mA | LVTTL_S8 | $T_{OLVTTL\_S8}$ | 1.47 | 1.69 | 1.86 | ns |
| LVTTL, Slow, 12 mA | LVTTL_S12 | $T_{OLVTTL\_S12}$ | 1.02 | 1.18 | 1.29 | ns |
| LVTTL, Slow, 16 mA | LVTTL_S16 | $T_{OLVTTL\_S16}$ | 0.46 | 0.53 | 0.58 | ns |
| LVTTL, Slow, 24 mA | LVTTL_S24 | $T_{OLVTTL\_S24}$ | 0.37 | 0.42 | 0.47 | ns |
| LVTTL, Fast, 2 mA | LVTTL_F2 | $T_{OLVTTL\_F2}$ | 4.42 | 5.09 | 5.59 | ns |
| LVTTL, Fast, 4 mA | LVTTL_F4 | $T_{OLVTTL\_F4}$ | 1.95 | 2.24 | 2.46 | ns |
| LVTTL, Fast, 6 mA | LVTTL_F6 | $T_{OLVTTL\_F6}$ | 1.10 | 1.26 | 1.39 | ns |
| LVTTL, Fast, 8 mA | LVTTL_F8 | $T_{OLVTTL\_F8}$ | 0.40 | 0.46 | 0.51 | ns |
| LVTTL, Fast, 12 mA | LVTTL_F12 | $T_{OLVTTL\_F12}$ | 0.24 | 0.27 | 0.30 | ns |
| LVTTL, Fast, 16 mA | LVTTL_F16 | $T_{OLVTTL\_F16}$ | 0.05 | 0.06 | 0.07 | ns |
| LVTTL, Fast, 24 mA | LVTTL_F24 | $T_{OLVTTL\_F24}$ | –0.01 | –0.01 | –0.01 | ns |
| LVCMOS (Low-Voltage CMOS), 3.3V, Slow, 2 mA | LVCMOS33_S2 | $T_{OLVCMOS33\_S2}$ | 5.42 | 6.23 | 6.86 | ns |
| LVCMOS, 3.3V, Slow, 4 mA | LVCMOS33_S4 | $T_{OLVCMOS33\_S4}$ | 3.14 | 3.61 | 3.97 | ns |
| LVCMOS, 3.3V, Slow, 6 mA | LVCMOS33_S6 | $T_{OLVCMOS33\_S6}$ | 2.26 | 2.60 | 2.86 | ns |
| LVCMOS, 3.3V, Slow, 8 mA | LVCMOS33_S8 | $T_{OLVCMOS33\_S8}$ | 1.47 | 1.69 | 1.86 | ns |
| LVCMOS, 3.3V, Slow, 12 mA | LVCMOS33_S12 | $T_{OLVCMOS33\_S12}$ | 1.03 | 1.18 | 1.30 | ns |
| LVCMOS, 3.3V, Slow, 16 mA | LVCMOS33_S16 | $T_{OLVCMOS33\_S16}$ | 0.45 | 0.52 | 0.57 | ns |
| LVCMOS, 3.3V, Slow, 24 mA | LVCMOS33_S24 | $T_{OLVCMOS33\_S24}$ | 0.39 | 0.44 | 0.49 | ns |
| LVCMOS, 3.3V, Fast, 2 mA | LVCMOS33_F2 | $T_{OLVCMOS33\_F2}$ | 4.46 | 5.13 | 5.64 | ns |
| LVCMOS, 3.3V, Fast, 4 mA | LVCMOS33_F4 | $T_{OLVCMOS33\_F4}$ | 1.96 | 2.25 | 2.48 | ns |
| LVCMOS, 3.3V, Fast, 6 mA | LVCMOS33_F6 | $T_{OLVCMOS33\_F6}$ | 1.11 | 1.28 | 1.40 | ns |
| LVCMOS, 3.3V, Fast, 8 mA | LVCMOS33_F8 | $T_{OLVCMOS33\_F8}$ | 0.41 | 0.47 | 0.52 | ns |
| LVCMOS, 3.3V, Fast, 12 mA | LVCMOS33_F12 | $T_{OLVCMOS33\_F12}$ | 0.23 | 0.26 | 0.28 | ns |
| LVCMOS, 3.3V, Fast, 16 mA | LVCMOS33_F16 | $T_{OLVCMOS33\_F16}$ | 0.02 | 0.02 | 0.03 | ns |
| LVCMOS, 3.3V, Fast, 24 mA | LVCMOS33_F24 | $T_{OLVCMOS33\_F24}$ | –0.07 | –0.08 | –0.09 | ns |
| LVCMOS, 2.5V, Slow, 2 mA | LVCMOS25_S2 | $T_{OLVCMOS25\_S2}$ | 4.12 | 4.74 | 5.21 | ns |
| LVCMOS, 2.5V, Slow, 4 mA | LVCMOS25_S4 | $T_{OLVCMOS25\_S4}$ | 2.43 | 2.80 | 3.07 | ns |
| LVCMOS, 2.5V, Slow, 6 mA | LVCMOS25_S6 | $T_{OLVCMOS25\_S6}$ | 1.76 | 2.02 | 2.22 | ns |
| LVCMOS, 2.5V, Slow, 8 mA | LVCMOS25_S8 | $T_{OLVCMOS25\_S8}$ | 1.04 | 1.19 | 1.31 | ns |
| LVCMOS, 2.5V, Slow, 12 mA | LVCMOS25_S12 | $T_{OLVCMOS25\_S12}$ | 0.76 | 0.87 | 0.96 | ns |
| LVCMOS, 2.5V, Slow, 16 mA | LVCMOS25_S16 | $T_{OLVCMOS25\_S16}$ | 0.41 | 0.47 | 0.52 | ns |
| LVCMOS, 2.5V, Slow, 24 mA | LVCMOS25_S24 | $T_{OLVCMOS25\_S24}$ | 0.23 | 0.26 | 0.28 | ns |
| LVCMOS, 2.5V, Fast, 2 mA | LVCMOS25_F2 | $T_{OLVCMOS25\_F2}$ | 3.29 | 3.78 | 4.16 | ns |
| LVCMOS, 2.5V, Fast, 4 mA | LVCMOS25_F4 | $T_{OLVCMOS25\_F4}$ | 1.31 | 1.50 | 1.65 | ns |

## Input Clock Tolerances

*Table 58:* **Input Clock Tolerances**

| Description | Symbol | Constraints $F_{CLKIN}$ | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | –7 | | –6 | | –5 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| **Input Clock Low/High Pulse Width** | | | | | | | | | |
| PSCLK | PSCLK_PULSE | < 1MHz | 25.00 | | 25.00 | | 25.00 | | ns |
| PSCLK and CLKIN(3) | PSCLK_PULSE and CLKIN_PULSE | 1 – 10 MHz | 25.00 | | 25.00 | | 25.00 | | ns |
| | | 10 – 25 MHz | 10.00 | | 10.00 | | 10.00 | | ns |
| | | 25 – 50 MHz | 5.00 | | 5.00 | | 5.00 | | ns |
| | | 50 – 100 MHz | 3.00 | | 3.00 | | 3.00 | | ns |
| | | 100 – 150 MHz | 2.40 | | 2.40 | | 2.40 | | ns |
| | | 150 – 200 MHz | 2.00 | | 2.00 | | 2.00 | | ns |
| | | 200 – 250 MHz | 1.80 | | 1.80 | | 1.80 | | ns |
| | | 250 – 300 MHz | 1.50 | | 1.50 | | 1.50 | | ns |
| | | 300 – 350 MHz | 1.30 | | 1.30 | | 1.30 | | ns |
| | | 350 – 400 MHz | 1.15 | | 1.15 | | 1.15 | | ns |
| | | > 400 MHz | 1.05 | | 1.05 | | 1.05 | | ns |
| **Input Clock Cycle-Cycle Jitter (Low Frequency Mode)** | | | | | | | | | |
| CLKIN (using DLL outputs)(1) | CLKIN_CYC_JITT_DLL_LF | | | ±300 | | ±300 | | ±300 | ps |
| CLKIN (using CLKFX outputs)(2) | CLKIN_CYC_JITT_FX_LF | | | ±300 | | ±300 | | ±300 | ps |
| **Input Clock Cycle-Cycle Jitter (High Frequency Mode)** | | | | | | | | | |
| CLKIN (using DLL outputs)(1) | CLKIN_CYC_JITT_DLL_HF | | | ±150 | | ±150 | | ±150 | ps |
| CLKIN (using CLKFX outputs)(2) | CLKIN_CYC_JITT_FX_HF | | | ±150 | | ±150 | | ±150 | ps |
| **Input Clock Period Jitter (Low Frequency Mode)** | | | | | | | | | |
| CLKIN (using DLL outputs)(1) | CLKIN_PER_JITT_DLL_LF | | | ±1 | | ±1 | | ±1 | ns |
| CLKIN (using CLKFX outputs)(2) | CLKIN_PER_JITT_FX_LF | | | ±1 | | ±1 | | ±1 | ns |
| **Input Clock Period Jitter (High Frequency Mode)** | | | | | | | | | |
| CLKIN (using DLL outputs)(1) | CLKIN_PER_JITT_DLL_HF | | | ±1 | | ±1 | | ±1 | ns |
| CLKIN (using CLKFX outputs)(2) | CLKIN_PER_JITT_FX_HF | | | ±1 | | ±1 | | ±1 | ns |
| **Feedback Clock Path Delay Variation** | | | | | | | | | |
| CLKFB off-chip feedback | CLKFB_DELAY_VAR_EXT | | | ±1 | | ±1 | | ±1 | ns |

**Notes:**
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

## Miscellaneous Timing Parameters

*Table 61:* **Miscellaneous Timing Parameters**

| Description | Symbol | Constraints $F_{CLKIN}$ | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -7 | -6 | -5 | |
| **Time Required to Achieve LOCK** | | | | | | |
| Using DLL outputs(1) | LOCK_DLL: | | | | | |
| | LOCK_DLL_60 | > 60MHz | 20.00 | 20.00 | 20.00 | us |
| | LOCK_DLL_50_60 | 50 - 60 MHz | 25.00 | 25.00 | 25.00 | us |
| | LOCK_DLL_40_50 | 40 - 50 MHz | 50.00 | 50.00 | 50.00 | us |
| | LOCK_DLL_30_40 | 30 - 40 MHz | 90.00 | 90.00 | 90.00 | us |
| | LOCK_DLL_24_30 | 24 - 30 MHz | 120.00 | 120.00 | 120.00 | us |
| Using CLKFX outputs | LOCK_FX_MIN | | 10.00 | 10.00 | 10.00 | ms |
| | LOCK_FX_MAX | | 10.00 | 10.00 | 10.00 | ms |
| Additional lock time with fine phase shifting | LOCK_DLL_FINE_SHIFT | | 50.00 | 50.00 | 50.00 | us |
| **Fine Phase Shifting** | | | | | | |
| Absolute shifting range | FINE_SHIFT_RANGE | | 10.00 | 10.00 | 10.00 | ns |
| **Delay Lines** | | | | | | |
| Tap delay resolution | DCM_TAP_MIN | | 30.00 | 30.00 | 30.00 | ps |
| | DCM_TAP_MAX | | 50.00 | 50.00 | 50.00 | ps |

**Notes:**
1. “DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.

## Frequency Synthesis

*Table 62:* **Frequency Synthesis**

| Attribute | Min | Max |
|---|---|---|
| CLKFX_MULTIPLY | 2 | 32 |
| CLKFX_DIVIDE | 1 | 32 |

## Parameter Cross-Reference

*Table 63:* **Parameter Cross-Reference**

| Libraries Guide | Data Sheet |
|---|---|
| DLL_CLKOUT_{MIN\|MAX}_LF | CLKOUT_FREQ_{1X\|2X\|DV}_LF |
| DFS_CLKOUT_{MIN\|MAX}_LF | CLKOUT_FREQ_FX_LF |
| DLL_CLKIN_{MIN\|MAX}_LF | CLKIN_FREQ_DLL_LF |
| DFS_CLKIN_{MIN\|MAX}_LF | CLKIN_FREQ_FX_LF |
| DLL_CLKOUT_{MIN\|MAX}_HF | CLKOUT_FREQ_{1X\|DV}_HF |
| DFS_CLKOUT_{MIN\|MAX}_HF | CLKOUT_FREQ_FX_HF |
| DLL_CLKIN_{MIN\|MAX}_HF | CLKIN_FREQ_DLL_HF |
| DFS_CLKIN_{MIN\|MAX}_HF | CLKIN_FREQ_FX_HF |

# Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information

DS083 (v5.0) June 21, 2011 **Product Specification**

This document provides Virtex™-II Pro Device/Package Combinations, Maximum I/Os, and Virtex-II Pro Pin Definitions, followed by pinout tables, for these packages:

- FG256/FGG256 Fine-Pitch BGA Package
- FG456/FGG456 Fine-Pitch BGA Package
- FG676/FGG676 Fine-Pitch BGA Package
- FF672 Flip-Chip Fine-Pitch BGA Package
- FF896 Flip-Chip Fine-Pitch BGA Package
- FF1152 Flip-Chip Fine-Pitch BGA Package
- FF1148 Flip-Chip Fine-Pitch BGA Package
- FF1517 Flip-Chip Fine-Pitch BGA Package
- FF1704 Flip-Chip Fine-Pitch BGA Package
- FF1696 Flip-Chip Fine-Pitch BGA Package

For device pinout diagrams and layout guidelines, refer to the **Virtex-II Pro Platform FPGA User Guide**. ASCII package pinout files are also available for download from the Xilinx website (**www.xilinx.com**).

## Virtex-II Pro Device/Package Combinations and Maximum I/Os(1)

Wire-bond and flip-chip packages are available. Table 1 and Table 2 show the maximum number of user I/Os possible in wire-bond and flip-chip packages, respectively.

- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FGG denotes Pb-free wire-bond fine-pitch BGA (1.00 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch)

*Table 1:* **Wire-Bond Packages Information**

| Package(1) | FG256/ FGG256 | FG456/ FGG456 | FG676/ FGG676 |
|---|---|---|---|
| Pitch (mm) | 1.00 | 1.00 | 1.00 |
| Size (mm) | 17 x 17 | 23 x 23 | 26 x 26 |
| Maximum I/Os | 140 | 248 | 412 |

**Notes:**
1. Wire-bond packages include FGG*nnn* Pb-free versions. See Virtex-II Pro Ordering Examples (Module 1).

*Table 2:* **Flip-Chip Packages Information**

| Package | FF672 | FF896 | FF1152 | FF1148 | FF1517 | FF1704 | FF1696 |
|---|---|---|---|---|---|---|---|
| Pitch (mm) | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| Size (mm) | 27 x 27 | 31 x 31 | 35 x 35 | 35 x 35 | 40 x 40 | 42.5 x 42.5 | 42.5 x 42.5 |
| Maximum I/Os | 396 | 556 | 644 | 812 | 964 | 1040 | 1200 |

Table 3 shows the number of available I/Os, the number of RocketIO™ (or RocketIO X) multi-gigabit transceiver (MGT) pins, and the number of differential I/O pairs for each Virtex-II Pro device/package combination. The number of I/Os per package includes all user I/Os *except* the fifteen control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, and RSVD), the nine (per transceiver) RocketIO MGT pins (TXP, TXN, RXP, RXN, AVCCAUXTX, AVCCAUXRX, VTTX, VTRX, and GNDA), and for Virtex-II Pro X devices only, the two BREFCLKN/ BREFCLKP differential clock input pairs (four pins). The Virtex-II Pro X devices are highlighted in bold type.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

*Table 3:* **Virtex-II Pro Available I/Os and RocketIO MGT Pins per Device/Package Combination**

| Virtex-II Pro Device | User I/Os & RocketIO MGT Pins | Virtex-II Pro Package[1] | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | FG256/ FGG256 | FG456/ FGG456 | FG676/ FGG456 | FF672 | FF896 | FF1152 | FF1148 | FF1517 | FF1704 | FF1696 |
| XC2VP2 | Available User I/Os | 140 | 156 | - | 204 | - | - | - | - | - | - |
| | RocketIO MGT Pins | 36 | 36 | - | 36 | - | - | - | - | - | - |
| | Differential I/O Pairs | 68 | 76 | - | 100 | - | - | - | - | - | - |
| XC2VP4 | Available User I/Os | 140 | 248 | - | 348 | - | - | - | - | - | - |
| | RocketIO MGT Pins | 36 | 36 | - | 36 | - | - | - | - | - | - |
| | Differential I/O Pairs | 68 | 122 | - | 172 | - | - | - | - | - | - |
| XC2VP7 | Available User I/Os | - | 248 | - | 396 | 396 | - | - | - | - | - |
| | RocketIO MGT Pins | - | 72 | - | 72 | 72 | - | - | - | - | - |
| | Differential I/O Pairs | - | 122 | - | 196 | 196 | - | - | - | - | - |
| XC2VP20 | Available User I/Os | - | - | 404 | - | 556 | 564 | - | - | - | - |
| | RocketIO MGT Pins | - | - | 72 | - | 72 | 72 | - | - | - | - |
| | Differential I/O Pairs | - | - | 196 | - | 272 | 276 | - | - | - | - |
| **XC2VPX20** | **Available User I/Os** | **-** | **-** | **-** | **-** | **552** | **-** | **-** | **-** | **-** | **-** |
| | **RocketIO X MGT Pins** | **-** | **-** | **-** | **-** | **72** | **-** | **-** | **-** | **-** | **-** |
| | **Differential I/O Pairs** | **-** | **-** | **-** | **-** | **270** | **-** | **-** | **-** | **-** | **-** |
| XC2VP30 | Available User I/Os | - | - | 416 | - | 556 | 644 | - | - | - | - |
| | RocketIO MGT Pins | - | - | 72 | - | 72 | 72 | - | - | - | - |
| | Differential I/O Pairs | - | - | 202 | - | 272 | 316 | - | - | - | - |
| XC2VP40 | Available User I/Os | - | - | 416 | - | - | 692 | 804 | - | - | - |
| | RocketIO MGT Pins | - | - | 72 | - | - | 108 | 0 | - | - | - |
| | Differential I/O Pairs | - | - | 202 | - | - | 340 | 396 | - | - | - |
| XC2VP50 | Available User I/Os | - | - | | - | - | 692 | 812 | 852 | - | - |
| | RocketIO MGT Pins | - | - | | - | - | 144 | 0 | 144 | - | - |
| | Differential I/O Pairs | - | - | | - | - | 340 | 400 | 420 | - | - |

*Table 5:* **FG256/FGG256 — XC2VP2 and XC2VP4**

| Bank | Pin Description | Pin Number |
|---|---|---|
| N/A | GND | R15 |
| N/A | GND | L6 |
| N/A | GND | L11 |
| N/A | GND | K9 |
| N/A | GND | K8 |
| N/A | GND | K7 |
| N/A | GND | K10 |
| N/A | GND | J9 |
| N/A | GND | J8 |
| N/A | GND | J7 |
| N/A | GND | J10 |
| N/A | GND | H9 |
| N/A | GND | H8 |
| N/A | GND | H7 |
| N/A | GND | H10 |
| N/A | GND | G9 |
| N/A | GND | G8 |
| N/A | GND | G7 |
| N/A | GND | G10 |
| N/A | GND | F6 |
| N/A | GND | F11 |
| N/A | GND | B2 |
| N/A | GND | B15 |
| N/A | GND | A16 |
| N/A | GND | A1 |

**Notes:**
1. See Table 4 for an explanation of the signals available on this pin.

*Table 7:* **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 |
| N/A | RSVD | C23 | | | |
| N/A | VBATT | A24 | | | |
| N/A | TMS | B24 | | | |
| N/A | TCK | B26 | | | |
| N/A | TDO | D24 | | | |
| N/A | CCLK | AE24 | | | |
| N/A | PWRDWN_B | AF24 | | | |
| N/A | DONE | AD23 | | | |
| N/A | AVCCAUXRX16 | AE23 | | | |
| N/A | VTRXPAD16 | AE22 | | | |
| N/A | RXNPAD16 | AF23 | | | |
| N/A | RXPPAD16 | AF22 | | | |
| N/A | GNDA16 | AD21 | | | |
| N/A | TXPPAD16 | AF21 | | | |
| N/A | TXNPAD16 | AF20 | | | |
| N/A | VTTXPAD16 | AE20 | | | |
| N/A | AVCCAUXTX16 | AE21 | | | |
| N/A | AVCCAUXRX18 | AE18 | | | |
| N/A | VTRXPAD18 | AE17 | | | |
| N/A | RXNPAD18 | AF18 | | | |
| N/A | RXPPAD18 | AF17 | | | |
| N/A | GNDA18 | AD16 | | | |
| N/A | TXPPAD18 | AF16 | | | |
| N/A | TXNPAD18 | AF15 | | | |
| N/A | VTTXPAD18 | AE15 | | | |
| N/A | AVCCAUXTX18 | AE16 | | | |
| N/A | AVCCAUXRX19 | AE12 | | | |
| N/A | VTRXPAD19 | AE11 | | | |
| N/A | RXNPAD19 | AF12 | | | |
| N/A | RXPPAD19 | AF11 | | | |
| N/A | GNDA19 | AD11 | | | |
| N/A | TXPPAD19 | AF10 | | | |
| N/A | TXNPAD19 | AF9 | | | |
| N/A | VTTXPAD19 | AE9 | | | |
| N/A | AVCCAUXTX19 | AE10 | | | |

*Table 10:* **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | | | |
|---|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 |
| 7 | IO_L18N_7 | L25 | NC | | | |
| 7 | IO_L17P_7 | F34 | NC | | | |
| 7 | IO_L17N_7 | F33 | NC | | | |
| 7 | IO_L16P_7 | G30 | NC | | | |
| 7 | IO_L16N_7/VREF_7 | G29 | NC | | | |
| 7 | IO_L15P_7 | G32 | NC | | | |
| 7 | IO_L15N_7 | G31 | NC | | | |
| 7 | IO_L06P_7 | F31 | | | | |
| 7 | IO_L06N_7 | F30 | | | | |
| 7 | IO_L05P_7 | J28 | | | | |
| 7 | IO_L05N_7 | J27 | | | | |
| 7 | IO_L04P_7 | E34 | | | | |
| 7 | IO_L04N_7/VREF_7 | E33 | | | | |
| 7 | IO_L03P_7 | E32 | | | | |
| 7 | IO_L03N_7 | E31 | | | | |
| 7 | IO_L02P_7 | F28 | | | | |
| 7 | IO_L02N_7 | F27 | | | | |
| 7 | IO_L01P_7/VRN_7 | D34 | | | | |
| 7 | IO_L01N_7/VRP_7 | D33 | | | | |
| | | | | | | |
| 0 | VCCO_0 | C29 | | | | |
| 0 | VCCO_0 | E20 | | | | |
| 0 | VCCO_0 | F25 | | | | |
| 0 | VCCO_0 | L20 | | | | |
| 0 | VCCO_0 | L21 | | | | |
| 0 | VCCO_0 | L22 | | | | |
| 0 | VCCO_0 | L23 | | | | |
| 0 | VCCO_0 | M18 | | | | |
| 0 | VCCO_0 | M19 | | | | |
| 0 | VCCO_0 | M20 | | | | |
| 0 | VCCO_0 | M21 | | | | |
| 0 | VCCO_0 | M22 | | | | |
| 1 | VCCO_1 | C6 | | | | |
| 1 | VCCO_1 | E15 | | | | |
| 1 | VCCO_1 | F10 | | | | |
| 1 | VCCO_1 | L12 | | | | |
| 1 | VCCO_1 | L13 | | | | |
| 1 | VCCO_1 | L14 | | | | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| 7 | VCCO_7 | U23 | | |
| 7 | VCCO_7 | T23 | | |
| 7 | VCCO_7 | R23 | | |
| 7 | VCCO_7 | P23 | | |
| 7 | VCCO_7 | N23 | | |
| 6 | VCCO_6 | AK33 | | |
| 6 | VCCO_6 | AM31 | | |
| 6 | VCCO_6 | AH31 | | |
| 6 | VCCO_6 | AD31 | | |
| 6 | VCCO_6 | Y31 | | |
| 6 | VCCO_6 | AM27 | | |
| 6 | VCCO_6 | AH27 | | |
| 6 | VCCO_6 | AD27 | | |
| 6 | VCCO_6 | Y27 | | |
| 6 | VCCO_6 | AF26 | | |
| 6 | VCCO_6 | AC24 | | |
| 6 | VCCO_6 | AB23 | | |
| 6 | VCCO_6 | AA23 | | |
| 6 | VCCO_6 | Y23 | | |
| 6 | VCCO_6 | W23 | | |
| 6 | VCCO_6 | V23 | | |
| 5 | VCCO_5 | AL24 | | |
| 5 | VCCO_5 | AG24 | | |
| 5 | VCCO_5 | AD23 | | |
| 5 | VCCO_5 | AC22 | | |
| 5 | VCCO_5 | AC21 | | |
| 5 | VCCO_5 | AL20 | | |
| 5 | VCCO_5 | AG20 | | |
| 5 | VCCO_5 | AC20 | | |
| 5 | VCCO_5 | AC19 | | |
| 5 | VCCO_5 | AC18 | | |
| 4 | VCCO_4 | AC17 | | |
| 4 | VCCO_4 | AC16 | | |
| 4 | VCCO_4 | AL15 | | |
| 4 | VCCO_4 | AG15 | | |
| 4 | VCCO_4 | AC15 | | |
| 4 | VCCO_4 | AC14 | | |
| 4 | VCCO_4 | AC13 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 5 | IO_L57N_5/VREF_5 | AT23 | | |
| 5 | IO_L57P_5 | AU23 | | |
| 5 | IO_L56N_5 | AJ22 | | |
| 5 | IO_L56P_5 | AK22 | | |
| 5 | IO_L55N_5 | AN23 | | |
| 5 | IO_L55P_5 | AP24 | | |
| 5 | IO_L54N_5 | AL23 | | |
| 5 | IO_L54P_5 | AM23 | | |
| 5 | IO_L53_5/No_Pair | AH23 | | |
| 5 | IO_L50_5/No_Pair | AG23 | | |
| 5 | IO_L49N_5 | AR24 | | |
| 5 | IO_L49P_5 | AR25 | | |
| 5 | IO_L48N_5 | AL24 | | |
| 5 | IO_L48P_5 | AM24 | | |
| 5 | IO_L47N_5 | AH22 | | |
| 5 | IO_L47P_5 | AJ23 | | |
| 5 | IO_L46N_5 | AT25 | | |
| 5 | IO_L46P_5 | AU25 | | |
| 5 | IO_L45N_5/VREF_5 | AN25 | | |
| 5 | IO_L45P_5 | AP25 | | |
| 5 | IO_L44N_5 | AH24 | | |
| 5 | IO_L44P_5 | AH25 | | |
| 5 | IO_L43N_5 | AL25 | | |
| 5 | IO_L43P_5 | AM25 | | |
| 5 | IO_L39N_5 | AT26 | | |
| 5 | IO_L39P_5 | AU26 | | |
| 5 | IO_L38N_5 | AK24 | | |
| 5 | IO_L38P_5 | AK25 | | |
| 5 | IO_L37N_5 | AP26 | | |
| 5 | IO_L37P_5 | AR26 | | |
| 5 | IO_L36N_5/VREF_5 | AM26 | NC | |
| 5 | IO_L36P_5 | AN26 | NC | |
| 5 | IO_L35N_5 | AJ25 | NC | |
| 5 | IO_L35P_5 | AJ26 | NC | |
| 5 | IO_L34N_5 | AR27 | NC | |
| 5 | IO_L34P_5 | AT27 | NC | |
| 5 | IO_L30N_5 | AN27 | NC | |
| 5 | IO_L30P_5 | AP28 | NC | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 7 | IO_L24N_7 | L37 | | |
| 7 | IO_L23P_7 | P31 | | |
| 7 | IO_L23N_7 | P32 | | |
| 7 | IO_L22P_7 | L34 | | |
| 7 | IO_L22N_7/VREF_7 | L35 | | |
| 7 | IO_L21P_7 | L32 | | |
| 7 | IO_L21N_7 | L33 | | |
| 7 | IO_L20P_7 | N29 | | |
| 7 | IO_L20N_7 | M29 | | |
| 7 | IO_L19P_7 | K38 | | |
| 7 | IO_L19N_7 | K39 | | |
| 7 | IO_L18P_7 | J37 | | |
| 7 | IO_L18N_7 | K37 | | |
| 7 | IO_L17P_7 | N30 | | |
| 7 | IO_L17N_7 | P30 | | |
| 7 | IO_L16P_7 | K35 | | |
| 7 | IO_L16N_7/VREF_7 | K36 | | |
| 7 | IO_L15P_7 | K34 | | |
| 7 | IO_L15N_7 | K33 | | |
| 7 | IO_L14P_7 | N31 | | |
| 7 | IO_L14N_7 | M32 | | |
| 7 | IO_L13P_7 | J38 | | |
| 7 | IO_L13N_7 | J39 | | |
| 7 | IO_L12P_7 | J35 | | |
| 7 | IO_L12N_7 | H36 | | |
| 7 | IO_L11P_7 | M30 | | |
| 7 | IO_L11N_7 | L31 | | |
| 7 | IO_L10P_7 | J33 | | |
| 7 | IO_L10N_7/VREF_7 | J34 | | |
| 7 | IO_L09P_7 | H37 | | |
| 7 | IO_L09N_7 | H38 | | |
| 7 | IO_L08P_7 | K31 | | |
| 7 | IO_L08N_7 | K32 | | |
| 7 | IO_L07P_7 | H33 | | |
| 7 | IO_L07N_7 | H34 | | |
| 7 | IO_L84P_7 | G38 | NC | |
| 7 | IO_L84N_7 | G39 | NC | |
| 7 | IO_L82P_7 | G36 | NC | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 2 | VCCO_2 | F8 | | |
| 2 | VCCO_2 | U7 | | |
| 2 | VCCO_2 | Y5 | | |
| 2 | VCCO_2 | N4 | | |
| 2 | VCCO_2 | J4 | | |
| 2 | VCCO_2 | E4 | | |
| 2 | VCCO_2 | U3 | | |
| 2 | VCCO_2 | E1 | | |
| 1 | VCCO_1 | N14 | | |
| 1 | VCCO_1 | K13 | | |
| 1 | VCCO_1 | F13 | | |
| 1 | VCCO_1 | P19 | | |
| 1 | VCCO_1 | P18 | | |
| 1 | VCCO_1 | P17 | | |
| 1 | VCCO_1 | K17 | | |
| 1 | VCCO_1 | F17 | | |
| 1 | VCCO_1 | P16 | | |
| 1 | VCCO_1 | N16 | | |
| 1 | VCCO_1 | P15 | | |
| 1 | VCCO_1 | N15 | | |
| 0 | VCCO_0 | K27 | | |
| 0 | VCCO_0 | F27 | | |
| 0 | VCCO_0 | N26 | | |
| 0 | VCCO_0 | P25 | | |
| 0 | VCCO_0 | N25 | | |
| 0 | VCCO_0 | P24 | | |
| 0 | VCCO_0 | N24 | | |
| 0 | VCCO_0 | P23 | | |
| 0 | VCCO_0 | K23 | | |
| 0 | VCCO_0 | F23 | | |
| 0 | VCCO_0 | P22 | | |
| 0 | VCCO_0 | P21 | | |
| | | | | |
| N/A | CCLK | AJ10 | | |
| N/A | PROG_B | D32 | | |
| N/A | DONE | AJ11 | | |
| N/A | M0 | AP31 | | |
| N/A | M1 | AJ30 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 7 | IO_L09P_7 | | K36 | | |
| 7 | IO_L09N_7 | | K35 | | |
| 7 | IO_L08P_7 | | K38 | | |
| 7 | IO_L08N_7 | | K37 | | |
| 7 | IO_L07P_7 | | L33 | | |
| 7 | IO_L07N_7 | | K34 | | |
| 7 | IO_L84P_7 | | J41 | | |
| 7 | IO_L84N_7 | | J42 | | |
| 7 | IO_L83P_7 | | J39 | | |
| 7 | IO_L83N_7 | | J38 | | |
| 7 | IO_L82P_7 | | J36 | | |
| 7 | IO_L82N_7/VREF_7 | | J37 | | |
| 7 | IO_L81P_7 | | J35 | | |
| 7 | IO_L81N_7 | | H36 | | |
| 7 | IO_L80P_7 | | H41 | | |
| 7 | IO_L80N_7 | | H40 | | |
| 7 | IO_L79P_7 | | H38 | | |
| 7 | IO_L79N_7 | | H39 | | |
| 7 | IO_L78P_7 | | H37 | | |
| 7 | IO_L78N_7 | | G38 | | |
| 7 | IO_L77P_7 | | G42 | | |
| 7 | IO_L77N_7 | | G41 | | |
| 7 | IO_L76P_7 | | G39 | | |
| 7 | IO_L76N_7/VREF_7 | | G40 | | |
| 7 | IO_L75P_7 | | F41 | | |
| 7 | IO_L75N_7 | | F42 | | |
| 7 | IO_L74P_7 | | F40 | | |
| 7 | IO_L74N_7 | | F39 | | |
| 7 | IO_L73P_7 | | E41 | | |
| 7 | IO_L73N_7 | | E42 | | |
| 7 | IO_L06P_7 | | D41 | | |
| 7 | IO_L06N_7 | | D42 | | |
| 7 | IO_L05P_7 | | E40 | | |
| 7 | IO_L05N_7 | | D40 | | |
| 7 | IO_L04P_7 | | F36 | | |
| 7 | IO_L04N_7/VREF_7 | | G37 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| N/A | VCCINT | | AF16 | | |
| N/A | VCCINT | | AG27 | | |
| N/A | VCCINT | | AG26 | | |
| N/A | VCCINT | | AG25 | | |
| N/A | VCCINT | | AG24 | | |
| N/A | VCCINT | | AG23 | | |
| N/A | VCCINT | | AG22 | | |
| N/A | VCCINT | | AG21 | | |
| N/A | VCCINT | | AG20 | | |
| N/A | VCCINT | | AG19 | | |
| N/A | VCCINT | | AG18 | | |
| N/A | VCCINT | | AG17 | | |
| N/A | VCCINT | | AG16 | | |
| N/A | VCCINT | | AH28 | | |
| N/A | VCCINT | | AH27 | | |
| N/A | VCCINT | | AH26 | | |
| N/A | VCCINT | | AH17 | | |
| N/A | VCCINT | | AH16 | | |
| N/A | VCCINT | | AH15 | | |
| N/A | VCCINT | | AJ29 | | |
| N/A | VCCINT | | AJ28 | | |
| N/A | VCCINT | | AJ27 | | |
| N/A | VCCINT | | AJ16 | | |
| N/A | VCCINT | | AJ15 | | |
| N/A | VCCINT | | AJ14 | | |
| N/A | VCCINT | | AK30 | | |
| N/A | VCCINT | | AK13 | | |
| N/A | VCCINT | | AA27 | | |
| N/A | VCCINT | | AA16 | | |
| N/A | VCCINT | | Y27 | | |
| N/A | VCCINT | | Y16 | | |
| N/A | VCCINT | | W27 | | |
| N/A | VCCINT | | W16 | | |
| N/A | VCCINT | | V27 | | |
| N/A | VCCINT | | V16 | | |
| N/A | VCCINT | | U27 | | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 4 | IO_L26P_4 | AU12 | |
| 4 | IO_L27N_4 | AR12 | |
| 4 | IO_L27P_4/VREF_4 | AP12 | |
| 4 | IO_L28N_4 | AW13 | |
| 4 | IO_L28P_4 | AW12 | |
| 4 | IO_L29N_4 | BA12 | |
| 4 | IO_L29P_4 | AY12 | |
| 4 | IO_L30N_4 | AN13 | |
| 4 | IO_L30P_4 | AM13 | |
| 4 | IO_L34N_4 | AU13 | |
| 4 | IO_L34P_4 | AT13 | |
| 4 | IO_L35N_4 | BA13 | |
| 4 | IO_L35P_4 | AY13 | |
| 4 | IO_L36N_4 | AM14 | |
| 4 | IO_L36P_4/VREF_4 | AL14 | |
| 4 | IO_L76N_4 | AR15 | |
| 4 | IO_L76P_4 | AT14 | |
| 4 | IO_L77N_4 | AV14 | |
| 4 | IO_L77P_4 | AU14 | |
| 4 | IO_L78N_4 | AP14 | |
| 4 | IO_L78P_4 | AN14 | |
| 4 | IO_L79N_4 | AW15 | |
| 4 | IO_L79P_4 | AY14 | |
| 4 | IO_L80_4/No_Pair | BB14 | |
| 4 | IO_L83_4/No_Pair | BA14 | |
| 4 | IO_L84N_4 | AM15 | |
| 4 | IO_L84P_4 | AL15 | |
| 4 | IO_L85N_4 | AT16 | |
| 4 | IO_L85P_4 | AT15 | |
| 4 | IO_L86N_4 | AV15 | |
| 4 | IO_L86P_4 | AU15 | |
| 4 | IO_L87N_4 | AP15 | |
| 4 | IO_L87P_4/VREF_4 | AN15 | |
| 4 | IO_L37N_4 | AY16 | |
| 4 | IO_L37P_4 | AY15 | |
| 4 | IO_L38N_4 | BB15 | |
| 4 | IO_L38P_4 | BA15 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 5 | IO_L10N_5 | AW27 | NC |
| 5 | IO_L10P_5 | AW26 | NC |
| 5 | IO_L45N_5/VREF_5 | AN27 | |
| 5 | IO_L45P_5 | AP27 | |
| 5 | IO_L44N_5 | AU27 | |
| 5 | IO_L44P_5 | AV27 | |
| 5 | IO_L43N_5 | AR27 | |
| 5 | IO_L43P_5 | AR26 | |
| 5 | IO_L39N_5 | AL27 | |
| 5 | IO_L39P_5 | AM27 | |
| 5 | IO_L38N_5 | BA28 | |
| 5 | IO_L38P_5 | BB28 | |
| 5 | IO_L37N_5 | AY28 | |
| 5 | IO_L37P_5 | AY27 | |
| 5 | IO_L87N_5/VREF_5 | AN28 | |
| 5 | IO_L87P_5 | AP28 | |
| 5 | IO_L86N_5 | AU28 | |
| 5 | IO_L86P_5 | AV28 | |
| 5 | IO_L85N_5 | AT28 | |
| 5 | IO_L85P_5 | AT27 | |
| 5 | IO_L84N_5 | AL28 | |
| 5 | IO_L84P_5 | AM28 | |
| 5 | IO_L83_5/No_Pair | BA29 | |
| 5 | IO_L80_5/No_Pair | BB29 | |
| 5 | IO_L79N_5 | AY29 | |
| 5 | IO_L79P_5 | AW28 | |
| 5 | IO_L78N_5 | AN29 | |
| 5 | IO_L78P_5 | AP29 | |
| 5 | IO_L77N_5 | AU29 | |
| 5 | IO_L77P_5 | AV29 | |
| 5 | IO_L76N_5 | AT29 | |
| 5 | IO_L76P_5 | AR28 | |
| 5 | IO_L36N_5/VREF_5 | AL29 | |
| 5 | IO_L36P_5 | AM29 | |
| 5 | IO_L35N_5 | AY30 | |
| 5 | IO_L35P_5 | BA30 | |
| 5 | IO_L34N_5 | AT30 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 7 | IO_L79P_7 | D41 | |
| 7 | IO_L79N_7 | D42 | |
| 7 | IO_L78P_7 | C39 | |
| 7 | IO_L78N_7 | C40 | |
| 7 | IO_L77P_7 | H34 | |
| 7 | IO_L77N_7 | H35 | |
| 7 | IO_L76P_7 | C37 | |
| 7 | IO_L76N_7/VREF_7 | D36 | |
| 7 | IO_L75P_7 | B38 | |
| 7 | IO_L75N_7 | C38 | |
| 7 | IO_L74P_7 | F34 | |
| 7 | IO_L74N_7 | G34 | |
| 7 | IO_L73P_7 | C35 | |
| 7 | IO_L73N_7 | C36 | |
| 7 | IO_L06P_7 | A39 | |
| 7 | IO_L06N_7 | B39 | |
| 7 | IO_L05P_7 | D34 | |
| 7 | IO_L05N_7 | D35 | |
| 7 | IO_L04P_7 | A37 | |
| 7 | IO_L04N_7/VREF_7 | B37 | |
| 7 | IO_L03P_7 | A36 | |
| 7 | IO_L03N_7 | B36 | |
| 7 | IO_L02P_7 | B34 | |
| 7 | IO_L02N_7 | C34 | |
| 7 | IO_L01P_7/VRN_7 | A35 | |
| 7 | IO_L01N_7/VRP_7 | B35 | |
| | | | |
| 7 | VCCO_7 | W39 | |
| 7 | VCCO_7 | P39 | |
| 7 | VCCO_7 | K39 | |
| 7 | VCCO_7 | F39 | |
| 7 | VCCO_7 | D37 | |
| 7 | VCCO_7 | W35 | |
| 7 | VCCO_7 | P35 | |
| 7 | VCCO_7 | K35 | |
| 7 | VCCO_7 | M33 | |
| 7 | VCCO_7 | H33 | |