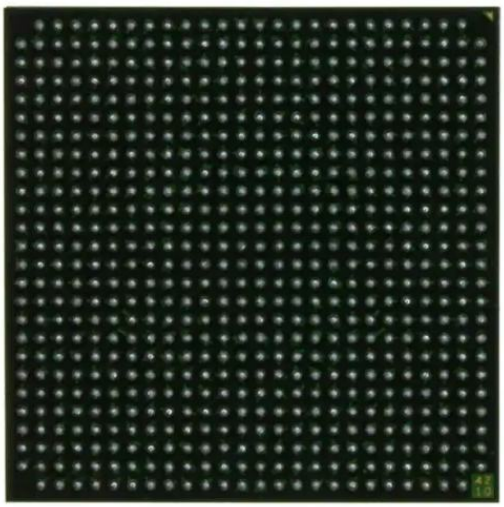

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	352
Number of Logic Elements/Cells	3168
Total RAM Bits	221184
Number of I/O	204
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp2-5ffg672c

Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description

DS083 (v5.0) June 21, 2011 **Product Specification**

Virtex-II Pro[1] Array Functional Description

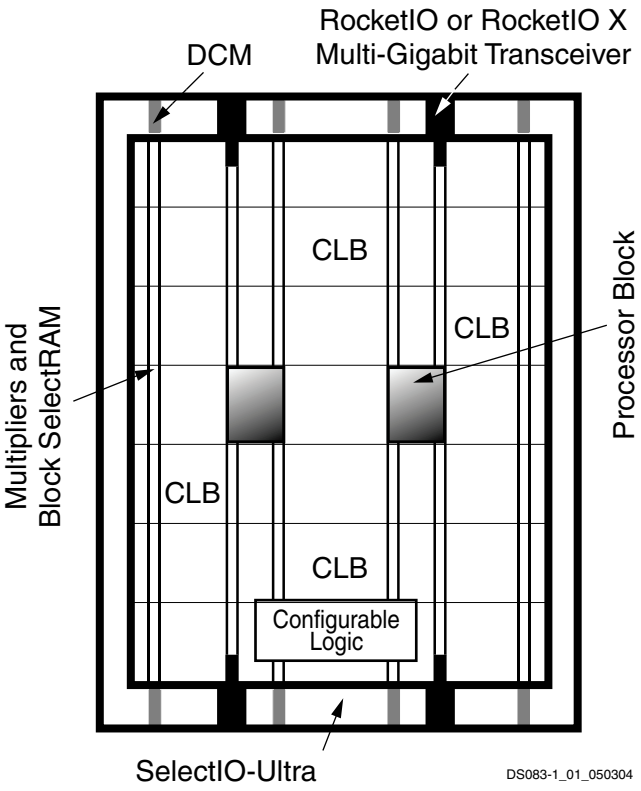


Figure 1: **Virtex-II Pro Generic Architecture Overview**

This module describes the following Virtex™-II Pro functional components, as shown in Figure 1:

- Embedded RocketIO™ (up to 3.125 Gb/s) or RocketIO X (up to 6.25 Gb/s) Multi-Gigabit Transceivers (MGTs)
- Processor blocks with embedded IBM PowerPC™ 405 RISC CPU core (PPC405) and integration circuitry.
- FPGA fabric based on Virtex-II architecture.

Virtex-II Pro User Guides

Virtex-II Pro User Guides cover theory of operation in more detail, and include implementation details, primitives and attributes, command/instruction sets, and many HDL code examples where appropriate. All parameter specifications are given only in Module 3 of this Data Sheet.

These User Guides are available:

- For detailed descriptions of PPC405 embedded core programming models and internal core operations, see **PowerPC Processor Reference Guide** and **PowerPC 405 Processor Block Reference Guide**.
- For detailed RocketIO transceiver digital/analog design considerations, see **RocketIO Transceiver User Guide**.
- For detailed RocketIO X transceiver digital/analog design considerations, see **RocketIO X Transceiver User Guide**,
- For detailed descriptions of the FPGA fabric (CLB, IOB, DCM, etc.), see **Virtex-II Pro Platform FPGA User Guide**.

All of the documents above, as well as a complete listing and description of Xilinx-developed Intellectual Property cores for Virtex-II Pro, are available on the Xilinx website.

Contents of This Module

Virtex-II Pro Compared to Virtex-II Devices

Virtex-II Pro devices are built on the Virtex-II FPGA architecture. Most FPGA features are identical to Virtex-II devices. Major differences are described below:

- The Virtex-II Pro FPGA family is the first to incorporate embedded PPC405 and RocketIO/RocketIO X cores.
- V_{CCAUX}, the auxiliary supply voltage, is 2.5V instead of 3.3V as for Virtex-II devices. Advanced processing at 0.13 µm has resulted in a smaller die, faster speed, and lower power consumption.
- Virtex-II Pro devices are neither bitstream-compatible nor pin-compatible with Virtex-II devices. However, Virtex-II designs can be compiled into Virtex-II Pro devices.
- On-chip input LVDS differential termination is available.
- SSTL3, AGP-2X/AGP, LVPECL_33, LVDS_33, and LVDSEXT_33 standards are not supported.
- The open-drain output pin TDO does not have an internal pull-up resistor.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

Table 5: **Clock Ratios for Various Data Widths**

Fabric Data Width	Frequency Ratio of USRCLK:USRCLK2
1-byte	1:2 (1)
2-byte	1:1
4-byte	2:1 (1)

Notes:
1. Each edge of slower clock must align with falling edge of faster clock.

FPGA Transmit Interface

The FPGA can send either one, two, or four characters of data to the transmitter. Each character can be either 8 bits or 10 bits wide. If 8-bit data is applied, the additional inputs become control signals for the 8B/10B encoder. When the 8B/10B encoder is bypassed, the 10-bit character order is generated as follows:

TXCHARDISPMODE[0] (first bit transmitted)
TXCHARDISPVAL[0]
TXDATA[7:0] (last bit transmitted is TXDATA[0])

Disparity Control

The 8B/10B encoder is initialized with a negative running disparity. Unique control allows forcing the current running disparity state.

TXRUNDISP signals its current running disparity. This may be useful in those cases where there is a need to manipulate the initial running disparity value.

Bits TXCHARDISPMODE and TXCHARDISPVAL control the generation of running disparity before each byte.

For example, the transceiver can generate the sequence

```
K28.5+ K28.5+ K28.5- K28.5-
```

or

```
K28.5- K28.5- K28.5+ K28.5+
```

by specifying inverted running disparity for the second and fourth bytes.

Transmit FIFO

Proper operation of the circuit is only possible if the FPGA clock (TXUSRCLK) is frequency-locked to the reference clock (REFCLK). Phase variations up to one clock cycle are allowable. The FIFO has a depth of four. Overflow or underflow conditions are detected and signaled at the interface. Bypassing of this FIFO is programmable.

8B/10B Encoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

A bypassable 8B/10B encoder is included. The encoder uses the same 256 data characters and 12 control characters used by Gigabit Ethernet, Fibre Channel, and InfiniBand.

The encoder accepts 8 bits of data along with a K-character signal for a total of 9 bits per character applied, and generates a 10 bit character for transmission. If the K-character signal is High, the data is encoded into one of the twelve possible K-characters available in the 8B/10B code. If the K-character input is Low, the 8 bits are encoded as standard data. If the K-character input is High, and a user applies other than one of the twelve possible combinations, TXKERR indicates the error.

8B/10B Decoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

An optional 8B/10B decoder is included. A programmable option allows the decoder to be bypassed. When the 8B/10B decoder is bypassed, the 10-bit character order is, for example,

RXCHARISK[0] (first bit received)
RXRUNDISP[0]
RXDATA[7:0] (last bit received is RXDATA[0])

The decoder uses the same table that is used for Gigabit Ethernet, Fibre Channel, and InfiniBand. In addition to decoding all data and K-characters, the decoder has several extra features. The decoder separately detects both “disparity errors” and “out-of-band” errors. A disparity error is the reception of 10-bit character that exists within the 8B/10B table but has an incorrect disparity. An out-of-band error is the reception of a 10-bit character that does not exist within the 8B/10B table. It is possible to obtain an out-of-band error without having a disparity error. The proper disparity is always computed for both legal and illegal characters. The current running disparity is available at the RXRUNDISP signal.

The 8B/10B decoder performs a unique operation if out-of-band data is detected. If out-of-band data is detected, the decoder signals the error and passes the illegal 10-bits through and places them on the outputs. This can be used for debugging purposes if desired.

The decoder also signals the reception of one of the 12 valid K-characters. In addition, a programmable comma detect is included. The comma detect signal registers a comma on the receipt of any comma+, comma–, or both. Since the comma is defined as a 7-bit character, this includes several out-of-band characters. Another option allows the decoder to detect only the three defined commas (K28.1, K28.5, and K28.7) as comma+, comma–, or both. In total, there are six possible options, three for valid commas and three for "any comma."

Note that all bytes (1, 2, or 4) at the RX FPGA interface each have their own individual 8B/10B indicators (K-character, disparity error, out-of-band error, current running disparity, and comma detect).

Functional Description: Processor Block

This section briefly describes the interfaces and components of the Processor Block. The subsequent section, Functional Description: Embedded PowerPC 405 Core beginning on page 20, offers a summary of major PPC405 core features. For an in-depth discussion on both the Processor Block and PPC405, see tthe **PowerPC Processor Reference Guide** and the **PowerPC 405 Processor Block Reference Guide** available on the Xilinx website at **http://www.xilinx.com**.

Processor Block Overview

Figure 14 shows the internal architecture of the Processor Block.

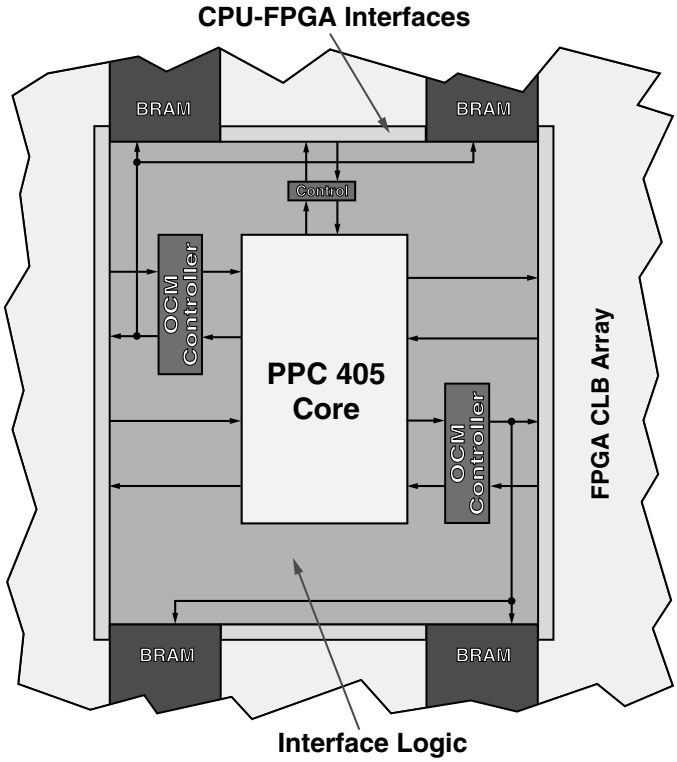


Figure 14: **Processor Block Architecture**

Within the Virtex-II Pro Processor Block, there are four components:

- Embedded IBM PowerPC 405-D5 RISC CPU core
- On-Chip Memory (OCM) controllers and interfaces
- Clock/control interface logic
- CPU-FPGA Interfaces

Embedded PowerPC 405 RISC Core

The PowerPC 405D5 core is a 0.13 µm implementation of the IBM PowerPC 405D4 core. The advanced process technology enables the embedded PowerPC 405 (PPC405) core to operate at 300+ MHz while maintaining low power consumption. Specially designed interface logic integrates the core with the surrounding CLBs, block RAMs, and general routing resources. Up to four Processor Blocks can be available in a single Virtex-II Pro device.

The embedded PPC405 core implements the PowerPC User Instruction Set Architecture (UISA), user-level registers, programming model, data types, and addressing modes for 32-bit fixed-point operations. 64-bit operations, auxiliary processor operations, and floating-point operations are trapped and can be emulated in software.

Most of the PPC405 core features are compatible with the specifications for the PowerPC Virtual Environment Architecture (VEA) and Operating Environment Architecture (OEA). They also provide a number of optimizations and extensions to the lower layers of the PowerPC Architecture. The full architecture of the PPC405 is defined by the PowerPC Embedded Environment and PowerPC UISA documentation, available from IBM.

On-Chip Memory (OCM) Controllers

Introduction

The OCM controllers serve as dedicated interfaces between the block RAMs in the FPGA fabric (see 18 Kb Block SelectRAM+ Resources, page 44) and OCM signals available on the embedded PPC405 core. The OCM signals on the PPC405 core are designed to provide very quick access to a fixed amount of instruction and data memory space. The OCM controller provides an interface to both the 64-bit Instruction-Side Block RAM (ISBRAM) and the 32-bit Data-Side Block RAM (DSBRAM). The designer can choose to implement:

- ISBRAM only
- DSBRAM only
- Both ISBRAM and DSBRAM
- No ISBRAM and no DSBRAM

One of OCM's primary advantages is that it guarantees a fixed latency of execution for a higher level of determinism. Additionally, it reduces cache pollution and thrashing, since the cache remains available for caching code from other memory resources.

Typical applications for DSOCM include scratch-pad memory, as well as use of the dual-port feature of block RAM to enable bidirectional data transfer between processor and FPGA. Typical applications for ISOCM include storage of interrupt service routines.

Functional Features

Common Features

- Separate Instruction and Data memory interface between processor core and BRAMs in FPGA
- Dedicated interface to Device Control Register (DCR) bus for ISOCM and DSOCM

CLB/Slice Configurations

Table 19 summarizes the logic resources in one CLB. All of the CLBs are identical and each CLB or slice can be implemented in one of the configurations listed. Table 20 shows the available resources in all CLBs.

Table 19: **Logic Resources in One CLB**

Slices	LUTs	Flip-Flops	MULT_ANDs	Arithmetic & Carry-Chains	SOP Chains	Distributed SelectRAM+	Shift Registers	TBUF
4	8	8	8	2	2	128 bits	128 bits	2

Table 20: **Virtex-II Pro Logic Resources Available in All CLBs**

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry-Chains(1)	Number of SOP Chains(1)
XC2VP2	16 x 22	1,408	2,816	45,056	2,816	44	32
XC2VP4	40 x 22	3,008	6,016	96,256	6,016	44	80
XC2VP7	40 x 34	4,928	9,856	157,696	9,856	68	80
XC2VP20	56 x 46	9,280	18,560	296,960	18,560	92	112
XC2VPX20	56 x 46	9,792	19,584	313,334	18,560	92	112
XC2VP30	80 x 46	13,696	27,392	438,272	27,392	92	160
XC2VP40	88 x 58	19,392	38,784	620,544	38,784	116	176
XC2VP50	88 x 70	23,616	47,232	755,712	47,232	140	176
XC2VP70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VPX70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VP100	120 x 94	44,096	88,192	1,411,072	88,192	188	240

Notes:
1. The carry-chains and SOP chains can be split or cascaded.

18 Kb Block SelectRAM+ Resources

Introduction

Virtex-II Pro devices incorporate large amounts of 18 Kb block SelectRAM+ resources. These complement the distributed SelectRAM+ resources that provide shallow RAM structures implemented in CLBs. Each Virtex-II Pro block SelectRAM+ resource is an 18 Kb true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical. CLK, EN, WE, and SSR polarities are defined through configuration.

Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for write) and Data/parity data outputs (for read).

Operation is synchronous; the block SelectRAM+ behaves like a register. Control, address and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, a configuration option) clock edge. Data outputs change as a result of the same clock edge.

Configuration

Virtex-II Pro block SelectRAM+ supports various configurations, including single- and dual-port RAM and various data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 21.

Table 21: **Dual- and Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

Single-Port Configuration

As a single-port RAM, the block SelectRAM+ has access to the 18 Kb memory locations in any of the 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations and to 16 Kb memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of the 9-bit, 18-bit and 36-bit widths is the ability to store a parity bit for each eight bits. Parity bits must be generated or checked exter-

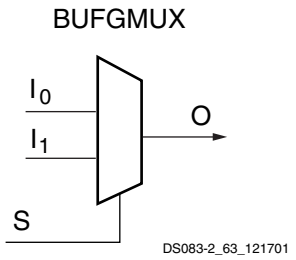


Figure 60: **Virtex-II Pro BUFGMUX Function**

If the presently selected clock is Low while S changes, or if it goes Low after S has changed, the output is kept Low until the other ("to-be-selected") clock has made a transition from High to Low. At that instant, the new clock starts driving the output.

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

All Virtex-II Pro devices have 16 global clock multiplexer buffers.

Figure 61 shows a switchover from I0 to I1.

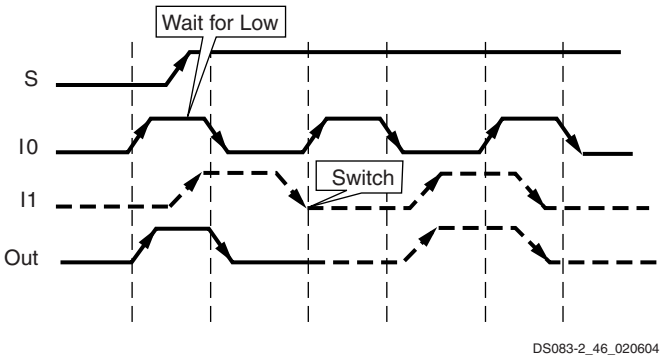


Figure 61: **Clock Multiplexer Waveform Diagram**

- The current clock is CLK0.
- S is activated High.
- If CLK0 is currently High, the multiplexer waits for CLK0 to go Low.
- Once CLK0 is Low, the multiplexer output stays Low until CLK1 transitions High to Low.
- When CLK1 transitions from High to Low, the output switches to CLK1.
- No glitches or short pulses can appear on the output.

Local Clocking

In addition to global clocks, there are local clock resources in the Virtex-II Pro devices. There are more than 72 local clocks in the Virtex-II Pro family. These resources can be used for many different applications, including but not limited to memory interfaces. For example, even using only the left and right I/O banks, Virtex-II Pro FPGAs can support up to 50 local clocks for DDR SDRAM. These interfaces can operate beyond 200 MHz on Virtex-II Pro devices.

Digital Clock Manager (DCM)

The Virtex-II Pro DCM offers a wide range of powerful clock management features.

- **Clock De-skew**: The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock, thus eliminating clock distribution delays.
- **Frequency Synthesis**: The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting**: The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four of the nine DCM clock outputs can drive inputs to global clock buffers or global clock multiplexer buffers simultaneously (see Figure 62). All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers.

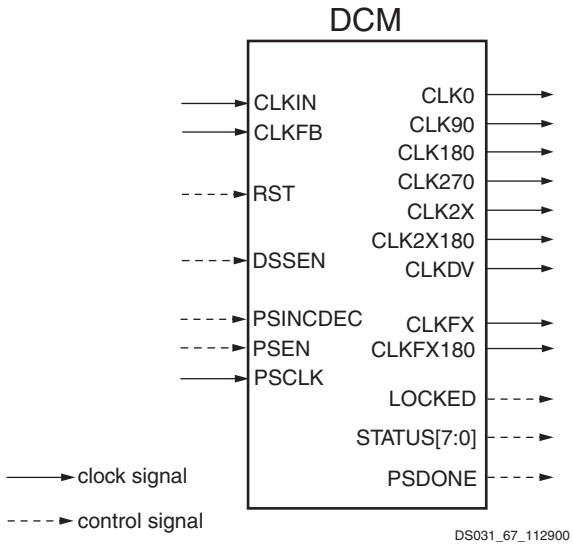


Figure 62: **Digital Clock Manager**

The DCM can be configured to delay the completion of the Virtex-II Pro configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

Table 46: **Pipelined Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Setup and Hold Times Before/After Clock					
Data Inputs	$T_{MULIDCK}/T_{MULCKID}$	1.86/ 0.00	2.06/ 0.00	2.31/ 0.00	ns, max
Clock Enable	$T_{MULIDCK\_CE}/T_{MULCKID\_CE}$	0.23/ 0.00	0.25/ 0.00	0.28/ 0.00	ns, max
Reset	$T_{MULIDCK\_RST}/T_{MULCKID\_RST}$	0.21/–0.09	0.24/–0.09	0.26/–0.10	ns, max
Clock to Output Pin					
Clock to Pin35	T_{MULTCK_P35}	2.45	2.92	3.27	ns, max
Clock to Pin34	T_{MULTCK_P34}	2.36	2.82	3.16	ns, max
Clock to Pin33	T_{MULTCK_P33}	2.28	2.72	3.05	ns, max
Clock to Pin32	T_{MULTCK_P32}	2.20	2.62	2.93	ns, max
Clock to Pin31	T_{MULTCK_P31}	2.12	2.52	2.82	ns, max
Clock to Pin30	T_{MULTCK_P30}	2.03	2.42	2.71	ns, max
Clock to Pin29	T_{MULTCK_P29}	1.95	2.32	2.60	ns, max
Clock to Pin28	T_{MULTCK_P28}	1.87	2.22	2.48	ns, max
Clock to Pin27	T_{MULTCK_P27}	1.79	2.12	2.37	ns, max
Clock to Pin26	T_{MULTCK_P26}	1.70	2.02	2.26	ns, max
Clock to Pin25	T_{MULTCK_P25}	1.62	1.92	2.15	ns, max
Clock to Pin24	T_{MULTCK_P24}	1.54	1.82	2.03	ns, max
Clock to Pin23	T_{MULTCK_P23}	1.46	1.71	1.92	ns, max
Clock to Pin22	T_{MULTCK_P22}	1.37	1.61	1.81	ns, max
Clock to Pin21	T_{MULTCK_P21}	1.29	1.51	1.69	ns, max
Clock to Pin20	T_{MULTCK_P20}	1.21	1.41	1.58	ns, max
Clock to Pin19	T_{MULTCK_P19}	1.13	1.31	1.47	ns, max
Clock to Pin18	T_{MULTCK_P18}	1.04	1.21	1.36	ns, max
Clock to Pin17	T_{MULTCK_P17}	0.96	1.11	1.24	ns, max
Clock to Pin16	T_{MULTCK_P16}	0.88	1.01	1.13	ns, max
Clock to Pin15	T_{MULTCK_P15}	0.80	0.91	1.02	ns, max
Clock to Pin14	T_{MULTCK_P14}	0.71	0.81	0.91	ns, max
Clock to Pin13	T_{MULTCK_P13}	0.63	0.71	0.79	ns, max
Clock to Pin12	T_{MULTCK_P12}	0.63	0.71	0.79	ns, max
Clock to Pin11	T_{MULTCK_P11}	0.63	0.71	0.79	ns, max
Clock to Pin10	T_{MULTCK_P10}	0.63	0.71	0.79	ns, max
Clock to Pin9	T_{MULTCK_P9}	0.63	0.71	0.79	ns, max
Clock to Pin8	T_{MULTCK_P8}	0.63	0.71	0.79	ns, max
Clock to Pin7	T_{MULTCK_P7}	0.63	0.71	0.79	ns, max
Clock to Pin6	T_{MULTCK_P6}	0.63	0.71	0.79	ns, max
Clock to Pin5	T_{MULTCK_P5}	0.63	0.71	0.79	ns, max
Clock to Pin4	T_{MULTCK_P4}	0.63	0.71	0.79	ns, max
Clock to Pin3	T_{MULTCK_P3}	0.63	0.71	0.79	ns, max
Clock to Pin2	T_{MULTCK_P2}	0.63	0.71	0.79	ns, max
Clock to Pin1	T_{MULTCK_P1}	0.63	0.71	0.79	ns, max
Clock to Pin0	T_{MULTCK_P0}	0.63	0.71	0.79	ns, max

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-II Pro source-synchronous transmitter and receiver data-valid windows.

Table 64: **Duty Cycle Distortion and Clock-Tree Skew**

Description	Symbol	Device	Speed Grade			Units
			–7	–6	–5	
Duty Cycle Distortion(1)	T_{DCD_LOCAL}	All	0.10	0.10	0.20	ns
	T_{DCD_CLK180}		0.10	0.11	0.13	ns
Clock Tree Skew(2)	T_{CKSKEW}	XC2VP2	0.13	0.13	0.13	ns
		XC2VP4	0.13	0.13	0.13	ns
		XC2VP7	0.13	0.13	0.13	ns
		XC2VP20	0.20	0.21	0.22	ns
		XC2VPX20	0.20	0.21	0.22	ns
		XC2VP30	0.20	0.22	0.24	ns
		XC2VP40	0.33	0.34	0.35	ns
		XC2VP50	0.40	0.41	0.42	ns
		XC2VP70	0.54	0.59	0.64	ns
		XC2VPX70	0.54	0.59	0.64	ns
		XC2VP100	N/A	0.79	0.87	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.

   T_{DCD_LOCAL} applies to cases where the dedicated path from the DCM to the BUFG is bypassed and where local (IOB) inversion is used to provide the negative-edge clock to the DDR element in the I/O. Users must follow the implementation guidelines contained in **XAPP685** for these specifications to apply.

   T_{DCD_CLK180} applies to cases where the CLK180 output of the DCM is used to provide the negative-edge clock to the DDR element in the I/O.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
3	IO_L05P_3	L13
3	IO_L03N_3/VREF_3	L12
3	IO_L03P_3	M13
3	IO_L02N_3	M16
3	IO_L02P_3	N16
3	IO_L01N_3/VRP_3	M15
3	IO_L01P_3/VRN_3	M14
4	IO_L01N_4/BUSY/DOUT(1)	P15
4	IO_L01P_4/INIT_B	P14
4	IO_L02N_4/D0/DIN(1)	R14
4	IO_L02P_4/D1	P13
4	IO_L03N_4/D2	T15
4	IO_L03P_4/D3	T14
4	IO_L06N_4/VRP_4	N12
4	IO_L06P_4/VRN_4	P12
4	IO_L07P_4/VREF_4	N11
4	IO_L09N_4	M11
4	IO_L09P_4/VREF_4	M10
4	IO_L69N_4	N10
4	IO_L69P_4/VREF_4	P10
4	IO_L74N_4/GCLK3S	N9
4	IO_L74P_4/GCLK2P	P9
4	IO_L75N_4/GCLK1S	R9
4	IO_L75P_4/GCLK0P	T9
5	IO_L75N_5/GCLK7S	T8
5	IO_L75P_5/GCLK6P	R8
5	IO_L74N_5/GCLK5S	P8
5	IO_L74P_5/GCLK4P	N8
5	IO_L69N_5/VREF_5	P7
5	IO_L69P_5	N7
5	IO_L09N_5/VREF_5	M7
5	IO_L09P_5	M6
5	IO_L07N_5/VREF_5	N6

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
7	VCCO_7	G6
N/A	CCLK	N15
N/A	PROG_B	D1
N/A	DONE	P16
N/A	M0	N3
N/A	M1	N2
N/A	M2	P1
N/A	TCK	D16
N/A	TDI	E1
N/A	TDO	E16
N/A	TMS	C16
N/A	PWRDWN_B	N14
N/A	HSWAP_EN	C1
N/A	RSVD	D14
N/A	VBATT	D15
N/A	DXP	D2
N/A	DXN	D3
N/A	AVCCAUXTX6	B5
N/A	VTTXPAD6	B4
N/A	TXNPAD6	A4
N/A	TXPPAD6	A5
N/A	GNDA6	C6
N/A	RXPPAD6	A6
N/A	RXNPAD6	A7
N/A	VTRXPAD6	B6
N/A	AVCCAUXRX6	B7
N/A	AVCCAUXTX7	B11
N/A	VTTXPAD7	B10
N/A	TXNPAD7	A10
N/A	TXPPAD7	A11
N/A	GNDA7	C11
N/A	RXPPAD7	A12
N/A	RXNPAD7	A13
N/A	VTRXPAD7	B12

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
5	IO_L46N_5	W11			
5	IO_L46P_5	W10			
5	IO_L45N_5/VREF_5	AD9			
5	IO_L45P_5	AC9			
5	IO_L43N_5	AB9			
5	IO_L43P_5	AA9			
5	IO_L39N_5	Y9			
5	IO_L39P_5	W9			
5	IO_L37N_5	AF8			
5	IO_L37P_5	AE8			
5	IO_L09N_5/VREF_5	AB8			
5	IO_L09P_5	AA8			
5	IO_L07N_5/VREF_5	Y8			
5	IO_L07P_5	W8			
5	IO_L06N_5/VRP_5	AD7			
5	IO_L06P_5/VRN_5	AC7			
5	IO_L05_5/No_Pair	AB7			
5	IO_L03N_5/D4	AA7			
5	IO_L03P_5/D5	Y7			
5	IO_L02N_5/D6	AC6			
5	IO_L02P_5/D7	AB6			
5	IO_L01N_5/RDWR_B	AC5			
5	IO_L01P_5/CS_B	AB5			
6	IO_L01P_6/VRN_6	AE1			
6	IO_L01N_6/VRP_6	AD1			
6	IO_L02P_6	AD2			
6	IO_L02N_6	AC3			
6	IO_L03P_6	AC2			
6	IO_L03N_6/VREF_6	AC1			
6	IO_L05P_6	AB4			
6	IO_L05N_6	AA5			
6	IO_L06P_6	AB2			
6	IO_L06N_6	AB1			
6	IO_L23P_6	AA6	NC		

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	RSVD	C23			
N/A	VBATT	A24			
N/A	TMS	B24			
N/A	TCK	B26			
N/A	TDO	D24			
N/A	CCLK	AE24			
N/A	PWRDWN_B	AF24			
N/A	DONE	AD23			
N/A	AVCCAUXRX16	AE23			
N/A	VTRXPAD16	AE22			
N/A	RXNPAD16	AF23			
N/A	RXPPAD16	AF22			
N/A	GNDA16	AD21			
N/A	TXPPAD16	AF21			
N/A	TXNPAD16	AF20			
N/A	VTTXPAD16	AE20			
N/A	AVCCAUXTX16	AE21			
N/A	AVCCAUXRX18	AE18			
N/A	VTRXPAD18	AE17			
N/A	RXNPAD18	AF18			
N/A	RXPPAD18	AF17			
N/A	GNDA18	AD16			
N/A	TXPPAD18	AF16			
N/A	TXNPAD18	AF15			
N/A	VTTXPAD18	AE15			
N/A	AVCCAUXTX18	AE16			
N/A	AVCCAUXRX19	AE12			
N/A	VTRXPAD19	AE11			
N/A	RXNPAD19	AF12			
N/A	RXPPAD19	AF11			
N/A	GNDA19	AD11			
N/A	TXPPAD19	AF10			
N/A	TXNPAD19	AF9			
N/A	VTTXPAD19	AE9			
N/A	AVCCAUXTX19	AE10			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
7	IO_L86N_7	U25				
7	IO_L85P_7	T32				
7	IO_L85N_7	T31				
7	IO_L60P_7	T30				
7	IO_L60N_7	T29				
7	IO_L59P_7	T28				
7	IO_L59N_7	T27				
7	IO_L58P_7	T33				
7	IO_L58N_7/VREF_7	R33				
7	IO_L57P_7	R32				
7	IO_L57N_7	R31				
7	IO_L56P_7	T26				
7	IO_L56N_7	T25				
7	IO_L55P_7	R34				
7	IO_L55N_7	P34				
7	IO_L54P_7	R29				
7	IO_L54N_7	R28				
7	IO_L53P_7	U24				
7	IO_L53N_7	T24				
7	IO_L52P_7	P32				
7	IO_L52N_7/VREF_7	P31				
7	IO_L51P_7	P30				
7	IO_L51N_7	P29				
7	IO_L50P_7	R26				
7	IO_L50N_7	R25				
7	IO_L49P_7	P33				
7	IO_L49N_7	N33				
7	IO_L48P_7	N32				
7	IO_L48N_7	N31				
7	IO_L47P_7	P28				
7	IO_L47N_7	P27				
7	IO_L46P_7	N34				
7	IO_L46N_7/VREF_7	M34				
7	IO_L45P_7	N30				
7	IO_L45N_7	N29				
7	IO_L44P_7	P26				
7	IO_L44N_7	P25				
7	IO_L43P_7	M32				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	VTTXPAD21	AN29				
N/A	AVCCAUXTX21	AN28				
N/A	AVCCAUXRX23	AN30	NC	NC		
N/A	VTRXPAD23	AN31	NC	NC		
N/A	RXNPAD23	AP30	NC	NC		
N/A	RXPPAD23	AP31	NC	NC		
N/A	GNDA23	AM30	NC	NC		
N/A	TXPPAD23	AP32	NC	NC		
N/A	TXNPAD23	AP33	NC	NC		
N/A	VTTXPAD23	AN33	NC	NC		
N/A	AVCCAUXTX23	AN32	NC	NC		
N/A	VCCINT	L11				
N/A	VCCINT	L24				
N/A	VCCINT	M12				
N/A	VCCINT	M23				
N/A	VCCINT	N13				
N/A	VCCINT	N14				
N/A	VCCINT	N15				
N/A	VCCINT	N16				
N/A	VCCINT	N17				
N/A	VCCINT	N18				
N/A	VCCINT	N19				
N/A	VCCINT	N20				
N/A	VCCINT	N21				
N/A	VCCINT	N22				
N/A	VCCINT	P13				
N/A	VCCINT	P22				
N/A	VCCINT	R13				
N/A	VCCINT	R22				
N/A	VCCINT	T13				
N/A	VCCINT	T22				
N/A	VCCINT	U13				
N/A	VCCINT	U22				
N/A	VCCINT	V13				
N/A	VCCINT	V22				
N/A	VCCINT	W13				
N/A	VCCINT	W22				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	V19				
N/A	GND	V20				
N/A	GND	V21				
N/A	GND	W1				
N/A	GND	W14				
N/A	GND	W15				
N/A	GND	W16				
N/A	GND	W17				
N/A	GND	W18				
N/A	GND	W19				
N/A	GND	W20				
N/A	GND	W21				
N/A	GND	W34				
N/A	GND	Y8				
N/A	GND	Y14				
N/A	GND	Y15				
N/A	GND	Y16				
N/A	GND	Y17				
N/A	GND	Y18				
N/A	GND	Y19				
N/A	GND	Y20				
N/A	GND	Y21				
N/A	GND	Y27				
N/A	GND	AA14				
N/A	GND	AA15				
N/A	GND	AA16				
N/A	GND	AA17				
N/A	GND	AA18				
N/A	GND	AA19				
N/A	GND	AA20				
N/A	GND	AA21				
N/A	GND	AC5				
N/A	GND	AC8				
N/A	GND	AC27				
N/A	GND	AC30				
N/A	GND	AE3				
N/A	GND	AE32				
N/A	GND	H23				

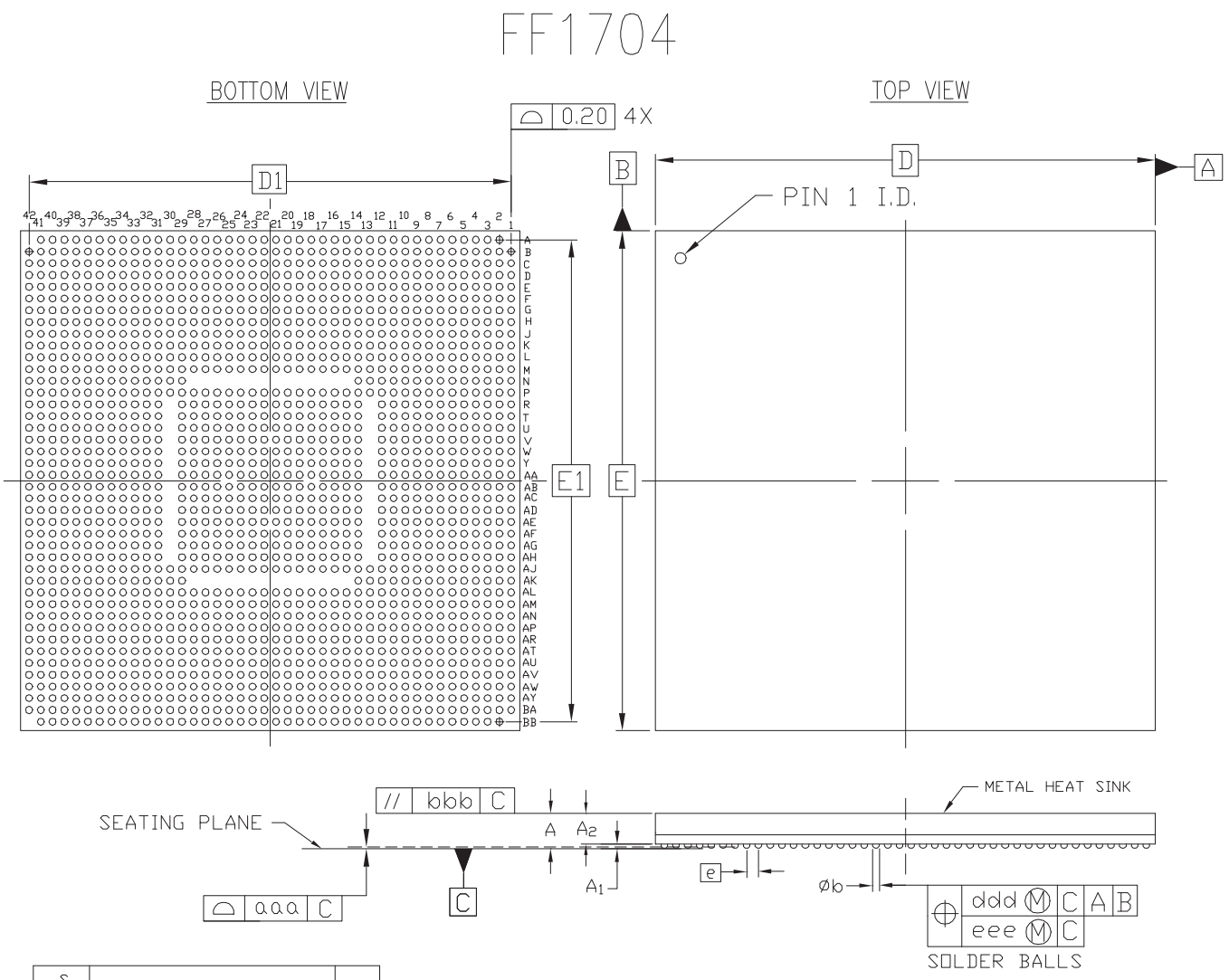
Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	VCCAUX	AP6		
N/A	VCCAUX	F6		
N/A	VCCAUX	AR5		
N/A	VCCAUX	E5		
N/A	VCCAUX	AW2		
N/A	VCCAUX	Y2		
N/A	VCCAUX	A2		
N/A	VCCAUX	AV1		
N/A	VCCAUX	AA1		
N/A	VCCAUX	Y1		
N/A	VCCAUX	W1		
N/A	VCCAUX	B1		
N/A	GND	A3		
N/A	GND	AV2		
N/A	GND	AU2		
N/A	GND	AA2		
N/A	GND	W2		
N/A	GND	C2		
N/A	GND	B2		
N/A	GND	AU1		
N/A	GND	AM1		
N/A	GND	AH1		
N/A	GND	AD1		
N/A	GND	T1		
N/A	GND	M1		
N/A	GND	H1		
N/A	GND	C1		
N/A	GND	AD5		
N/A	GND	T5		
N/A	GND	M5		
N/A	GND	H5		
N/A	GND	AU4		
N/A	GND	AT4		
N/A	GND	D4		
N/A	GND	C4		
N/A	GND	AW3		
N/A	GND	AV3		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	RXPPAD17		BB15		
N/A	GNDA17		AY16		
N/A	TXPPAD17		BB16		
N/A	TXNPAD17		BB17		
N/A	VTTXPAD17		BA17		
N/A	AVCCAUXTX17		BA16		
N/A	AVCCAUXRX18		BA18		
N/A	VTRXPAD18		BA19		
N/A	RXNPAD18		BB18		
N/A	RXPPAD18		BB19		
N/A	GNDA18		AY21		
N/A	TXPPAD18		BB20		
N/A	TXNPAD18		BB21		
N/A	VTTXPAD18		BA21		
N/A	AVCCAUXTX18		BA20		
N/A	AVCCAUXRX19		BA22		
N/A	VTRXPAD19		BA23		
N/A	RXNPAD19		BB22		
N/A	RXPPAD19		BB23		
N/A	GNDA19		AY22		
N/A	TXPPAD19		BB24		
N/A	TXNPAD19		BB25		
N/A	VTTXPAD19		BA25		
N/A	AVCCAUXTX19		BA24		
N/A	AVCCAUXRX20		BA26		
N/A	VTRXPAD20		BA27		
N/A	RXNPAD20		BB26		
N/A	RXPPAD20		BB27		
N/A	GNDA20		AY27		
N/A	TXPPAD20		BB28		
N/A	TXNPAD20		BB29		
N/A	VTTXPAD20		BA29		
N/A	AVCCAUXTX20		BA28		
N/A	AVCCAUXRX21		BA30		
N/A	VTRXPAD21		BA31		
N/A	RXNPAD21		BB30		

FF1704 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.45	
A_1	0.40	0.50	0.60	
A_2			2.85	
D/E	42.50 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M		42		2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAV-1 (DEPOPULATED)

Figure 9: **FF1704 Flip-Chip Fine-Pitch BGA Package Specifications**

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L22N_2/VREF_2	L4	
2	IO_L22P_2	L5	
2	IO_L23N_2	T8	
2	IO_L23P_2	T9	
2	IO_L24N_2	L3	
2	IO_L24P_2	K3	
2	IO_L25N_2	L1	
2	IO_L25P_2	L2	
2	IO_L26N_2	U12	
2	IO_L26P_2	V12	
2	IO_L27N_2	M7	
2	IO_L27P_2	L6	
2	IO_L28N_2/VREF_2	M5	
2	IO_L28P_2	M6	
2	IO_L29N_2	U10	
2	IO_L29P_2	U11	
2	IO_L30N_2	M3	
2	IO_L30P_2	M4	
2	IO_L31N_2	N6	
2	IO_L31P_2	N7	
2	IO_L32N_2	U7	
2	IO_L32P_2	U8	
2	IO_L33N_2	N3	
2	IO_L33P_2	N4	
2	IO_L34N_2/VREF_2	N2	
2	IO_L34P_2	M2	
2	IO_L35N_2	V10	
2	IO_L35P_2	V11	
2	IO_L36N_2	P6	
2	IO_L36P_2	P7	
2	IO_L37N_2	P1	
2	IO_L37P_2	P2	
2	IO_L38N_2	V8	
2	IO_L38P_2	V9	
2	IO_L39N_2	R6	
2	IO_L39P_2	P5	
2	IO_L40N_2/VREF_2	R4	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L56N_3	AC11	
3	IO_L56P_3	AC12	
3	IO_L55N_3	AD3	
3	IO_L55P_3	AE3	
3	IO_L54N_3	AE1	
3	IO_L54P_3	AE2	
3	IO_L53N_3	AC6	
3	IO_L53P_3	AC7	
3	IO_L52N_3	AF2	
3	IO_L52P_3	AF3	
3	IO_L51N_3/VREF_3	AF6	
3	IO_L51P_3	AG6	
3	IO_L50N_3	AD10	
3	IO_L50P_3	AD11	
3	IO_L49N_3	AG4	
3	IO_L49P_3	AG5	
3	IO_L48N_3	AF4	
3	IO_L48P_3	AG3	
3	IO_L47N_3	AC10	
3	IO_L47P_3	AD9	
3	IO_L46N_3	AG1	
3	IO_L46P_3	AG2	
3	IO_L45N_3/VREF_3	AG7	
3	IO_L45P_3	AH7	
3	IO_L44N_3	AC8	
3	IO_L44P_3	AD7	
3	IO_L43N_3	AH4	
3	IO_L43P_3	AH5	
3	IO_L42N_3	AH1	
3	IO_L42P_3	AH2	
3	IO_L41N_3	AE10	
3	IO_L41P_3	AE11	
3	IO_L40N_3	AJ6	
3	IO_L40P_3	AJ7	
3	IO_L39N_3/VREF_3	AH6	
3	IO_L39P_3	AJ5	
3	IO_L38N_3	AE8	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCAUX	A2	
N/A	VCCAUX	BA1	
N/A	VCCAUX	AY1	
N/A	VCCAUX	AL1	
N/A	VCCAUX	AB1	
N/A	VCCAUX	AA1	
N/A	VCCAUX	M1	
N/A	VCCAUX	C1	
N/A	VCCAUX	B1	
N/A	GND	AV42	
N/A	GND	AP42	
N/A	GND	AK42	
N/A	GND	AF42	
N/A	GND	AC42	
N/A	GND	Y42	
N/A	GND	U42	
N/A	GND	N42	
N/A	GND	J42	
N/A	GND	E42	
N/A	GND	BA41	
N/A	GND	AY41	
N/A	GND	C41	
N/A	GND	B41	
N/A	GND	BA40	
N/A	GND	B40	
N/A	GND	BB38	
N/A	GND	AV38	
N/A	GND	AP38	
N/A	GND	AK38	
N/A	GND	AF38	
N/A	GND	AC38	
N/A	GND	Y38	
N/A	GND	U38	
N/A	GND	N38	
N/A	GND	J38	
N/A	GND	E38	
N/A	GND	A38	