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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	352
Number of Logic Elements/Cells	3168
Total RAM Bits	221184
Number of I/O	140
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp2-5fg256i

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/13/02	2.0	New Virtex-II Pro family members. New timing parameters per speedsfile **v1.62**.
09/03/02	2.1	Updates to Table 1 and Table 3. Processor Block information added to Table 4.
09/27/02	2.2	In Table 1, correct max number of XC2VP30 I/Os to 644.
11/20/02	2.3	Add bullet items for 3.3V I/O features.
01/20/03	2.4	• In Table 3, add FG676 package option for XC2VP20, XC2VP30, and XC2VP40. • Remove FF1517 package option for XC2VP40.
03/24/03	2.4.1	• Correct number of single-ended I/O standards from 19 to 22. • Correct minimum RocketIO serial speed from 622 Mbps to 600 Mbps.
08/25/03	2.4.2	• Add footnote referring to XAPP659 to callout for 3.3V I/O standards on page 4.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Table 1: Corrected number of RocketIO transceiver blocks for XC2VP40. • Section Virtex-II Pro Platform FPGA Technology (All Devices): Updated number of differential standards supported from six to ten. • Section Input/Output Blocks (IOBs): Added text stating that differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards. • Figure 1: Added note stating that -7 devices are not available in Industrial grade.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/30/04	4.0	Merged in DS110-1 (Module 1 of Virtex-II Pro X data sheet). Added information on available Pb-free packages.
11/17/04	4.1	*No changes in Module 1 for this revision.*
03/01/05	4.2	Table 3: Corrected number of RocketIO transceivers for XC2VP7-FG456.
06/20/05	4.3	*No changes in Module 1 for this revision.*
09/15/05	4.4	• Changed all instances of 10.3125 Gb/s (RocketIO transceiver maximum bit rate) to 6.25 Gb/s. • Changed all instances of 412.5 Gb/s (RocketIO X transceiver maximum multi-channel raw data transfer rate) to 250 Gb/s.
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s. • Changed maximum performance for -7 Virtex-II Pro X MGT (Table 4) to N/A.
03/05/07	4.6	*No changes in Module 1 for this revision.*
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner.

Other RocketIO X Features and Notes

Loopback

In order to facilitate testing without having the need to either apply patterns or measure data at GHz rates, four programmable loop-back features are available.

The first option, serial loopback, is available in two modes: *pre-driver* and *post-driver*.

- The pre-driver mode loops back to the receiver without going through the output driver. In this mode, TXP and TXN are not driven and therefore need not be terminated.
- The post-driver mode is the same as the RocketIO loopback. In this mode, TXP and TXN are driven and must be properly terminated.

The third option, parallel loopback, checks the digital circuitry. When parallel loopback is enabled, the serial loopback path is disabled. However, the transmitter outputs remain active, and data can be transmitted. If TXINHIBIT is asserted, TXP is forced to 0 until TXINHIBIT is de-asserted.

The fourth option, repeater loopback, allows received data to be transmitted without going through the FPGA fabric.

Reset

The receiver and transmitter have their own synchronous reset inputs. The transmitter reset, TXRESET, recenters the transmission FIFO and resets all transmitter registers and the encoder. The receiver reset, RXRESET, recenters the receiver elastic buffer and resets all receiver registers and the decoder. When the signals TXRESET or RXRESET are asserted High, the PCS is in reset. After TXRESET or RXRESET are deasserted, the PCS takes five clocks to come out of reset for each clock domain.

The PMA configuration vector is not affected during this reset, so the PMA speed, filter settings, and so on, all remain the same. Also, the PMA internal pipeline is not affected and continues to operate in normal fashion.

Power

The transceiver voltage regulator circuits must not be shared with any other supplies (including FPGA supplies V_{CCINT}, V_{CCO}, V_{CCAUX}, and V_{REF}). Voltage regulators can be shared among transceiver power supplies of the same voltage, but each supply pin must still have its own separate passive filtering network.

All RocketIO transceivers in the FPGA, whether instantiated in the design or not, must be connected to power and ground. Unused transceivers can be powered by any 1.5V or 2.5V source, and passive filtering is not required.

The Power Down feature is controlled by the transceiver's POWERDOWN input pin. Any given transceiver that is not instantiated in the design is automatically set to the POWERDOWN state by the Xilinx ISE development software. The Power Down pin on the FPGA package has no effect on the MGT.

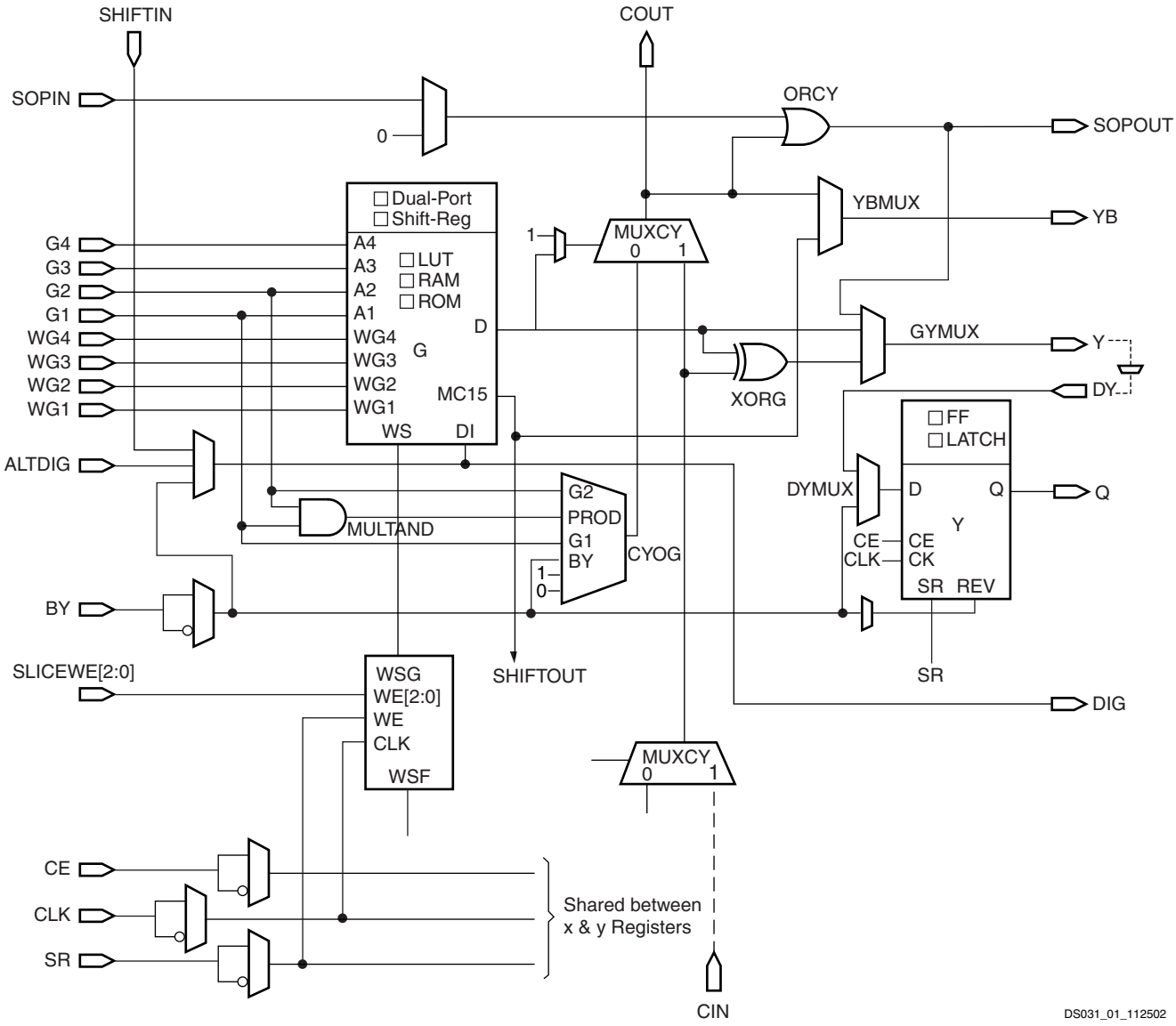


Figure 34: **Virtex-II Pro Slice (Top Half)**

3. NO_CHANGE

The NO_CHANGE option maintains the content of the output registers, regardless of the write operation. The clock edge during the write mode has no effect on the content of the data output register DO. When the port is configured as NO_CHANGE, only a read operation loads a new value in the output register DO, as shown in Figure 51.

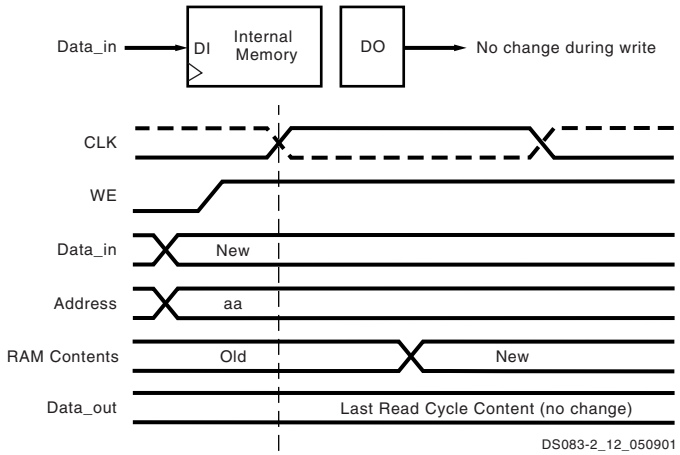


Figure 51: **NO_CHANGE Mode**

Control Pins and Attributes

Virtex-II Pro SelectRAM+ memory has two independent ports with the control signals described in Table 24. All control inputs including the clock have an optional inversion.

Table 24: **Control Functions**

Control Signal	Function
CLK	Read and Write Clock
EN	Enable affects Read, Write, Set, Reset
WE	Write Enable
SSR	Set DO register to SRVAL (attribute)

Initial memory content is determined by the INIT_xx attributes. Separate attributes determine the output register value after device configuration (INIT) and SSR is asserted (SRVAL). Both attributes (INIT_B and SRVAL) are available for each port when a block SelectRAM+ resource is configured as dual-port RAM.

Total Amount of SelectRAM+ Memory

Virtex-II Pro SelectRAM+ memory blocks are organized in multiple columns. The number of blocks per column depends on the row size, the number of Processor Blocks, and the number of RocketIO transceivers.

Table 25 shows the number of columns as well as the total amount of block SelectRAM+ memory available for each Virtex-II Pro device. The 18 Kb SelectRAM+ blocks are cascadable to implement deeper or wider single- or dual-port memory resources.

Table 25: **Virtex-II Pro SelectRAM+ Memory Available**

Device	Columns	Total SelectRAM+ Memory		
		Blocks	in Kb	in Bits
XC2VP2	4	12	216	221,184
XC2VP4	4	28	504	516,096
XC2VP7	6	44	792	811,008
XC2VP20	8	88	1,584	1,622,016
XC2VP30	8	136	2,448	2,506,752
XC2VPX20	8	88	1,584	1,622,016
XC2VP40	10	192	3,456	3,538,944
XC2VP50	12	232	4,176	4,276,224
XC2VP70	14	328	5,904	6,045,696
XC2VPX70	14	308	5,544	5,677,056
XC2VP100	16	444	7,992	8,183,808

Figure 52 shows the layout of the block RAM columns in the XC2VP4 device.

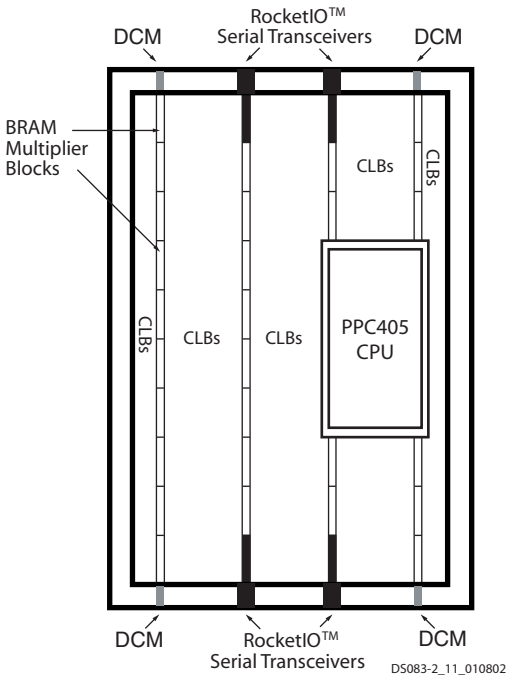


Figure 52: **XC2VP4 Block RAM Column Layout**

SelectIO-Ultra DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: **DC Input and Output Levels**

IOSTANDARD Attribute	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, max	V, min	mA	mA
LVTTL	–0.2	0.8	2.0	3.45	0.4	2.4	24	–24
LVCMOS33	–0.2	0.8	2.0	3.45	0.4	V_{CCO} – 0.4	24	–24
LVCMOS25	–0.2	0.7	1.7	V_{CCO} + 0.4	0.4	V_{CCO} – 0.4	24	–24
LVCMOS18	–0.2	30% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.4	0.4	V_{CCO} – 0.45	16	–16
LVCMOS15	–0.2	30% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.4	0.4	V_{CCO} – 0.45	16	–16
PCI33_3	–0.2	30% V_{CCO}	50% V_{CCO}	3.6	10% V_{CCO}	90% V_{CCO}		
PCI66_3	–0.2	30% V_{CCO}	50% V_{CCO}	3.6	10% V_{CCO}	90% V_{CCO}		
PCIX	–0.2	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)
GTLP	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.6	n/a	36	n/a
GTL	–0.2	V_{REF} – 0.05	V_{REF} + 0.05	V_{CCO} + 0.4	0.4	n/a	40	n/a
HSTL_I	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	8(2)	–8(2)
HSTL_II	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	16(2)	–16(2)
HSTL_III	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	24(2)	–8(2)
HSTL_IV	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	48(2)	–8(2)
SSTL2_I	–0.2	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2_II	–0.2	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL18_I	–0.2	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	6.7	–6.7
SSTL18_II	–0.2	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	13.4	–13.4

Notes:
1. Tested according to relevant specifications.
2. This applies to 1.5V and 1.8V HSTL.

LDT DC Specifications (LDT_25)

Table 7: **LDT DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Differential Output Voltage	V_{OD}	R_T = 100 ohm across Q and $\overline{Q}$ signals	495	600	715	mV
Change in V_{OD} Magnitude	ΔV_{OD}		–15		15	mV
Output Common Mode Voltage	V_{OCM}	R_T = 100 ohm across Q and $\overline{Q}$ signals	495	600	715	mV
Change in V_{OS} Magnitude	ΔV_{OCM}		–15		15	mV
Input Differential Voltage	V_{ID}		200	600	1000	mV
Change in V_{ID} Magnitude	ΔV_{ID}		–15		15	mV
Input Common Mode Voltage	V_{ICM}		440	600	780	mV
Change in V_{ICM} Magnitude	ΔV_{ICM}		–15		15	mV

Table 31: **RocketIO X RXUSRCLK2 Switching Characteristics *(Continued)***

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
RXDEC64B66BUSE RXDEC8B10BUSE control input	$T_{GCCK\_}RDEC/T_{GCCK\_}RDEC$				ns, min
RXDESCRAM64B66BUSE control input	$T_{GCCK\_}RDES/T_{GCCK\_}RDES$				ns, min
RXINTDATAWIDTH control input	$T_{GCCK\_}RIDATW/T_{GCCK\_}RIDATW$				ns, min
RXSLIDE control input	$T_{GCCK\_}RXSLIDE/T_{GCCK\_}RXSLIDE$				ns, min
Clock to Out					
PMARXLOCK status output	$T_{GCKST\_}PLCK$				ns, max
RXNOTINTABLE status outputs	$T_{GCKST\_}RNIT$				ns, max
RXDISPERR status outputs	$T_{GCKST\_}RDERR$				ns, max
RXCHARISCOMMA status outputs	$T_{GCKST\_}RCMCH$				ns, max
RXREALIGN status output	$T_{GCKST\_}ALIGN$				ns, max
RXCOMMADET status output	$T_{GCKST\_}CMDT$				ns, max
RXLOSSOFSYNC status outputs	$T_{GCKST\_}RLOS$				ns, max
RXCLKCORCNT status outputs	$T_{GCKST\_}RCCCNT$				ns, max
RXBUFSTATUS status outputs	$T_{GCKST\_}RBSTA$				ns, max
CHBONDDONE status output	$T_{GCKST\_}CHBD$				ns, max
RXCHARISK status outputs	$T_{GCKST\_}RKCH$				ns, max
RXRUNDISP status outputs	$T_{GCKST\_}RRDIS$				ns, max
RXDATA data outputs	$T_{GCKDO\_}RDAT$				ns, max
Clock					
RXUSRCLK2 minimum pulse width, High	T_{RX2PWH}				ns, min
RXUSRCLK2 minimum pulse width, Low	T_{RX2PWL}				ns, min

Table 32: **RocketIO RXUSRCLK2 Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (RXUSRCLK2)					
RXRESET control input	$T_{GCCK\_}RRST/T_{GCKC\_}RRST$	0.02/ 0.00	0.02/ 0.00	0.02/ 0.00	ns, min
RXPOLARITY control input	$T_{GCCK\_}RPOL/T_{GCKC\_}RPOL$	0.02/ 0.00	0.02/ 0.00	0.02/ 0.00	ns, min
ENCHANSYNC control input	$T_{GCCK\_}ECSY/T_{GCKC\_}ECSY$	0.02/ 0.00	0.02/ 0.00	0.02/ 0.00	ns, min
Clock to Out					
RXNOTINTABLE status outputs	$T_{GCKST\_}RNIT$	0.50	0.50	0.55	ns, max
RXDISPERR status outputs	$T_{GCKST\_}RDERR$	0.50	0.50	0.55	ns, max
RXCHARISCOMMA status outputs	$T_{GCKST\_}RCMCH$	0.50	0.50	0.55	ns, max
RXREALIGN status output	$T_{GCKST\_}ALIGN$	0.41	0.41	0.46	ns, max
RXCOMMADET status output	$T_{GCKST\_}CMDT$	0.41	0.41	0.46	ns, max
RXLOSSOFSYNC status outputs	$T_{GCKST\_}RLOS$	0.50	0.50	0.55	ns, max
RXCLKCORCNT status outputs	$T_{GCKST\_}RCCCNT$	0.41	0.41	0.46	ns, max

Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information

DS083 (v5.0) June 21, 2011 **Product Specification**

This document provides Virtex™-II Pro Device/Package Combinations, Maximum I/Os, and Virtex-II Pro Pin Definitions, followed by pinout tables, for these packages:

- FG256/FGG256 Fine-Pitch BGA Package
- FG456/FGG456 Fine-Pitch BGA Package
- FG676/FGG676 Fine-Pitch BGA Package
- FF672 Flip-Chip Fine-Pitch BGA Package
- FF896 Flip-Chip Fine-Pitch BGA Package
- FF1152 Flip-Chip Fine-Pitch BGA Package
- FF1148 Flip-Chip Fine-Pitch BGA Package
- FF1517 Flip-Chip Fine-Pitch BGA Package
- FF1704 Flip-Chip Fine-Pitch BGA Package
- FF1696 Flip-Chip Fine-Pitch BGA Package

For device pinout diagrams and layout guidelines, refer to the **Virtex-II Pro Platform FPGA User Guide**. ASCII package pinout files are also available for download from the Xilinx website (**www.xilinx.com**).

Virtex-II Pro Device/Package Combinations and Maximum I/Os(1)

Wire-bond and flip-chip packages are available. Table 1 and Table 2 show the maximum number of user I/Os possible in wire-bond and flip-chip packages, respectively.

- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FGG denotes Pb-free wire-bond fine-pitch BGA (1.00 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch)

Table 1: **Wire-Bond Packages Information**

Package(1)	FG256/ FGG256	FG456/ FGG456	FG676/ FGG676
Pitch (mm)	1.00	1.00	1.00
Size (mm)	17 x 17	23 x 23	26 x 26
Maximum I/Os	140	248	412

Notes:
1. Wire-bond packages include FGG*nnn* Pb-free versions. See Virtex-II Pro Ordering Examples (Module 1).

Table 2: **Flip-Chip Packages Information**

Package	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Size (mm)	27 x 27	31 x 31	35 x 35	35 x 35	40 x 40	42.5 x 42.5	42.5 x 42.5
Maximum I/Os	396	556	644	812	964	1040	1200

Table 3 shows the number of available I/Os, the number of RocketIO™ (or RocketIO X) multi-gigabit transceiver (MGT) pins, and the number of differential I/O pairs for each Virtex-II Pro device/package combination. The number of I/Os per package includes all user I/Os *except* the fifteen control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, and RSVD), the nine (per transceiver) RocketIO MGT pins (TXP, TXN, RXP, RXN, AVCCAUXTX, AVCCAUXRX, VTTX, VTRX, and GNDA), and for Virtex-II Pro X devices only, the two BREFCLKN/ BREFCLKP differential clock input pairs (four pins). The Virtex-II Pro X devices are highlighted in bold type.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L06N_6	V1			
6	IO_L43P_6	U4	NC		
6	IO_L43N_6	U3	NC		
6	IO_L45P_6	U2	NC		
6	IO_L45N_6/VREF_6	U1	NC		
6	IO_L47P_6	U5	NC		
6	IO_L47N_6	T5	NC		
6	IO_L48P_6	T4	NC		
6	IO_L48N_6	T3	NC		
6	IO_L49P_6	T2	NC		
6	IO_L49N_6	T1	NC		
6	IO_L51P_6	R4	NC		
6	IO_L51N_6/VREF_6	R3	NC		
6	IO_L53P_6	R2	NC		
6	IO_L53N_6	R1	NC		
6	IO_L54P_6	R5	NC		
6	IO_L54N_6	P6	NC		
6	IO_L55P_6	P4	NC		
6	IO_L55N_6	P3	NC		
6	IO_L57P_6	P2	NC		
6	IO_L57N_6/VREF_6	P1	NC		
6	IO_L59P_6	P5	NC		
6	IO_L59N_6	N5	NC		
6	IO_L60P_6	N4	NC		
6	IO_L60N_6	N3	NC		
6	IO_L85P_6	N2			
6	IO_L85N_6	N1			
6	IO_L87P_6	N6			
6	IO_L87N_6/VREF_6	M6			
6	IO_L89P_6	M5			
6	IO_L89N_6	M4			
6	IO_L90P_6	M3			
6	IO_L90N_6	M2			
7	IO_L90P_7	L2			
7	IO_L90N_7	L3			
7	IO_L88P_7	L4			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L01P_6/VRN_6	AF24			
6	IO_L01N_6/VRP_6	AE24			
6	IO_L02P_6	AD23			
6	IO_L02N_6	AC24			
6	IO_L03P_6	AE26			
6	IO_L03N_6/VREF_6	AF25			
6	IO_L04P_6	AD25			
6	IO_L04N_6	AD26			
6	IO_L05P_6	AC25			
6	IO_L05N_6	AC26			
6	IO_L06P_6	AB23			
6	IO_L06N_6	AB24			
6	IO_L39P_6	AB25	NC	NC	NC
6	IO_L39N_6/VREF_6	AB26	NC	NC	NC
6	IO_L41P_6	AA22	NC	NC	NC
6	IO_L41N_6	AA23	NC	NC	NC
6	IO_L42P_6	AA24	NC	NC	NC
6	IO_L42N_6	AA25	NC	NC	NC
6	IO_L43P_6	Y21	NC		
6	IO_L43N_6	Y22	NC		
6	IO_L44P_6	Y23	NC		
6	IO_L44N_6	Y24	NC		
6	IO_L45P_6	AA26	NC		
6	IO_L45N_6/VREF_6	Y26	NC		
6	IO_L46P_6	W21	NC		
6	IO_L46N_6	W22	NC		
6	IO_L47P_6	W23	NC		
6	IO_L47N_6	W24	NC		
6	IO_L48P_6	W25	NC		
6	IO_L48N_6	W26	NC		
6	IO_L49P_6	V20	NC		
6	IO_L49N_6	V21	NC		
6	IO_L50P_6	V22	NC		
6	IO_L50N_6	V23	NC		
6	IO_L51P_6	V24	NC		
6	IO_L51N_6/VREF_6	V25	NC		
6	IO_L52P_6	U21	NC		

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
1	VCCO_1		K13			
1	VCCO_1		K12			
1	VCCO_1		K11			
1	VCCO_1		K10			
1	VCCO_1		J13			
1	VCCO_1		J12			
1	VCCO_1		J11			
1	VCCO_1		J10			
2	VCCO_2		R10			
2	VCCO_2		P10			
2	VCCO_2		N10			
2	VCCO_2		N9			
2	VCCO_2		M10			
2	VCCO_2		M9			
2	VCCO_2		L10			
2	VCCO_2		L9			
2	VCCO_2		K9			
2	VCCO_2		J9			
3	VCCO_3		AB9			
3	VCCO_3		AA9			
3	VCCO_3		Y10			
3	VCCO_3		Y9			
3	VCCO_3		W10			
3	VCCO_3		W9			
3	VCCO_3		V10			
3	VCCO_3		V9			
3	VCCO_3		U10			
3	VCCO_3		T10			
4	VCCO_4		AB13			
4	VCCO_4		AB12			
4	VCCO_4		AB11			
4	VCCO_4		AB10			
4	VCCO_4		AA15			
4	VCCO_4		AA14			
4	VCCO_4		AA13			
4	VCCO_4		AA12			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	VCCINT		Y13			
N/A	VCCINT		Y12			
N/A	VCCINT		W20			
N/A	VCCINT		W11			
N/A	VCCINT		V20			
N/A	VCCINT		V11			
N/A	VCCINT		U20			
N/A	VCCINT		U11			
N/A	VCCINT		T20			
N/A	VCCINT		T11			
N/A	VCCINT		R20			
N/A	VCCINT		R11			
N/A	VCCINT		P20			
N/A	VCCINT		P11			
N/A	VCCINT		N20			
N/A	VCCINT		N11			
N/A	VCCINT		M20			
N/A	VCCINT		M11			
N/A	VCCINT		L19			
N/A	VCCINT		L18			
N/A	VCCINT		L17			
N/A	VCCINT		L16			
N/A	VCCINT		L15			
N/A	VCCINT		L14			
N/A	VCCINT		L13			
N/A	VCCINT		L12			
N/A	GND		AK22			
N/A	GND		AK9			
N/A	GND		AJ29			
N/A	GND		AJ2			
N/A	GND		AH28			
N/A	GND		AH17			
N/A	GND		AH14			
N/A	GND		AH3			
N/A	GND		AG27			
N/A	GND		AG22			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
1	IO_L74N_1/GCLK1P	D17				
1	IO_L74P_1/GCLK0S	E17				
1	IO_L73N_1	F17				
1	IO_L73P_1	G17				
1	IO_L69N_1/VREF_1	K17				
1	IO_L69P_1	L17				
1	IO_L68N_1	D16				
1	IO_L68P_1	E16				
1	IO_L67N_1	F16				
1	IO_L67P_1	G16				
1	IO_L57N_1/VREF_1	H16				
1	IO_L57P_1	J16				
1	IO_L56N_1	D15				
1	IO_L56P_1	D14				
1	IO_L55N_1	F15				
1	IO_L55P_1	G15				
1	IO_L54N_1	K16				
1	IO_L54P_1	L16				
1	IO_L53_1/No_Pair	C13				
1	IO_L50_1/No_Pair	C14				
1	IO_L49N_1	E14				
1	IO_L49P_1	F14				
1	IO_L48N_1	J15				
1	IO_L48P_1	K15				
1	IO_L47N_1	C11				
1	IO_L47P_1	D11				
1	IO_L46N_1	D12				
1	IO_L46P_1	D13				
1	IO_L45N_1/VREF_1	G14				
1	IO_L45P_1	H14				
1	IO_L44N_1	D10				
1	IO_L44P_1	E10				
1	IO_L43N_1	E13				
1	IO_L43P_1	F13				
1	IO_L39N_1	J14				
1	IO_L39P_1	K14				
1	IO_L38N_1	C9				
1	IO_L38P_1	D9				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
3	IO_L58P_3	W6				
3	IO_L57N_3/VREF_3	Y3				
3	IO_L57P_3	Y4				
3	IO_L56N_3	W7				
3	IO_L56P_3	W8				
3	IO_L55N_3	Y6				
3	IO_L55P_3	Y7				
3	IO_L54N_3	AA2				
3	IO_L54P_3	AB2				
3	IO_L53N_3	W9				
3	IO_L53P_3	W10				
3	IO_L52N_3	AA3				
3	IO_L52P_3	AA4				
3	IO_L51N_3/VREF_3	AB1				
3	IO_L51P_3	AC1				
3	IO_L50N_3	Y9				
3	IO_L50P_3	Y10				
3	IO_L49N_3	AA5				
3	IO_L49P_3	AA6				
3	IO_L48N_3	AB3				
3	IO_L48P_3	AB4				
3	IO_L47N_3	AA7				
3	IO_L47P_3	AA8				
3	IO_L46N_3	AB5				
3	IO_L46P_3	AB6				
3	IO_L45N_3/VREF_3	AC2				
3	IO_L45P_3	AD2				
3	IO_L44N_3	AA9				
3	IO_L44P_3	AA10				
3	IO_L43N_3	AC3				
3	IO_L43P_3	AC4				
3	IO_L42N_3	AD1				
3	IO_L42P_3	AE1				
3	IO_L41N_3	AB7				
3	IO_L41P_3	AB8				
3	IO_L40N_3	AC6				
3	IO_L40P_3	AC7				
3	IO_L39N_3/VREF_3	AD3				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
6	IO_L53P_6	W25				
6	IO_L53N_6	W26				
6	IO_L54P_6	AB33				
6	IO_L54N_6	AA33				
6	IO_L55P_6	Y28				
6	IO_L55N_6	Y29				
6	IO_L56P_6	W27				
6	IO_L56N_6	W28				
6	IO_L57P_6	Y31				
6	IO_L57N_6/VREF_6	Y32				
6	IO_L58P_6	W29				
6	IO_L58N_6	W30				
6	IO_L59P_6	W24				
6	IO_L59N_6	V24				
6	IO_L60P_6	AA34				
6	IO_L60N_6	Y34				
6	IO_L85P_6	W31				
6	IO_L85N_6	W32				
6	IO_L86P_6	V25				
6	IO_L86N_6	V26				
6	IO_L87P_6	Y33				
6	IO_L87N_6/VREF_6	W33				
6	IO_L88P_6	V29				
6	IO_L88N_6	V30				
6	IO_L89P_6	V27				
6	IO_L89N_6	V28				
6	IO_L90P_6	V31				
6	IO_L90N_6	V32				
7	IO_L90P_7	U32				
7	IO_L90N_7	U31				
7	IO_L89P_7	U28				
7	IO_L89N_7	U27				
7	IO_L88P_7	V33				
7	IO_L88N_7/VREF_7	U33				
7	IO_L87P_7	U30				
7	IO_L87N_7	U29				
7	IO_L86P_7	U26				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
2	IO_L21P_2	E6		
2	IO_L22N_2/VREF_2	F7		
2	IO_L22P_2	F8		
2	IO_L23N_2	M10		
2	IO_L23P_2	L10		
2	IO_L24N_2	G5		
2	IO_L24P_2	F5		
2	IO_L25N_2	F3		
2	IO_L25P_2	F4		
2	IO_L26N_2	M8		
2	IO_L26P_2	M9		
2	IO_L27N_2	F1		
2	IO_L27P_2	F2		
2	IO_L28N_2/VREF_2	G6		
2	IO_L28P_2	G7		
2	IO_L29N_2	M7		
2	IO_L29P_2	N8		
2	IO_L30N_2	G3		
2	IO_L30P_2	H4		
2	IO_L31N_2	G1		
2	IO_L31P_2	G2		
2	IO_L32N_2	N10		
2	IO_L32P_2	N11		
2	IO_L33N_2	H5		
2	IO_L33P_2	H6		
2	IO_L34N_2/VREF_2	H2		
2	IO_L34P_2	H3		
2	IO_L35N_2	N6		
2	IO_L35P_2	N7		
2	IO_L36N_2	K4		
2	IO_L36P_2	J4		
2	IO_L37N_2	J2		
2	IO_L37P_2	J3		
2	IO_L38N_2	P10		
2	IO_L38P_2	P11		
2	IO_L39N_2	K5		
2	IO_L39P_2	K6		
2	IO_L40N_2/VREF_2	L3		

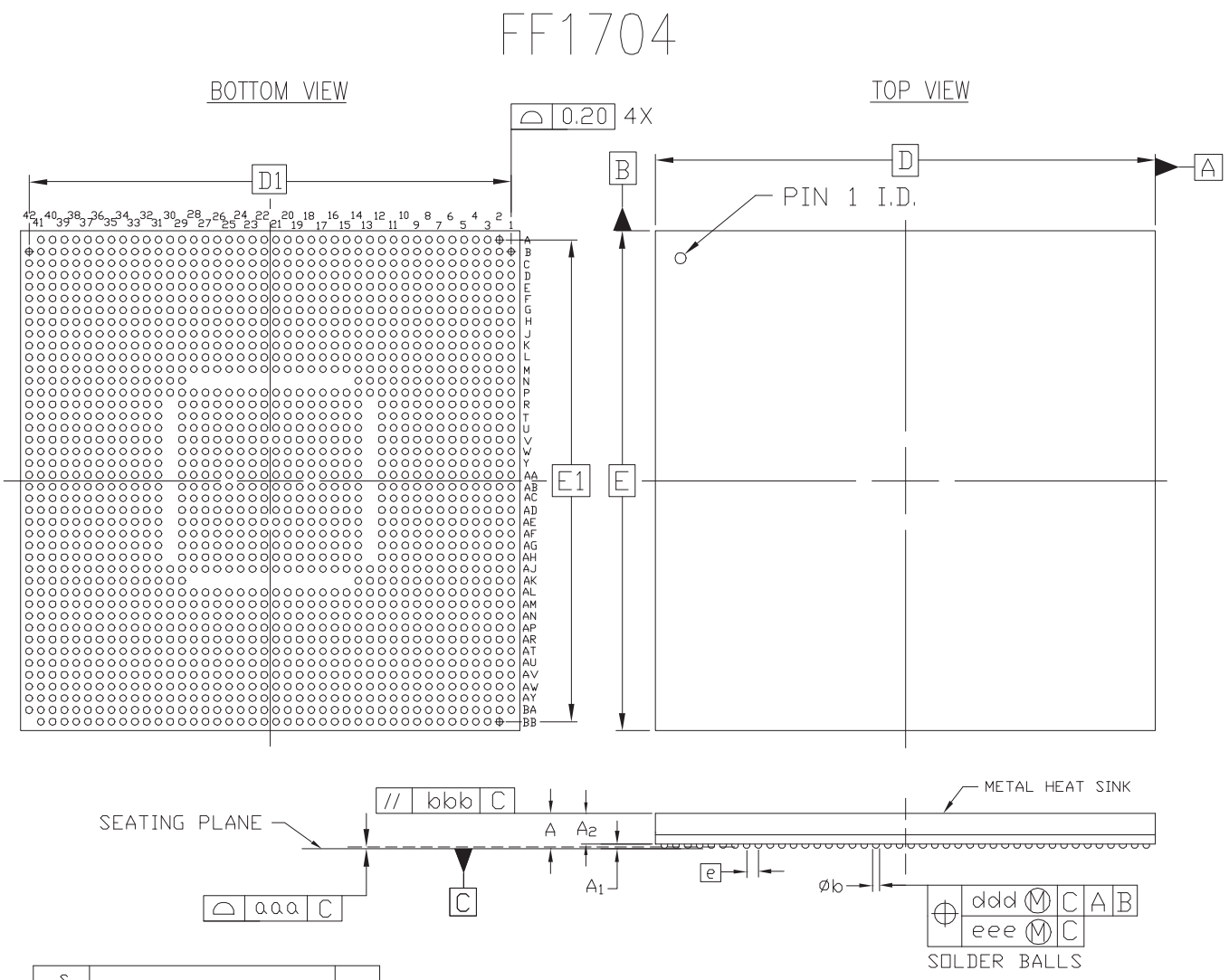
Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
3	IO_L36N_3	AE4		
3	IO_L36P_3	AF4		
3	IO_L35N_3	AC10		
3	IO_L35P_3	AD10		
3	IO_L34N_3	AE1		
3	IO_L34P_3	AE2		
3	IO_L33N_3/VREF_3	AF6		
3	IO_L33P_3	AF7		
3	IO_L32N_3	AC8		
3	IO_L32P_3	AC9		
3	IO_L31N_3	AF2		
3	IO_L31P_3	AF3		
3	IO_L30N_3	AG5		
3	IO_L30P_3	AG6		
3	IO_L29N_3	AD9		
3	IO_L29P_3	AE9		
3	IO_L28N_3	AG4		
3	IO_L28P_3	AH3		
3	IO_L27N_3/VREF_3	AG2		
3	IO_L27P_3	AG3		
3	IO_L26N_3	AD7		
3	IO_L26P_3	AE7		
3	IO_L25N_3	AH6		
3	IO_L25P_3	AH7		
3	IO_L24N_3	AH5		
3	IO_L24P_3	AJ5		
3	IO_L23N_3	AE8		
3	IO_L23P_3	AF8		
3	IO_L22N_3	AH1		
3	IO_L22P_3	AH2		
3	IO_L21N_3/VREF_3	AJ6		
3	IO_L21P_3	AK6		
3	IO_L20N_3	AG7		
3	IO_L20P_3	AG8		
3	IO_L19N_3	AJ3		
3	IO_L19P_3	AJ4		
3	IO_L18N_3	AJ1		
3	IO_L18P_3	AJ2		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
4	IO_L03N_4/D2	AN10		
4	IO_L03P_4/D3	AM10		
4	IO_L05_4/No_Pair	AK10		
4	IO_L06N_4/VRP_4	AR10		
4	IO_L06P_4/VRN_4	AP10		
4	IO_L07N_4	AU10		
4	IO_L07P_4/VREF_4	AT10		
4	IO_L08N_4	AJ12		
4	IO_L08P_4	AJ13		
4	IO_L09N_4	AL10		
4	IO_L09P_4/VREF_4	AL11		
4	IO_L19N_4	AN11		
4	IO_L19P_4	AM11		
4	IO_L20N_4	AH13		
4	IO_L20P_4	AH14		
4	IO_L21N_4	AR11		
4	IO_L21P_4	AP11		
4	IO_L25N_4	AU11		
4	IO_L25P_4	AT11		
4	IO_L26N_4	AL14		
4	IO_L26P_4	AK14		
4	IO_L27N_4	AM12		
4	IO_L27P_4/VREF_4	AL12		
4	IO_L28N_4	AT12	NC	
4	IO_L28P_4	AR12	NC	
4	IO_L29N_4	AJ14	NC	
4	IO_L29P_4	AJ15	NC	
4	IO_L30N_4	AM13	NC	
4	IO_L30P_4	AL13	NC	
4	IO_L34N_4	AP12	NC	
4	IO_L34P_4	AN13	NC	
4	IO_L35N_4	AL15	NC	
4	IO_L35P_4	AK15	NC	
4	IO_L36N_4	AT13	NC	
4	IO_L36P_4/VREF_4	AR13	NC	
4	IO_L37N_4	AN14		
4	IO_L37P_4	AM14		
4	IO_L38N_4	AH15		

FF1704 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.45	
A_1	0.40	0.50	0.60	
A_2			2.85	
D/E	42.50 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M		42		2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAV-1 (DEPOPULATED)

Figure 9: **FF1704 Flip-Chip Fine-Pitch BGA Package Specifications**

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L22N_2/VREF_2	L4	
2	IO_L22P_2	L5	
2	IO_L23N_2	T8	
2	IO_L23P_2	T9	
2	IO_L24N_2	L3	
2	IO_L24P_2	K3	
2	IO_L25N_2	L1	
2	IO_L25P_2	L2	
2	IO_L26N_2	U12	
2	IO_L26P_2	V12	
2	IO_L27N_2	M7	
2	IO_L27P_2	L6	
2	IO_L28N_2/VREF_2	M5	
2	IO_L28P_2	M6	
2	IO_L29N_2	U10	
2	IO_L29P_2	U11	
2	IO_L30N_2	M3	
2	IO_L30P_2	M4	
2	IO_L31N_2	N6	
2	IO_L31P_2	N7	
2	IO_L32N_2	U7	
2	IO_L32P_2	U8	
2	IO_L33N_2	N3	
2	IO_L33P_2	N4	
2	IO_L34N_2/VREF_2	N2	
2	IO_L34P_2	M2	
2	IO_L35N_2	V10	
2	IO_L35P_2	V11	
2	IO_L36N_2	P6	
2	IO_L36P_2	P7	
2	IO_L37N_2	P1	
2	IO_L37P_2	P2	
2	IO_L38N_2	V8	
2	IO_L38P_2	V9	
2	IO_L39N_2	R6	
2	IO_L39P_2	P5	
2	IO_L40N_2/VREF_2	R4	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L59N_2	AA11	
2	IO_L59P_2	AA12	
2	IO_L60N_2	W1	
2	IO_L60P_2	W2	
2	IO_L85N_2	Y2	
2	IO_L85P_2	Y3	
2	IO_L86N_2	AA9	
2	IO_L86P_2	AA10	
2	IO_L87N_2	AA5	
2	IO_L87P_2	AA6	
2	IO_L88N_2/VREF_2	AA4	
2	IO_L88P_2	Y4	
2	IO_L89N_2	AA7	
2	IO_L89P_2	AA8	
2	IO_L90N_2	AA2	
2	IO_L90P_2	AA3	
3	IO_L90N_3	AB5	
3	IO_L90P_3	AB6	
3	IO_L89N_3	AB11	
3	IO_L89P_3	AB12	
3	IO_L88N_3	AB2	
3	IO_L88P_3	AB3	
3	IO_L87N_3/VREF_3	AB4	
3	IO_L87P_3	AC4	
3	IO_L86N_3	AB9	
3	IO_L86P_3	AB10	
3	IO_L85N_3	AC2	
3	IO_L85P_3	AC3	
3	IO_L60N_3	AD5	
3	IO_L60P_3	AD6	
3	IO_L59N_3	AB7	
3	IO_L59P_3	AB8	
3	IO_L58N_3	AD1	
3	IO_L58P_3	AD2	
3	IO_L57N_3/VREF_3	AE4	
3	IO_L57P_3	AE5	