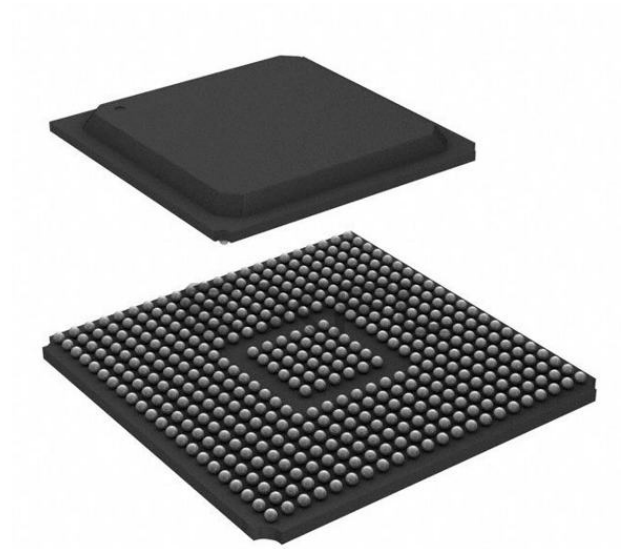

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	352
Number of Logic Elements/Cells	3168
Total RAM Bits	221184
Number of I/O	156
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp2-5fg456c

The top half of the figure shows the transmission of words split across four transceivers (channels or lanes). PPPP, QQQQ, RRRR, SSSS, and TTTT represent words sent over the four channels.

The bottom-left portion of Figure 13 shows the initial situation in the FPGA's receivers at the other end of the four channels. Due to variations in transmission delay—especially if the channels are routed through repeaters—the FPGA fabric might not correctly assemble the bytes into complete words. The bottom-left illustration shows the incorrect assembly of data words PQPP, QRQQ, RSRR, and so forth.

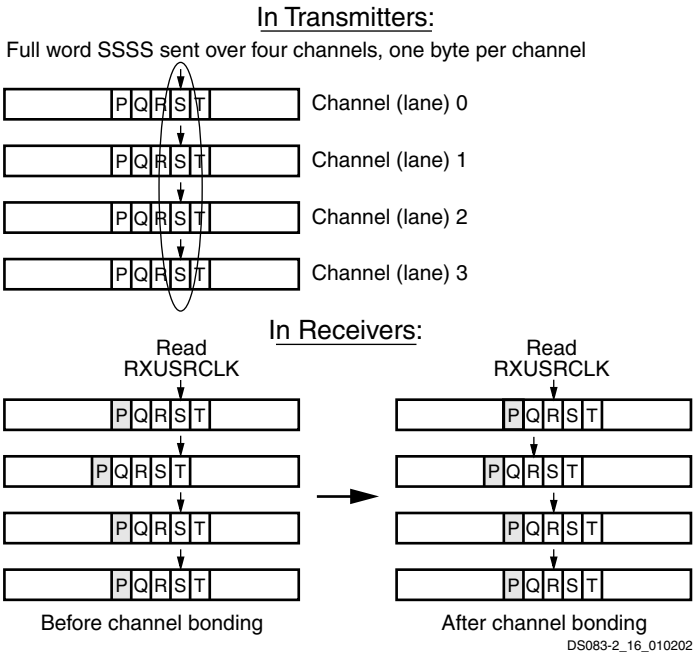


Figure 13: **Channel Bonding (Alignment)**

To support correction of this misalignment, the data stream includes special byte sequences that define corresponding points in the several channels. In the bottom half of Figure 13, the shaded "P" bytes represent these special characters. Each receiver recognizes the "P" channel bonding character, and remembers its location in the buffer. At some point, one transceiver designated as the master instructs all the transceivers to align to the channel bonding character "P" (or to some location relative to the channel bonding character).

After this operation, words transmitted to the FPGA fabric are properly aligned: RRRR, SSSS, TTTT, and so forth, as shown in the bottom-right portion of Figure 13. To ensure that the channels remain properly aligned following the channel bonding operation, the master transceiver must also control the clock correction operations described in the previous section for all channel-bonded transceivers.

Transmitter Buffer

The transmitter's buffer write pointer (TXUSRCLK) is frequency-locked to its read pointer (REFCLK). Therefore, clock correction and channel bonding are not required. The purpose of the transmitter's buffer is to accommodate a phase difference between TXUSRCLK and REFCLK. A simple FIFO suffices for this purpose. A FIFO depth of four will permit reliable operation with simple detection of overflow or underflow, which could occur if the clocks are not frequency-locked.

RocketIO Configuration

This section outlines functions that can be selected or controlled by configuration. Xilinx implementation software supports 16 transceiver primitives, as shown in Table 6.

Each of the primitives in Table 6 defines default values for the configuration attributes, allowing some number of them to be modified by the user. Refer to the ***RocketIO Transceiver User Guide*** for more details.

Table 6: **Supported RocketIO MGT Protocol Primitives**

GT_CUSTOM	Fully customizable by user
GT_FIBRE_CHAN_1	Fibre Channel, 1-byte data path
GT_FIBRE_CHAN_2	Fibre Channel, 2-byte data path
GT_FIBRE_CHAN_4	Fibre Channel, 4-byte data path
GT_ETHERNET_1	Gigabit Ethernet, 1-byte data path
GT_ETHERNET_2	Gigabit Ethernet, 2-byte data path
GT_ETHERNET_4	Gigabit Ethernet, 4-byte data path
GT_XAUI_1	10-gigabit Ethernet, 1-byte data path
GT_XAUI_2	10-gigabit Ethernet, 2-byte data path
GT_XAUI_4	10-gigabit Ethernet, 4-byte data path
GT_INFINIBAND_1	Infiniband, 1-byte data path
GT_INFINIBAND_2	Infiniband, 2-byte data path
GT_INFINIBAND_4	Infiniband, 4-byte data path
GT_AURORA_1(1)	1-byte data path
GT_AURORA_2(1)	2-byte data path
GT_AURORA_4(1)	4-byte data path

Notes:
1. For more information on the Aurora protocol, visit http://www.xilinx.com.

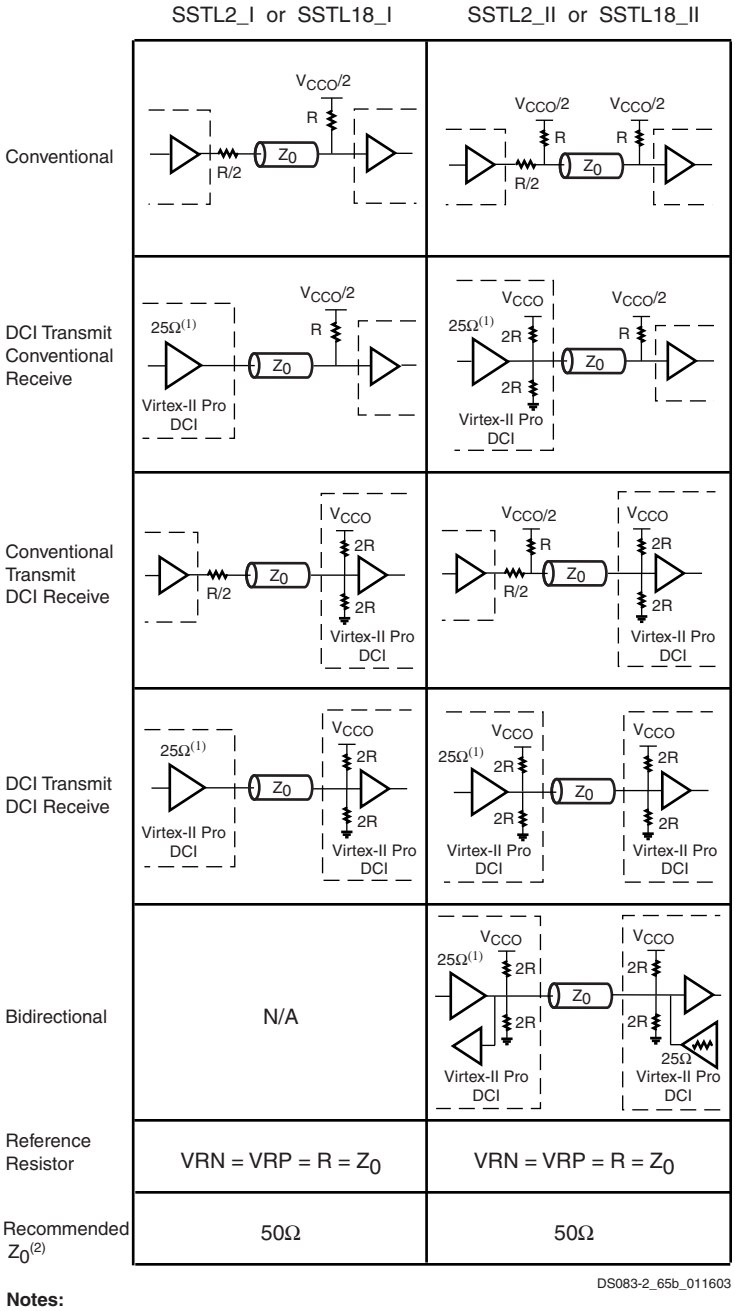
Other RocketIO Features and Notes

CRC

The RocketIO transceiver CRC logic supports the 32-bit invariant CRC calculation used by Infiniband, FibreChannel, and Gigabit Ethernet.

On the transmitter side, the CRC logic recognizes where the CRC bytes should be inserted and replaces four placeholder bytes at the tail of a data packet with the computed CRC. For Gigabit Ethernet and FibreChannel, transmitter

Figure 29 provides examples illustrating the use of the SSTL2_I_DCI, SSTL2_II_DCI, SSTL18_I_DCI, and SSTL18_II_DCI I/O standards. For a complete list, see the ***Virtex-II Pro Platform FPGA User Guide***.



Notes:
1. The SSTL-compatible 25Ω series resistor is accounted for in the DCI buffer, and it is not DCI controlled.
2. Z_0 is the recommended PCB trace impedance.

Figure 29: **SSTL DCI Usage Examples**

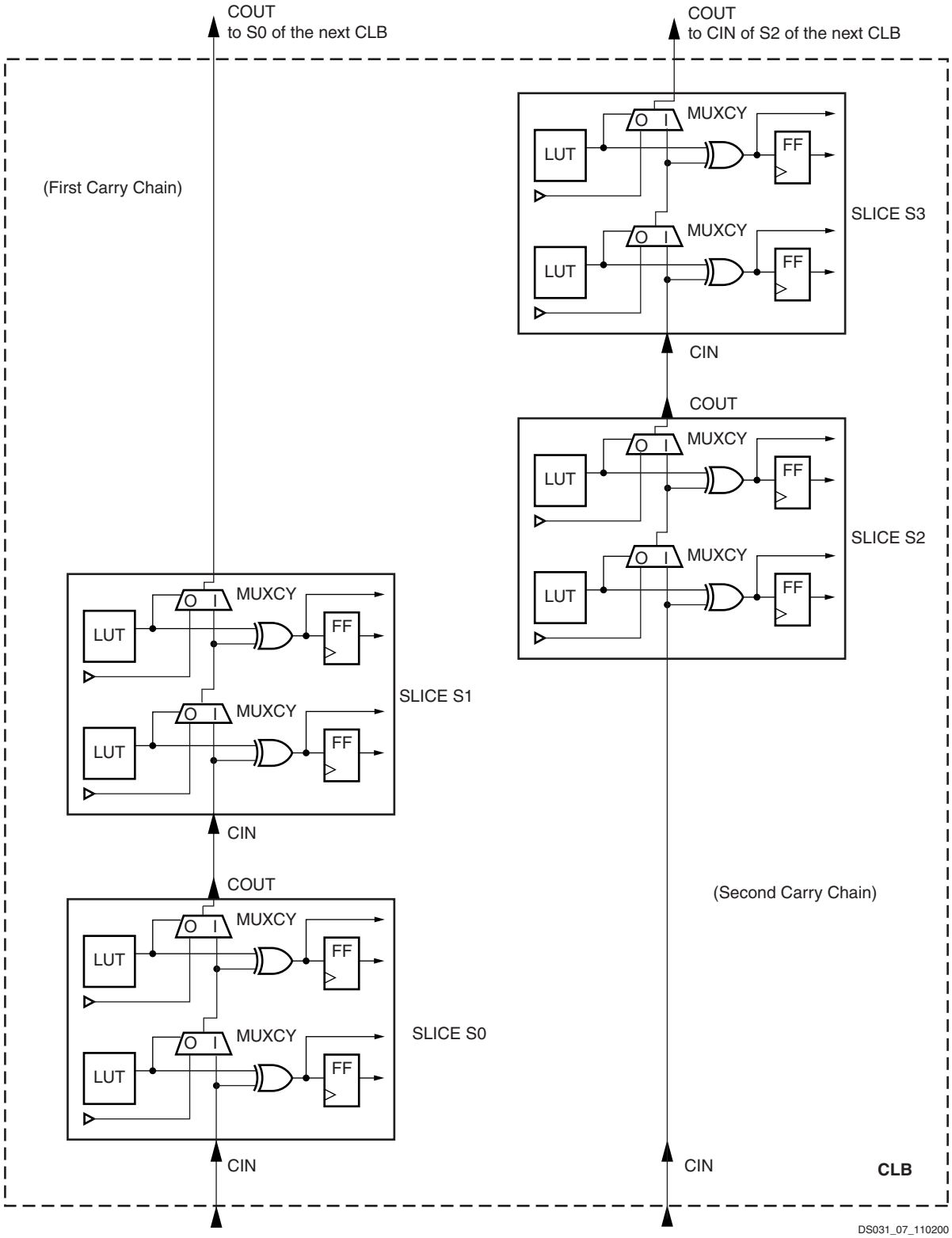


Figure 42: **Fast Carry Logic Path**

Date	Version	Revision
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s.
03/05/07	4.6	*No changes in Module 2 for this revision.*
11/05/07	4.7	• Updated copyright notice and legal disclaimer. • Debug Interface, page 19, and Boundary-Scan (JTAG, IEEE 1532) Mode, page 57: Updated IEEE 1149.1 compliance statement.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner.

Notice of Disclaimer

Virtex-II Pro Data Sheet

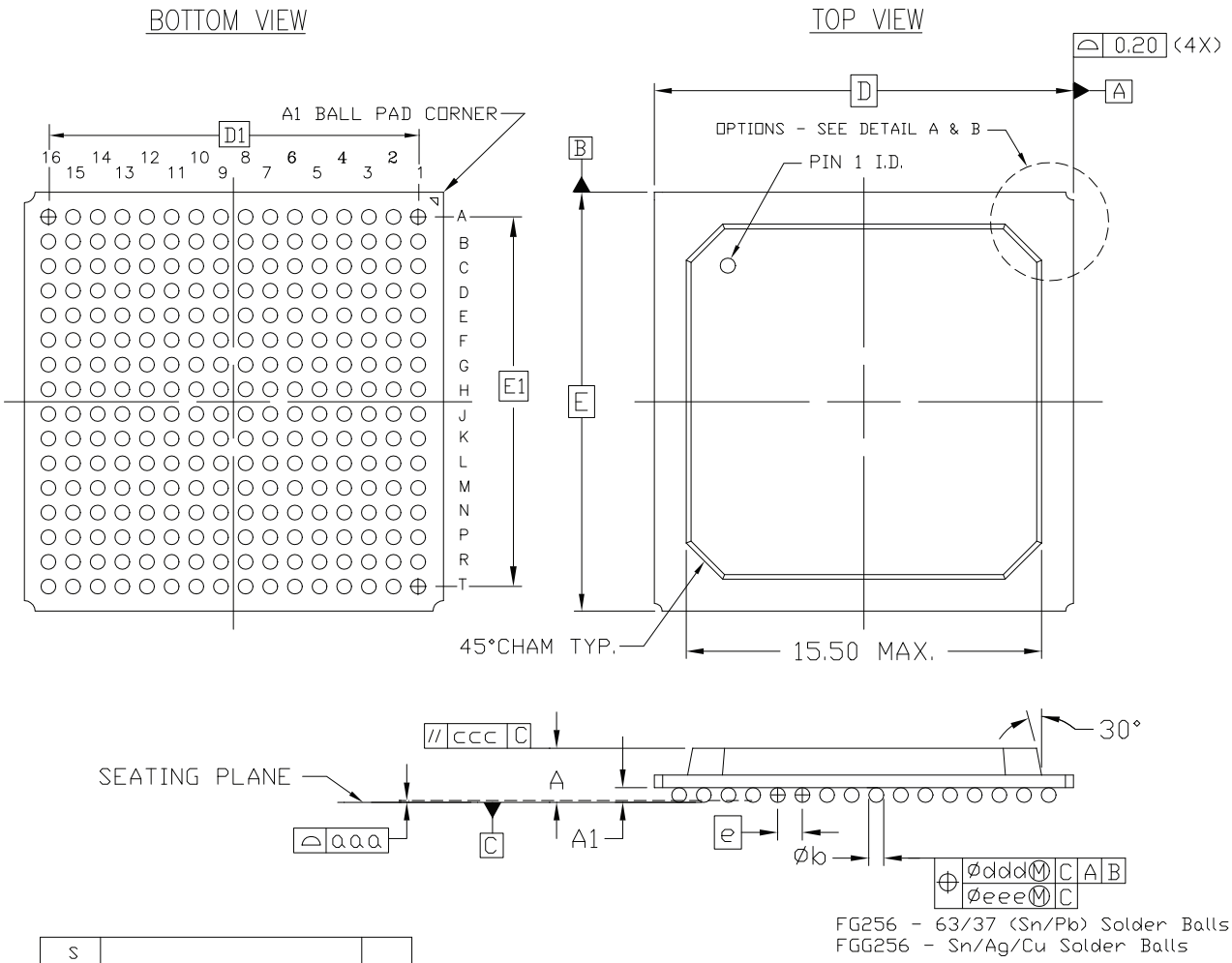
The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
N/A	AVCCAUXRX7	B13
N/A	AVCCAUXRX18	R13
N/A	VTRXPAD18	R12
N/A	RXNPAD18	T13
N/A	RXPPAD18	T12
N/A	GNDA18	P11
N/A	TXPPAD18	T11
N/A	TXNPAD18	T10
N/A	VTTXPAD18	R10
N/A	AVCCAUXTX18	R11
N/A	AVCCAUXRX19	R7
N/A	VTRXPAD19	R6
N/A	RXNPAD19	T7
N/A	RXPPAD19	T6
N/A	GNDA19	P6
N/A	TXPPAD19	T5
N/A	TXNPAD19	T4
N/A	VTTXPAD19	R4
N/A	AVCCAUXTX19	R5
N/A	VCCINT	N4
N/A	VCCINT	N13
N/A	VCCINT	M5
N/A	VCCINT	M12
N/A	VCCINT	E5
N/A	VCCINT	E12
N/A	VCCINT	D4
N/A	VCCINT	D13
N/A	VCCAUX	R16
N/A	VCCAUX	R1
N/A	VCCAUX	B16
N/A	VCCAUX	B1
N/A	GND	T16
N/A	GND	T1
N/A	GND	R2

FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A			2.00	3
A_1	0.35	0.50	0.60	
D/E	17.00 BSC			
D_1/E_1	15.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	16			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. NOMINAL DIMENSION IS TYPICALLY 1.60-1.73mm
4. CONFORMS TO JEDEC MS-034-AAF-1

Figure 1: **FG256/FGG256 Fine-Pitch BGA Package Specifications**

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
0	IO_L55N_0	G12			
0	IO_L55P_0	F12			
0	IO_L57N_0	E12			
0	IO_L57P_0/VREF_0	F13			
0	IO_L67N_0	D12			
0	IO_L67P_0	C12			
0	IO_L69N_0	J13			
0	IO_L69P_0/VREF_0	H13			
0	IO_L74N_0/GCLK7P	E13			
0	IO_L74P_0/GCLK6S	D13			
0	IO_L75N_0/GCLK5P	C13			
0	IO_L75P_0/GCLK4S	B13			
1	IO_L75N_1/GCLK3P	B14			
1	IO_L75P_1/GCLK2S	C14			
1	IO_L74N_1/GCLK1P	D14			
1	IO_L74P_1/GCLK0S	E14			
1	IO_L69N_1/VREF_1	H14			
1	IO_L69P_1	J14			
1	IO_L67N_1	C15			
1	IO_L67P_1	D15			
1	IO_L57N_1/VREF_1	F14			
1	IO_L57P_1	E15			
1	IO_L55N_1	F15			
1	IO_L55P_1	G15			
1	IO_L54N_1	H15			
1	IO_L54P_1	J15			
1	IO_L53_1/No_Pair	F16			
1	IO_L50_1/No_Pair	G16			
1	IO_L49N_1	C17			
1	IO_L49P_1	D17			
1	IO_L48N_1	E16			
1	IO_L48P_1	E17			
1	IO_L46N_1	H16			
1	IO_L46P_1	H17			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
3	IO_L90N_3	P2			
3	IO_L90P_3	P3			
3	IO_L89N_3	P4			
3	IO_L89P_3	P5			
3	IO_L88N_3	P6			
3	IO_L88P_3	P7			
3	IO_L87N_3/VREF_3	R1			
3	IO_L87P_3	R2			
3	IO_L86N_3	R3			
3	IO_L86P_3	R4			
3	IO_L85N_3	R5			
3	IO_L85P_3	R6			
3	IO_L60N_3	P8	NC		
3	IO_L60P_3	R8	NC		
3	IO_L59N_3	T1	NC		
3	IO_L59P_3	T2	NC		
3	IO_L58N_3	T3	NC		
3	IO_L58P_3	T4	NC		
3	IO_L57N_3/VREF_3	T5	NC		
3	IO_L57P_3	T6	NC		
3	IO_L56N_3	R7	NC		
3	IO_L56P_3	T7	NC		
3	IO_L55N_3	T8	NC		
3	IO_L55P_3	U7	NC		
3	IO_L54N_3	U1	NC		
3	IO_L54P_3	V1	NC		
3	IO_L53N_3	U3	NC		
3	IO_L53P_3	U4	NC		
3	IO_L52N_3	U5	NC		
3	IO_L52P_3	U6	NC		
3	IO_L51N_3/VREF_3	V2	NC		
3	IO_L51P_3	V3	NC		
3	IO_L50N_3	V4	NC		
3	IO_L50P_3	V5	NC		
3	IO_L49N_3	V6	NC		
3	IO_L49P_3	V7	NC		

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
1	IO_L54N_1		G13	NC		
1	IO_L54P_1		H13	NC		
1	IO_L53_1/No_Pair		A10	NC		
1	IO_L50_1/No_Pair		B10	NC		
1	IO_L49N_1		F14	NC		
1	IO_L49P_1		G14	NC		
1	IO_L48N_1		F12	NC		
1	IO_L48P_1		F11	NC		
1	IO_L47N_1		B9	NC		
1	IO_L47P_1		C9	NC		
1	IO_L46N_1		E13	NC		
1	IO_L46P_1		E12	NC		
1	IO_L45N_1/VREF_1		G12			
1	IO_L45P_1		H12			
1	IO_L44N_1		A8			
1	IO_L44P_1		B8			
1	IO_L43N_1		D11			
1	IO_L43P_1		E11			
1	IO_L39N_1		G11			
1	IO_L39P_1		H11			
1	IO_L38N_1		C8			
1	IO_L38P_1		D8			
1	IO_L37N_1		D10			
1	IO_L37P_1		E10			
1	IO_L09N_1/VREF_1		G10			
1	IO_L09P_1		H10			
1	IO_L08N_1		C7			
1	IO_L08P_1		D7			
1	IO_L07N_1		F10			
1	IO_L07P_1		F9			
1	IO_L06N_1		G9			
1	IO_L06P_1		H9			
1	IO_L05_1/No_Pair		G8			
1	IO_L03N_1/VREF_1		E9			
1	IO_L03P_1		E8			
1	IO_L02N_1		F8			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
6	IO_L86P_6		T23			
6	IO_L86N_6		T24			
6	IO_L87P_6		U28			
6	IO_L87N_6/VREF_6		U29			
6	IO_L88P_6		T27			
6	IO_L88N_6		T28			
6	IO_L89P_6		T25			
6	IO_L89N_6		T26			
6	IO_L90P_6		V30			
6	IO_L90N_6		U30			
7	IO_L90P_7		R28			
7	IO_L90N_7		R27			
7	IO_L89P_7		R26			
7	IO_L89N_7		R25			
7	IO_L88P_7		T29			
7	IO_L88N_7/VREF_7		R29			
7	IO_L87P_7		P27			
7	IO_L87N_7		P26			
7	IO_L86P_7		R24			
7	IO_L86N_7		R23			
7	IO_L85P_7		P29			
7	IO_L85N_7		P28			
7	IO_L60P_7		N28			
7	IO_L60N_7		N27			
7	IO_L59P_7		P24			
7	IO_L59N_7		P23			
7	IO_L58P_7		P30			
7	IO_L58N_7/VREF_7		N30			
7	IO_L57P_7		M28			
7	IO_L57N_7		M27			
7	IO_L56P_7		R22			
7	IO_L56N_7		P22			
7	IO_L55P_7		N29			
7	IO_L55N_7		M29			
7	IO_L54P_7		L27			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
4	VCCO_4	AD15				
4	VCCO_4	AJ10				
4	VCCO_4	AK15				
4	VCCO_4	AM6				
5	VCCO_5	AC18				
5	VCCO_5	AC19				
5	VCCO_5	AC20				
5	VCCO_5	AC21				
5	VCCO_5	AC22				
5	VCCO_5	AD20				
5	VCCO_5	AD21				
5	VCCO_5	AD22				
5	VCCO_5	AD23				
5	VCCO_5	AJ25				
5	VCCO_5	AK20				
5	VCCO_5	AM29				
6	VCCO_6	V23				
6	VCCO_6	W23				
6	VCCO_6	Y23				
6	VCCO_6	Y24				
6	VCCO_6	Y30				
6	VCCO_6	AA23				
6	VCCO_6	AA24				
6	VCCO_6	AB23				
6	VCCO_6	AB24				
6	VCCO_6	AC24				
6	VCCO_6	AE29				
6	VCCO_6	AJ32				
7	VCCO_7	F32				
7	VCCO_7	K29				
7	VCCO_7	M24				
7	VCCO_7	N23				
7	VCCO_7	N24				
7	VCCO_7	P23				
7	VCCO_7	P24				
7	VCCO_7	R23				
7	VCCO_7	R24				
7	VCCO_7	R30				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
7	IO_L51P_7	N31		
7	IO_L51N_7	P31		
7	IO_L50P_7	T27		
7	IO_L50N_7	R28		
7	IO_L49P_7	M33		
7	IO_L49N_7	M34		
7	IO_L48P_7	M31		
7	IO_L48N_7	M32		
7	IO_L47P_7	R24		
7	IO_L47N_7	R25		
7	IO_L46P_7	M29		
7	IO_L46N_7/VREF_7	M30		
7	IO_L45P_7	L33		
7	IO_L45N_7	L34		
7	IO_L44P_7	P27		
7	IO_L44N_7	P28		
7	IO_L43P_7	L29		
7	IO_L43N_7	L30		
7	IO_L42P_7	K33		
7	IO_L42N_7	K34		
7	IO_L41P_7	P26		
7	IO_L41N_7	R26		
7	IO_L40P_7	K32		
7	IO_L40N_7/VREF_7	L32		
7	IO_L39P_7	K29		
7	IO_L39N_7	K30		
7	IO_L38P_7	P24		
7	IO_L38N_7	P25		
7	IO_L37P_7	J32		
7	IO_L37N_7	J33		
7	IO_L36P_7	J31		
7	IO_L36N_7	K31		
7	IO_L35P_7	N28		
7	IO_L35N_7	N29		
7	IO_L34P_7	H32		
7	IO_L34N_7/VREF_7	H33		
7	IO_L33P_7	H29		
7	IO_L33N_7	H30		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	GND	V16		
N/A	GND	U16		
N/A	GND	T16		
N/A	GND	R16		
N/A	GND	P16		
N/A	GND	J16		
N/A	GND	E16		
N/A	GND	A16		
N/A	GND	AA15		
N/A	GND	Y15		
N/A	GND	W15		
N/A	GND	V15		
N/A	GND	U15		
N/A	GND	T15		
N/A	GND	R15		
N/A	GND	P15		
N/A	GND	Y14		
N/A	GND	W14		
N/A	GND	V14		
N/A	GND	U14		
N/A	GND	T14		
N/A	GND	R14		
N/A	GND	AP13		
N/A	GND	AK13		
N/A	GND	AF13		
N/A	GND	J13		
N/A	GND	E13		
N/A	GND	A13		
N/A	GND	AE10		
N/A	GND	K10		
N/A	GND	AP9		
N/A	GND	AK9		
N/A	GND	AB9		
N/A	GND	W9		
N/A	GND	T9		
N/A	GND	N9		
N/A	GND	E9		
N/A	GND	A9		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GND	W18		
N/A	GND	V18		
N/A	GND	U18		
N/A	GND	T18		
N/A	GND	AD17		
N/A	GND	AC17		
N/A	GND	AB17		
N/A	GND	AA17		
N/A	GND	Y17		
N/A	GND	W17		
N/A	GND	V17		
N/A	GND	U17		
N/A	GND	P20		
N/A	GND	L20		
N/A	GND	G20		
N/A	GND	C20		
N/A	GND	AD19		
N/A	GND	AC19		
N/A	GND	AB19		
N/A	GND	AA19		
N/A	GND	Y19		
N/A	GND	W19		
N/A	GND	V19		
N/A	GND	U19		
N/A	GND	T19		
N/A	GND	AD18		
N/A	GND	AC18		
N/A	GND	U21		
N/A	GND	T21		
N/A	GND	AU20		
N/A	GND	AN20		
N/A	GND	AJ20		
N/A	GND	AF20		
N/A	GND	AD20		
N/A	GND	AC20		
N/A	GND	AB20		
N/A	GND	AA20		
N/A	GND	Y20		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	IO_L48N_1		J17		
1	IO_L48P_1		H17		
1	IO_L47N_1		K17		
1	IO_L47P_1		L17		
1	IO_L46N_1		M17		
1	IO_L46P_1		M18		
1	IO_L45N_1/VREF_1		F16		
1	IO_L45P_1		E16		
1	IO_L44N_1		G16		
1	IO_L44P_1		H16		
1	IO_L43N_1		K16		
1	IO_L43P_1		J16		
1	IO_L39N_1		M16		
1	IO_L39P_1		L16		
1	IO_L38N_1		C15		
1	IO_L38P_1		C14		
1	IO_L37N_1		F15		
1	IO_L37P_1		E15		
1	IO_L87N_1/VREF_1		J15	NC	
1	IO_L87P_1		H15	NC	
1	IO_L86N_1		K15	NC	
1	IO_L86P_1		L15	NC	
1	IO_L85N_1		E14	NC	
1	IO_L85P_1		D14	NC	
1	IO_L84N_1		G14	NC	
1	IO_L84P_1		F14	NC	
1	IO_L83_1/No_Pair		H14	NC	
1	IO_L78N_1		L14	NC	
1	IO_L78P_1		K14	NC	
1	IO_L36N_1/VREF_1		M14		
1	IO_L36P_1		M15		
1	IO_L35N_1		C13		
1	IO_L35P_1		D13		
1	IO_L34N_1		F13		
1	IO_L34P_1		E13		
1	IO_L30N_1		H13		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
4	IO_L60P_4		AR19		
4	IO_L64N_4		AV19		
4	IO_L64P_4		AU19		
4	IO_L65N_4		AW19		
4	IO_L65P_4		AY19		
4	IO_L66N_4		AL21		
4	IO_L66P_4/VREF_4		AL20		
4	IO_L67N_4		AN20		
4	IO_L67P_4		AM20		
4	IO_L68N_4		AP20		
4	IO_L68P_4		AR20		
4	IO_L69N_4		AV20		
4	IO_L69P_4/VREF_4		AU20		
4	IO_L73N_4		AY20		
4	IO_L73P_4		AW20		
4	IO_L74N_4/GCLK3S		AN21		
4	IO_L74P_4/GCLK2P		AP21		
4	IO_L75N_4/GCLK1S		AU21		
4	IO_L75P_4/GCLK0P		AT21		
5	IO_L75N_5/GCLK7S	BREFCLKN	AT22		
5	IO_L75P_5/GCLK6P	BREFCLKP	AU22		
5	IO_L74N_5/GCLK5S		AP22		
5	IO_L74P_5/GCLK4P		AN22		
5	IO_L73N_5		AW23		
5	IO_L73P_5		AY23		
5	IO_L69N_5/VREF_5		AU23		
5	IO_L69P_5		AV23		
5	IO_L68N_5		AR23		
5	IO_L68P_5		AP23		
5	IO_L67N_5		AM23		
5	IO_L67P_5		AN23		
5	IO_L66N_5/VREF_5		AL23		
5	IO_L66P_5		AL22		
5	IO_L65N_5		AY24		
5	IO_L65P_5		AW24		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	TXPPAD3		A36		
N/A	GNDA3		C35		
N/A	RXPPAD3		A35		
N/A	RXNPAD3		A34		
N/A	VTRXPAD3		B35		
N/A	AVCCAUXRX3		B34		
N/A	AVCCAUXTX4		B32		
N/A	VTTXPAD4		B33		
N/A	TXNPAD4		A33		
N/A	TXPPAD4		A32		
N/A	GNDA4		C31		
N/A	RXPPAD4		A31		
N/A	RXNPAD4		A30		
N/A	VTRXPAD4		B31		
N/A	AVCCAUXRX4		B30		
N/A	AVCCAUXTX5		B28		
N/A	VTTXPAD5		B29		
N/A	TXNPAD5		A29		
N/A	TXPPAD5		A28		
N/A	GNDA5		C27		
N/A	RXPPAD5		A27		
N/A	RXNPAD5		A26		
N/A	VTRXPAD5		B27		
N/A	AVCCAUXRX5		B26		
N/A	AVCCAUXTX6		B24		
N/A	VTTXPAD6		B25		
N/A	TXNPAD6		A25		
N/A	TXPPAD6		A24		
N/A	GNDA6		C22		
N/A	RXPPAD6		A23		
N/A	RXNPAD6		A22		
N/A	VTRXPAD6		B23		
N/A	AVCCAUXRX6		B22		
N/A	AVCCAUXTX7		B20		
N/A	VTTXPAD7		B21		
N/A	TXNPAD7		A21		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	TXPPAD11		A4		
N/A	GNDA11		C4		
N/A	RXPPAD11		A3		
N/A	RXNPAD11		A2		
N/A	VTRXPAD11		B3		
N/A	AVCCAUXRX11		B2		
N/A	AVCCAUXRX14		BA2		
N/A	VTRXPAD14		BA3		
N/A	RXNPAD14		BB2		
N/A	RXPPAD14		BB3		
N/A	GNDA14		AY4		
N/A	TXPPAD14		BB4		
N/A	TXNPAD14		BB5		
N/A	VTTXPAD14		BA5		
N/A	AVCCAUXTX14		BA4		
N/A	AVCCAUXRX15		BA6		
N/A	VTRXPAD15		BA7		
N/A	RXNPAD15		BB6		
N/A	RXPPAD15		BB7		
N/A	GNDA15		AY8		
N/A	TXPPAD15		BB8		
N/A	TXNPAD15		BB9		
N/A	VTTXPAD15		BA9		
N/A	AVCCAUXTX15		BA8		
N/A	AVCCAUXRX16		BA10		
N/A	VTRXPAD16		BA11		
N/A	RXNPAD16		BB10		
N/A	RXPPAD16		BB11		
N/A	GNDA16		AY12		
N/A	TXPPAD16		BB12		
N/A	TXNPAD16		BB13		
N/A	VTTXPAD16		BA13		
N/A	AVCCAUXTX16		BA12		
N/A	AVCCAUXRX17		BA14		
N/A	VTRXPAD17		BA15		
N/A	RXNPAD17		BB14		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
0	IO_L67P_0	J22	
0	IO_L68N_0	K23	
0	IO_L68P_0	L23	
0	IO_L69N_0	F22	
0	IO_L69P_0/VREF_0	G22	
0	IO_L73N_0	D22	
0	IO_L73P_0	E22	
0	IO_L74N_0/GCLK7P	K22	
0	IO_L74P_0/GCLK6S	L22	
0	IO_L75N_0/GCLK5P	B22	
0	IO_L75P_0/GCLK4S	C22	
1	IO_L75N_1/GCLK3P	C21	
1	IO_L75P_1/GCLK2S	B21	
1	IO_L74N_1/GCLK1P	L21	
1	IO_L74P_1/GCLK0S	K21	
1	IO_L73N_1	E21	
1	IO_L73P_1	D21	
1	IO_L69N_1/VREF_1	G21	
1	IO_L69P_1	F21	
1	IO_L68N_1	L20	
1	IO_L68P_1	K20	
1	IO_L67N_1	J21	
1	IO_L67P_1	H21	
1	IO_L66N_1/VREF_1	C20	
1	IO_L66P_1	B20	
1	IO_L65N_1	M20	
1	IO_L65P_1	M21	
1	IO_L64N_1	G20	
1	IO_L64P_1	F20	
1	IO_L60N_1	B19	
1	IO_L60P_1	A19	
1	IO_L59N_1	K19	
1	IO_L59P_1	J19	
1	IO_L58N_1	D19	
1	IO_L58P_1	D20	
1	IO_L57N_1/VREF_1	F19	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	VCCO_7	AA29	
7	VCCO_7	Y29	
7	VCCO_7	W29	
7	VCCO_7	V29	
7	VCCO_7	U29	
7	VCCO_7	T29	
7	VCCO_7	R29	
7	VCCO_7	AA28	
7	VCCO_7	Y28	
7	VCCO_7	W28	
7	VCCO_7	V28	
7	VCCO_7	U28	
7	VCCO_7	T28	
6	VCCO_6	AU39	
6	VCCO_6	AN39	
6	VCCO_6	AJ39	
6	VCCO_6	AD39	
6	VCCO_6	AW37	
6	VCCO_6	AN35	
6	VCCO_6	AJ35	
6	VCCO_6	AD35	
6	VCCO_6	AR33	
6	VCCO_6	AL33	
6	VCCO_6	AH29	
6	VCCO_6	AG29	
6	VCCO_6	AF29	
6	VCCO_6	AE29	
6	VCCO_6	AD29	
6	VCCO_6	AC29	
6	VCCO_6	AB29	
6	VCCO_6	AG28	
6	VCCO_6	AF28	
6	VCCO_6	AE28	
6	VCCO_6	AD28	
6	VCCO_6	AC28	
6	VCCO_6	AB28	
5	VCCO_5	AW33	