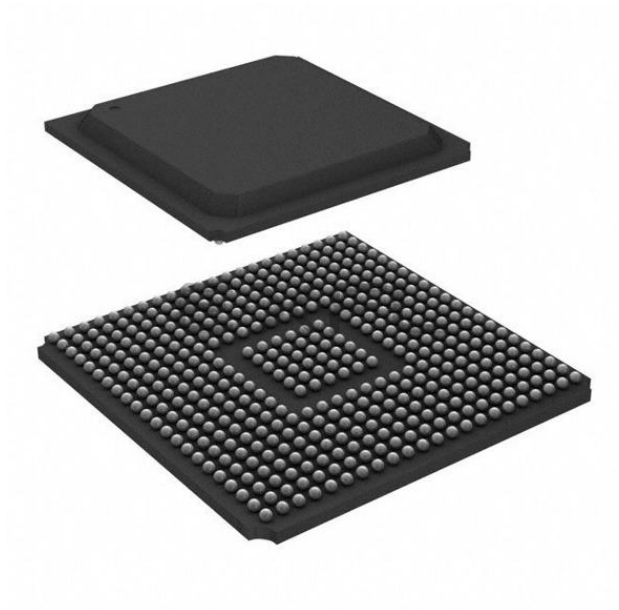

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	352
Number of Logic Elements/Cells	3168
Total RAM Bits	221184
Number of I/O	156
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp2-5fgg456i

3. NO_CHANGE

The NO_CHANGE option maintains the content of the output registers, regardless of the write operation. The clock edge during the write mode has no effect on the content of the data output register DO. When the port is configured as NO_CHANGE, only a read operation loads a new value in the output register DO, as shown in Figure 51.

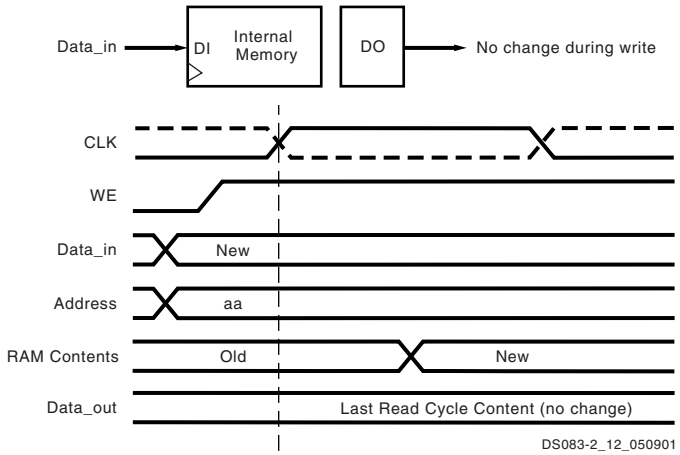

Figure 51: **NO_CHANGE Mode**

Control Pins and Attributes

Virtex-II Pro SelectRAM+ memory has two independent ports with the control signals described in Table 24. All control inputs including the clock have an optional inversion.

Table 24: **Control Functions**

Control Signal	Function
CLK	Read and Write Clock
EN	Enable affects Read, Write, Set, Reset
WE	Write Enable
SSR	Set DO register to SRVAL (attribute)

Initial memory content is determined by the INIT_xx attributes. Separate attributes determine the output register value after device configuration (INIT) and SSR is asserted (SRVAL). Both attributes (INIT_B and SRVAL) are available for each port when a block SelectRAM+ resource is configured as dual-port RAM.

Total Amount of SelectRAM+ Memory

Virtex-II Pro SelectRAM+ memory blocks are organized in multiple columns. The number of blocks per column depends on the row size, the number of Processor Blocks, and the number of RocketIO transceivers.

Table 25 shows the number of columns as well as the total amount of block SelectRAM+ memory available for each Virtex-II Pro device. The 18 Kb SelectRAM+ blocks are cascadable to implement deeper or wider single- or dual-port memory resources.

Table 25: **Virtex-II Pro SelectRAM+ Memory Available**

Device	Columns	Total SelectRAM+ Memory		
		Blocks	in Kb	in Bits
XC2VP2	4	12	216	221,184
XC2VP4	4	28	504	516,096
XC2VP7	6	44	792	811,008
XC2VP20	8	88	1,584	1,622,016
XC2VP30	8	136	2,448	2,506,752
XC2VPX20	8	88	1,584	1,622,016
XC2VP40	10	192	3,456	3,538,944
XC2VP50	12	232	4,176	4,276,224
XC2VP70	14	328	5,904	6,045,696
XC2VPX70	14	308	5,544	5,677,056
XC2VP100	16	444	7,992	8,183,808

Figure 52 shows the layout of the block RAM columns in the XC2VP4 device.

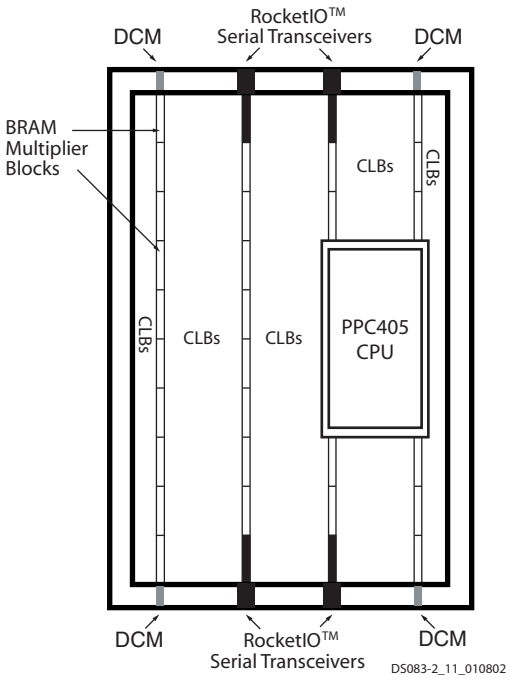

Figure 52: **XC2VP4 Block RAM Column Layout**

Date	Version	Revision
03/24/03	2.5.1	• Table 10: Corrected I/O standard names SSTL18_I and SSTL18_II to SSTL18_I_DCI and SSTL18_II_DCI respectively. • Figure 61, text below: Corrected wording of criteria for clock switching.
05/27/03	2.6	• Removed Compatible Output Standards and Compatible Input Standards tables. • Added new Table 12, Summary of Voltage Supply Requirements for All Input and Output Standards. This table replaces deleted I/O standards tables. • Corrected sentence in section Input/Output Individual Options, page 27, to read “The optional weak-keeper circuit is connected to each *user I/O pad*.” • Added section Rules for Combining I/O Standards in the Same Bank, page 29.
06/02/03	2.7	• Added four Differential Termination I/O standards to Table 9 and Table 12. • Added section On-Chip Differential Termination and Figure 31, page 34.
08/25/03	2.7.1	• Added footnote referring to XAPP659 to 3.3V I/O callouts in Table 8 and Table 12.
09/10/03	2.8	• Section Configuration, page 56: Added text indicating that the mode pins M0-M2 must be held to a constant DC level during and after configuration.
10/14/03	2.9	• Deleted section Functional Description: RocketIO Multi-Gigabit Transceiver (MGT), page 10. Added section Local Clocking, page 51. • Sections Slave-Serial Mode and Master-Serial Mode, page 56: Changed "rising" to "falling" edge with respect to DOUT. • Table 8, page 24 and Table 10, page 25: Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Section BUFGMUX, page 50: Corrected the definition of the "presently selected clock" to be I0 or I1. Corrected signal names in Figure 61 and associated text from CLK0 and CLK1 to I0 and I1.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
04/22/04	3.2	• Section Clock De-skew, page 52: Removed reference to CLK2X as an option for DCM clock feedback.
06/30/04	4.0	Merged in DS110-2 (Module 2 of Virtex-II Pro X data sheet). Separate RocketIO and RocketIO X sections created.
11/17/04	4.1	• Figure 11, page 12: Corrected figure by removing coupling capacitors from input. • Section Rules for Combining I/O Standards in the Same Bank, page 29: Corrected I/O standard in the first example from LVDS_25_DCI to LVDS_25.
03/01/05	4.2	• Reassigned heading hierarchies for better agreement with content. • Table 7: Corrected VCCAUXTX and VCCAUXRX to AVCCAUXTX and AVCCAUXRX respectively. • Table 9: Corrected V_{OD} (output voltage) range for LVDSEXT_25. • Table 25: Corrected SelectRAM+ memory available for XC2VPX70 device. • Table 33: Updated configuration default bitstream lengths.
06/20/05	4.3	*No changes in Module 2 for this revision.*
09/15/05	4.4	• Table 1: Deleted SONET OC-192 protocol. • Table 3: Deleted RocketIO X primitives for SONET OC-192, 10 Gbit Ethernet, and Xilinx 10G (Aurora) protocols. • Changed all instances of 10.3125 Gb/s to 6.25 Gb/s. • Table 7: Changed RocketIO X VCCAUXRX from 1.5V globally to 1.5V for 8B/10B encoding, 1.8V for all other encoding protocols.

Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics

DS083 (v5.0) June 21, 2011 **Product Specification**

Virtex-II Pro[1] Electrical Characteristics

Virtex™-II Pro devices are provided in -7, -6, and -5 speed grades, with -7 having the highest performance.

Virtex-II Pro DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -6 speed grade industrial device are the same as for a -6 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex-II Pro DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description[1]		Virtex-II Pro X	Virtex-II Pro	Units
V_{CCINT}	Internal supply voltage relative to GND		–0.5 to 1.6		V
V_{CCAUX}	Auxiliary supply voltage relative to GND		–0.5 to 3.0		V
V_{CCO}	Output drivers supply voltage relative to GND		–0.5 to 3.75		V
V_{BATT}	Key memory battery backup supply		–0.5 to 4.05		V
V_{REF}	Input reference voltage		–0.3 to 3.75		V
V_{IN}	3.3V I/O input voltage relative to GND (user and dedicated I/Os)		–0.3 to 4.05[3]		V
	2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)		–0.5 to V_{CCO} + 0.5		V
V_{TS}	Voltage applied to 3-state 3.3V output (user and dedicated I/Os)		–0.3 to 4.05[3]		V
	Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os)		–0.5 to V_{CCO} + 0.5		V
AVCCAUXRX	Receive auxilliary supply voltage relative to GNDA (analog ground)		–0.5 to 2.0	–0.5 to 3.0	V
AVCCAUXTX	Transmit auxilliary supply voltage relative to GNDA (analog ground)		–0.5 to 3.0	–0.5 to 3.0	V
V_{TRX}	Terminal receive supply voltage relative to GND		–0.5 to 3.0	–0.5 to 3.0	V
V_{TTX}	Terminal transmit supply voltage relative to GND		–0.5 to 1.6	–0.5 to 3.0	V
T_{STG}	Storage temperature (ambient)		–65 to +150		°C
T_{SOL}	Maximum soldering temperature[2]	All regular FG/FF flip-chip packages	+220		°C
		Pb-free FGG256 wire-bond package	N/A	+260	°C
		Pb-free FGG456 and FGG676 wire-bond packages	N/A	+250	°C
T_J	Maximum junction temperature[2]		+125		°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see the **Device Packaging and Thermal Characteristics Guide** information on the Xilinx website.
3. 3.3V I/O Absolute Maximum limit applied to DC and AC signals. Refer to **XAPP659** for more details.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

Table 35: **IOB Input Switching Characteristics *(Continued)***

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All	0.84/–0.61	0.86/–0.63	0.90/–0.67	ns, min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$	XC2VP2	2.28/–1.89	2.60/–2.15	2.95/–2.43	ns, max
		XC2VP4	2.55/–2.10	2.87/–2.36	3.21/–2.65	ns, max
		XC2VP7	2.48/–2.05	2.82/–2.32	3.15/–2.60	ns, max
		XC2VP20	2.63/–2.05	3.02/–2.35	3.40/–2.66	ns, max
		XC2VPX20	2.63/–2.05	3.02/–2.35	3.40/–2.66	ns, max
		XC2VP30	2.67/–2.07	3.09/–2.42	3.49/–2.73	ns, max
		XC2VP40	3.28/–2.56	3.61/–2.83	4.01/–3.15	ns, max
		XC2VP50	3.84/–3.02	4.08/–3.21	4.42/–3.48	ns, max
		XC2VP70	3.98/–3.13	4.23/–3.33	4.55/–3.58	ns, max
		XC2VPX70	3.98/–3.13	4.23/–3.33	4.55/–3.58	ns, max
		XC2VP100	N/A	6.48/–5.13	7.04/–5.57	ns, max
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All	0.39/ 0.01	0.44/ 0.01	0.49/ 0.01	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.52	0.57	0.75	ns, min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	1.13	1.27	1.42	ns, max
GSR to output IQ	T_{GSRQ}	All	5.87	6.75	7.43	ns, max

Notes:
1. Input timing for LVCMOS25 is measured at 1.25V. For other I/O standards, see Table 39.

DCM Timing Parameters

All devices are 100% functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions. All output jitter and phase specifications are determined through statistical measurement at the package pins.

Operating Frequency Ranges

Table 57: **Operating Frequency Ranges**

			Speed Grade			
Description	**Symbol**	**Constraints**	**-7**	**-6**	**-5**	**Units**
Output Clocks (Low Frequency Mode)						
CLK0, CLK90, CLK180, CLK270	CLKOUT_FREQ_1X_LF_MIN		24.00	24.00	24.00	MHz
	CLKOUT_FREQ_1X_LF_MAX		270.00	210.00	180.00	MHz
CLK2X, CLK2X180(5,6)	CLKOUT_FREQ_2X_LF_MIN		48.00	48.00	48.00	MHz
	CLKOUT_FREQ_2X_LF_MAX		450.00	420.00	360.00	MHz
CLKDV	CLKOUT_FREQ_DV_LF_MIN		1.50	1.50	1.50	MHz
	CLKOUT_FREQ_DV_LF_MAX		140.00	140.00	120.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_LF_MIN		24.00	24.00	24.00	MHz
	CLKOUT_FREQ_FX_LF_MAX		240.00	240.00	210.00	MHz
Input Clocks (Low Frequency Mode)						
CLKIN (using DLL outputs)(1,3,4)	CLKIN_FREQ_DLL_LF_MIN		24.00	24.00	24.00	MHz
	CLKIN_FREQ_DLL_LF_MAX		270.00	210.00	180.00	MHz
CLKIN (using CLKFX outputs)(2,3,4)	CLKIN_FREQ_FX_LF_MIN		1.00	1.00	1.00	MHz
	CLKIN_FREQ_FX_LF_MAX		240.00	240.00	210.00	MHz
PSCLK	PSCLK_FREQ_LF_MIN		0.01	0.01	0.01	MHz
	PSCLK_FREQ_LF_MAX		450.00	420.00	360.00	MHz
Output Clocks (High Frequency Mode)						
CLK0, CLK180(6)	CLKOUT_FREQ_1X_HF_MIN		48.00	48.00	48.00	MHz
	CLKOUT_FREQ_1X_HF_MAX		450.00	420.00	360.00	MHz
CLKDV	CLKOUT_FREQ_DV_HF_MIN		3.00	3.00	3.00	MHz
	CLKOUT_FREQ_DV_HF_MAX		280.00	280.00	240.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_HF_MIN		210.00	210.00	210.00	MHz
	CLKOUT_FREQ_FX_HF_MAX		320.00	320.00	270.00	MHz
Input Clocks (High Frequency Mode)						
CLKIN (using DLL outputs)(1,3,4,6)	CLKIN_FREQ_DLL_HF_MIN		48.00	48.00	48.00	MHz
	CLKIN_FREQ_DLL_HF_MAX		450.00	420.00	360.00	MHz
CLKIN (using CLKFX outputs)(2,3,4)	CLKIN_FREQ_FX_HF_MIN		50.00	50.00	50.00	MHz
	CLKIN_FREQ_FX_HF_MAX		320.00	320.00	270.00	MHz
PSCLK	PSCLK_FREQ_HF_MIN		0.01	0.01	0.01	MHz
	PSCLK_FREQ_HF_MAX		450.00	420.00	360.00	MHz

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If the CLKIN_DIVIDE_BY_2 attribute of the DCM is used, then double these values.
4. If the CLKIN_DIVIDE_BY_2 attribute of the DCM is used and CLKIN frequency > 400 MHz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).
5. CLK2X and CLK2X180 may not be used as the input to the CLKFB pin. See the ***Virtex-II Pro Platform FPGA User Guide*** for more information.
6. For the XC2VP100 -6 device only, clock macros for corner DCMS (X0Y0, X5Y0, X0Y1, X5Y1) are required to operate at maximum clock frequency. See **XAPP685** for implementation examples.

Table 67: **Example Pin-to-Pin Setup/Hold: Source-Synchronous Configuration**

Description	Symbol	Device	Speed Grade			Units
			–7	–6	–5	
Example Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin,(1) Using DCM and Global Clock Buffer. Values represent an 18-bit bus located in Banks 2, 3, 6, or 7 and grouped to one Horizontal Global Clock Line. TRACE must be used to determine the actual values for any given design. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25.						
No Delay Global Clock and IFF(2) with DCM	T_{PSDCM_0}/T_{PHDCM_0}	XC2VP2	0.23/0.39	0.21/0.42	0.21/0.42	ns
		XC2VP4	0.26/0.37	0.24/0.40	0.24/0.41	ns
		XC2VP7	0.18/ 0.36	0.18/ 0.40	0.18/ 0.41	ns
		XC2VP20	0.14/ 0.41	0.13/ 0.42	0.12/ 0.44	ns
		XC2VPX20	0.14/ 0.41	0.13/ 0.42	0.12/ 0.44	ns
		XC2VP30	0.29/ 0.25	0.31/ 0.24	0.31/ 0.24	ns
		XC2VP40	0.25/ 0.30	0.26/ 0.29	0.27/ 0.29	ns
		XC2VP50	0.18/ 0.36	0.18/ 0.38	0.17/ 0.39	ns
		XC2VP70	0.18/ 0.37	0.18/ 0.38	0.18/ 0.38	ns
		XC2VPX70	0.18/ 0.37	0.18/ 0.38	0.18/ 0.38	ns
		XC2VP100	N/A	0.18/ 0.33	0.19/ 0.37	ns

Notes:
1. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case duty-cycle distortion using CLK0 and CLK180, T_{DCD_CLK180}

   Package skew is not included in these measurements.
2. IFF = Input Flip-Flop

Source Synchronous Timing Budgets

This section describes how to use the parameters provided in the Source-Synchronous Switching Characteristics section to develop system-specific timing budgets. The following analysis provides information necessary for determining Virtex-II Pro contributions to an overall system timing analysis; no assumptions are made about the effects of Inter-Symbol Interference or PCB skew.

Virtex-II Pro Transmitter Data-Valid Window (T_X)

T_X is the minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

T_X = Data Period - [Jitter(1) + Duty Cycle Distortion(2) + TCKSKEW(3) + TPKGSKEW(4)]

Notes:
1. Jitter values and accumulation methodology to be provided in a future release of this document. The absolute period jitter values found in the DCM Timing Parameters section of the particular DCM output clock used to clock the IOB FF can be used for a best case analysis.
2. This value depends on the clocking methodology used. See Note1 for Table 64.
3. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
5	IO_L46N_5	W11			
5	IO_L46P_5	W10			
5	IO_L45N_5/VREF_5	AD9			
5	IO_L45P_5	AC9			
5	IO_L43N_5	AB9			
5	IO_L43P_5	AA9			
5	IO_L39N_5	Y9			
5	IO_L39P_5	W9			
5	IO_L37N_5	AF8			
5	IO_L37P_5	AE8			
5	IO_L09N_5/VREF_5	AB8			
5	IO_L09P_5	AA8			
5	IO_L07N_5/VREF_5	Y8			
5	IO_L07P_5	W8			
5	IO_L06N_5/VRP_5	AD7			
5	IO_L06P_5/VRN_5	AC7			
5	IO_L05_5/No_Pair	AB7			
5	IO_L03N_5/D4	AA7			
5	IO_L03P_5/D5	Y7			
5	IO_L02N_5/D6	AC6			
5	IO_L02P_5/D7	AB6			
5	IO_L01N_5/RDWR_B	AC5			
5	IO_L01P_5/CS_B	AB5			
6	IO_L01P_6/VRN_6	AE1			
6	IO_L01N_6/VRP_6	AD1			
6	IO_L02P_6	AD2			
6	IO_L02N_6	AC3			
6	IO_L03P_6	AC2			
6	IO_L03N_6/VREF_6	AC1			
6	IO_L05P_6	AB4			
6	IO_L05N_6	AA5			
6	IO_L06P_6	AB2			
6	IO_L06N_6	AB1			
6	IO_L23P_6	AA6	NC		

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
6	IO_L55P_6	T2			
6	IO_L55N_6	T1			
6	IO_L57P_6	R9			
6	IO_L57N_6/VREF_6	R8			
6	IO_L59P_6	R6			
6	IO_L59N_6	P6			
6	IO_L60P_6	R5			
6	IO_L60N_6	R4			
6	IO_L85P_6	R2			
6	IO_L85N_6	R1			
6	IO_L87P_6	P9			
6	IO_L87N_6/VREF_6	P8			
6	IO_L89P_6	P5			
6	IO_L89N_6	P4			
6	IO_L90P_6	P3			
6	IO_L90N_6	P2			
7	IO_L90P_7	N2			
7	IO_L90N_7	N3			
7	IO_L88P_7	N4			
7	IO_L88N_7/VREF_7	N5			
7	IO_L86P_7	N8			
7	IO_L86N_7	N9			
7	IO_L85P_7	M1			
7	IO_L85N_7	M2			
7	IO_L60P_7	M4			
7	IO_L60N_7	M5			
7	IO_L58P_7	N6			
7	IO_L58N_7/VREF_7	M6			
7	IO_L56P_7	M8			
7	IO_L56N_7	M9			
7	IO_L55P_7	L1			
7	IO_L55N_7	L2			
7	IO_L54P_7	L5			
7	IO_L54N_7	L6			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	AVCCAUXRX9	B4	NC	NC	
N/A	AVCCAUXRX16	AE4	NC	NC	
N/A	VTRXPAD16	AE5	NC	NC	
N/A	RXNPAD16	AF4	NC	NC	
N/A	RXPPAD16	AF5	NC	NC	
N/A	GNDA16	AD5	NC	NC	
N/A	TXPPAD16	AF6	NC	NC	
N/A	TXNPAD16	AF7	NC	NC	
N/A	VTTXPAD16	AE7	NC	NC	
N/A	AVCCAUXTX16	AE6	NC	NC	
N/A	AVCCAUXRX18	AE9			
N/A	VTRXPAD18	AE10			
N/A	RXNPAD18	AF9			
N/A	RXPPAD18	AF10			
N/A	GNDA18	AD11			
N/A	TXPPAD18	AF11			
N/A	TXNPAD18	AF12			
N/A	VTTXPAD18	AE12			
N/A	AVCCAUXTX18	AE11			
N/A	AVCCAUXTX4	B22	NC	NC	
N/A	VTTXPAD4	B23	NC	NC	
N/A	TXNPAD4	A23	NC	NC	
N/A	TXPPAD4	A22	NC	NC	
N/A	GNDA4	C22	NC	NC	
N/A	RXPPAD4	A21	NC	NC	
N/A	RXNPAD4	A20	NC	NC	
N/A	VTRXPAD4	B21	NC	NC	
N/A	AVCCAUXRX4	B20	NC	NC	
N/A	AVCCAUXTX6	B17			
N/A	VTTXPAD6	B18			
N/A	TXNPAD6	A18			
N/A	TXPPAD6	A17			
N/A	GNDA6	C16			
N/A	RXPPAD6	A16			
N/A	RXNPAD6	A15			
N/A	VTRXPAD6	B16			
N/A	AVCCAUXRX6	B15			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L38N_2	N10				
2	IO_L38P_2	N9				
2	IO_L39N_2	M7				
2	IO_L39P_2	M6				
2	IO_L40N_2/VREF_2	L2				
2	IO_L40P_2	M2				
2	IO_L41N_2	N8				
2	IO_L41P_2	N7				
2	IO_L42N_2	L4				
2	IO_L42P_2	L3				
2	IO_L43N_2	M4				
2	IO_L43P_2	M3				
2	IO_L44N_2	P10				
2	IO_L44P_2	P9				
2	IO_L45N_2	N6				
2	IO_L45P_2	N5				
2	IO_L46N_2/VREF_2	M1				
2	IO_L46P_2	N1				
2	IO_L47N_2	P8				
2	IO_L47P_2	P7				
2	IO_L48N_2	N4				
2	IO_L48P_2	N3				
2	IO_L49N_2	N2				
2	IO_L49P_2	P2				
2	IO_L50N_2	R10				
2	IO_L50P_2	R9				
2	IO_L51N_2	P6				
2	IO_L51P_2	P5				
2	IO_L52N_2/VREF_2	P4				
2	IO_L52P_2	P3				
2	IO_L53N_2	T11				
2	IO_L53P_2	U11				
2	IO_L54N_2	R7				
2	IO_L54P_2	R6				
2	IO_L55N_2	P1				
2	IO_L55P_2	R1				
2	IO_L56N_2	T10				
2	IO_L56P_2	T9				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	TXPPAD17	AP12	NC	NC	NC	
N/A	TXNPAD17	AP13	NC	NC	NC	
N/A	VTTXPAD17	AN13	NC	NC	NC	
N/A	AVCCAUXTX17	AN12	NC	NC	NC	
N/A	AVCCAUXRX18	AN14				
N/A	VTRXPAD18	AN15				
N/A	RXNPAD18	AP14				
N/A	RXPPAD18	AP15				
N/A	GNDA18	AM15				
N/A	TXPPAD18	AP16				
N/A	TXNPAD18	AP17				
N/A	VTTXPAD18	AN17				
N/A	AVCCAUXTX18	AN16				
N/A	AVCCAUXRX19	AN18				
N/A	VTRXPAD19	AN19				
N/A	RXNPAD19	AP18				
N/A	RXPPAD19	AP19				
N/A	GNDA19	AM20				
N/A	TXPPAD19	AP20				
N/A	TXNPAD19	AP21				
N/A	VTTXPAD19	AN21				
N/A	AVCCAUXTX19	AN20				
N/A	AVCCAUXRX20	AN22	NC	NC	NC	
N/A	VTRXPAD20	AN23	NC	NC	NC	
N/A	RXNPAD20	AP22	NC	NC	NC	
N/A	RXPPAD20	AP23	NC	NC	NC	
N/A	GNDA20	AM23	NC	NC	NC	
N/A	TXPPAD20	AP24	NC	NC	NC	
N/A	TXNPAD20	AP25	NC	NC	NC	
N/A	VTTXPAD20	AN25	NC	NC	NC	
N/A	AVCCAUXTX20	AN24	NC	NC	NC	
N/A	AVCCAUXRX21	AN26				
N/A	VTRXPAD21	AN27				
N/A	RXNPAD21	AP26				
N/A	RXPPAD21	AP27				
N/A	GNDA21	AM27				
N/A	TXPPAD21	AP28				
N/A	TXNPAD21	AP29				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
4	IO_L02P_4/D1	AE11		
4	IO_L03N_4/D2	AM10		
4	IO_L03P_4/D3	AL10		
4	IO_L05_4/No_Pair	AH10		
4	IO_L06N_4/VRP_4	AP10		
4	IO_L06P_4/VRN_4	AN10		
4	IO_L07N_4	AH11		
4	IO_L07P_4/VREF_4	AH12		
4	IO_L08N_4	AG12		
4	IO_L08P_4	AG13		
4	IO_L09N_4	AK11		
4	IO_L09P_4/VREF_4	AJ11		
4	IO_L19N_4	AM11		
4	IO_L19P_4	AM12		
4	IO_L20N_4	AF12		
4	IO_L20P_4	AE12		
4	IO_L21N_4	AP11		
4	IO_L21P_4	AN11		
4	IO_L25N_4	AK12		
4	IO_L25P_4	AJ12		
4	IO_L26N_4	AE13		
4	IO_L26P_4	AD13		
4	IO_L27N_4	AL12		
4	IO_L27P_4/VREF_4	AL13		
4	IO_L37N_4	AP12		
4	IO_L37P_4	AN12		
4	IO_L38N_4	AF14		
4	IO_L38P_4	AF15		
4	IO_L39N_4	AJ13		
4	IO_L39P_4	AH13		
4	IO_L43N_4	AN13		
4	IO_L43P_4	AM13		
4	IO_L44N_4	AE14		
4	IO_L44P_4	AD14		
4	IO_L45N_4	AH14		
4	IO_L45P_4/VREF_4	AG14		
4	IO_L46N_4	AK14		
4	IO_L46P_4	AJ14		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	GND	AF30		
N/A	GND	AB30		
N/A	GND	W30		
N/A	GND	T30		
N/A	GND	N30		
N/A	GND	J30		
N/A	GND	E30		
N/A	GND	A30		
N/A	GND	AP26		
N/A	GND	AK26		
N/A	GND	AB26		
N/A	GND	W26		
N/A	GND	T26		
N/A	GND	N26		
N/A	GND	E26		
N/A	GND	A26		
N/A	GND	AE25		
N/A	GND	K25		
N/A	GND	AP22		
N/A	GND	AK22		
N/A	GND	AF22		
N/A	GND	J22		
N/A	GND	E22		
N/A	GND	A22		
N/A	GND	Y21		
N/A	GND	W21		
N/A	GND	V21		
N/A	GND	U21		
N/A	GND	T21		
N/A	GND	R21		
N/A	GND	AA20		
N/A	GND	Y20		
N/A	GND	W20		
N/A	GND	V20		
N/A	GND	U20		
N/A	GND	T20		
N/A	GND	R20		
N/A	GND	P20		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
1	IO_L36N_1/VREF_1	E13	NC	
1	IO_L36P_1	D13	NC	
1	IO_L35N_1	K15	NC	
1	IO_L35P_1	J15	NC	
1	IO_L34N_1	G13	NC	
1	IO_L34P_1	F12	NC	
1	IO_L30N_1	J13	NC	
1	IO_L30P_1	H13	NC	
1	IO_L29N_1	L15	NC	
1	IO_L29P_1	L14	NC	
1	IO_L28N_1	E12	NC	
1	IO_L28P_1	D12	NC	
1	IO_L27N_1/VREF_1	J12		
1	IO_L27P_1	H12		
1	IO_L26N_1	K14		
1	IO_L26P_1	J14		
1	IO_L25N_1	D11		
1	IO_L25P_1	C11		
1	IO_L21N_1	F11		
1	IO_L21P_1	E11		
1	IO_L20N_1	M14		
1	IO_L20P_1	M13		
1	IO_L19N_1	H11		
1	IO_L19P_1	G11		
1	IO_L09N_1/VREF_1	J11		
1	IO_L09P_1	J10		
1	IO_L08N_1	L13		
1	IO_L08P_1	L12		
1	IO_L07N_1	D10		
1	IO_L07P_1	C10		
1	IO_L06N_1	F10		
1	IO_L06P_1	E10		
1	IO_L05_1/No_Pair	K10		
1	IO_L03N_1/VREF_1	H10		
1	IO_L03P_1	G10		
1	IO_L02N_1	K12		
1	IO_L02P_1	K11		
1	IO_L01N_1/VRP_1	E9		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L30N_2	N6		
2	IO_L30P_2	N7		
2	IO_L31N_2	M4		
2	IO_L31P_2	N5		
2	IO_L32N_2	R11		
2	IO_L32P_2	R12		
2	IO_L33N_2	N1		
2	IO_L33P_2	N2		
2	IO_L34N_2/VREF_2	P6		
2	IO_L34P_2	P7		
2	IO_L35N_2	R13		
2	IO_L35P_2	T13		
2	IO_L36N_2	P4		
2	IO_L36P_2	P5		
2	IO_L37N_2	P3		
2	IO_L37P_2	N3		
2	IO_L38N_2	T10		
2	IO_L38P_2	T11		
2	IO_L39N_2	P1		
2	IO_L39P_2	P2		
2	IO_L40N_2/VREF_2	R7		
2	IO_L40P_2	R8		
2	IO_L41N_2	T12		
2	IO_L41P_2	U12		
2	IO_L42N_2	R5		
2	IO_L42P_2	R6		
2	IO_L43N_2	R3		
2	IO_L43P_2	R4		
2	IO_L44N_2	U8		
2	IO_L44P_2	T8		
2	IO_L45N_2	R1		
2	IO_L45P_2	R2		
2	IO_L46N_2/VREF_2	T6		
2	IO_L46P_2	T7		
2	IO_L47N_2	U9		
2	IO_L47P_2	U10		
2	IO_L48N_2	T2		
2	IO_L48P_2	T3		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
4	IO_L03N_4/D2	AN10		
4	IO_L03P_4/D3	AM10		
4	IO_L05_4/No_Pair	AK10		
4	IO_L06N_4/VRP_4	AR10		
4	IO_L06P_4/VRN_4	AP10		
4	IO_L07N_4	AU10		
4	IO_L07P_4/VREF_4	AT10		
4	IO_L08N_4	AJ12		
4	IO_L08P_4	AJ13		
4	IO_L09N_4	AL10		
4	IO_L09P_4/VREF_4	AL11		
4	IO_L19N_4	AN11		
4	IO_L19P_4	AM11		
4	IO_L20N_4	AH13		
4	IO_L20P_4	AH14		
4	IO_L21N_4	AR11		
4	IO_L21P_4	AP11		
4	IO_L25N_4	AU11		
4	IO_L25P_4	AT11		
4	IO_L26N_4	AL14		
4	IO_L26P_4	AK14		
4	IO_L27N_4	AM12		
4	IO_L27P_4/VREF_4	AL12		
4	IO_L28N_4	AT12	NC	
4	IO_L28P_4	AR12	NC	
4	IO_L29N_4	AJ14	NC	
4	IO_L29P_4	AJ15	NC	
4	IO_L30N_4	AM13	NC	
4	IO_L30P_4	AL13	NC	
4	IO_L34N_4	AP12	NC	
4	IO_L34P_4	AN13	NC	
4	IO_L35N_4	AL15	NC	
4	IO_L35P_4	AK15	NC	
4	IO_L36N_4	AT13	NC	
4	IO_L36P_4/VREF_4	AR13	NC	
4	IO_L37N_4	AN14		
4	IO_L37P_4	AM14		
4	IO_L38N_4	AH15		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GND	W18		
N/A	GND	V18		
N/A	GND	U18		
N/A	GND	T18		
N/A	GND	AD17		
N/A	GND	AC17		
N/A	GND	AB17		
N/A	GND	AA17		
N/A	GND	Y17		
N/A	GND	W17		
N/A	GND	V17		
N/A	GND	U17		
N/A	GND	P20		
N/A	GND	L20		
N/A	GND	G20		
N/A	GND	C20		
N/A	GND	AD19		
N/A	GND	AC19		
N/A	GND	AB19		
N/A	GND	AA19		
N/A	GND	Y19		
N/A	GND	W19		
N/A	GND	V19		
N/A	GND	U19		
N/A	GND	T19		
N/A	GND	AD18		
N/A	GND	AC18		
N/A	GND	U21		
N/A	GND	T21		
N/A	GND	AU20		
N/A	GND	AN20		
N/A	GND	AJ20		
N/A	GND	AF20		
N/A	GND	AD20		
N/A	GND	AC20		
N/A	GND	AB20		
N/A	GND	AA20		
N/A	GND	Y20		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	TXPPAD11		A4		
N/A	GNDA11		C4		
N/A	RXPPAD11		A3		
N/A	RXNPAD11		A2		
N/A	VTRXPAD11		B3		
N/A	AVCCAUXRX11		B2		
N/A	AVCCAUXRX14		BA2		
N/A	VTRXPAD14		BA3		
N/A	RXNPAD14		BB2		
N/A	RXPPAD14		BB3		
N/A	GNDA14		AY4		
N/A	TXPPAD14		BB4		
N/A	TXNPAD14		BB5		
N/A	VTTXPAD14		BA5		
N/A	AVCCAUXTX14		BA4		
N/A	AVCCAUXRX15		BA6		
N/A	VTRXPAD15		BA7		
N/A	RXNPAD15		BB6		
N/A	RXPPAD15		BB7		
N/A	GNDA15		AY8		
N/A	TXPPAD15		BB8		
N/A	TXNPAD15		BB9		
N/A	VTTXPAD15		BA9		
N/A	AVCCAUXTX15		BA8		
N/A	AVCCAUXRX16		BA10		
N/A	VTRXPAD16		BA11		
N/A	RXNPAD16		BB10		
N/A	RXPPAD16		BB11		
N/A	GNDA16		AY12		
N/A	TXPPAD16		BB12		
N/A	TXNPAD16		BB13		
N/A	VTTXPAD16		BA13		
N/A	AVCCAUXTX16		BA12		
N/A	AVCCAUXRX17		BA14		
N/A	VTRXPAD17		BA15		
N/A	RXNPAD17		BB14		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		E22		
N/A	GND		E21		
N/A	GND		E5		
N/A	GND		D39		
N/A	GND		D32		
N/A	GND		D28		
N/A	GND		D15		
N/A	GND		D11		
N/A	GND		D4		
N/A	GND		C42		
N/A	GND		C41		
N/A	GND		C40		
N/A	GND		C3		
N/A	GND		C2		
N/A	GND		C1		
N/A	GND		B42		
N/A	GND		B1		
N/A	GND		N14		
N/A	GND		N29		
N/A	GND		AK14		
N/A	GND		AK29		
N/A	GND		P13		
N/A	GND		P30		
N/A	GND		AJ13		
N/A	GND		AJ30		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD22	
N/A	GND	AC22	
N/A	GND	AB22	
N/A	GND	AA22	
N/A	GND	Y22	
N/A	GND	W22	
N/A	GND	V22	
N/A	GND	U22	
N/A	GND	AF21	
N/A	GND	AE21	
N/A	GND	AD21	
N/A	GND	AC21	
N/A	GND	AB21	
N/A	GND	AA21	
N/A	GND	Y21	
N/A	GND	W21	
N/A	GND	V21	
N/A	GND	U21	
N/A	GND	BB20	
N/A	GND	AV20	
N/A	GND	AP20	
N/A	GND	AF20	
N/A	GND	AE20	
N/A	GND	AD20	
N/A	GND	AC20	
N/A	GND	AB20	
N/A	GND	AA20	
N/A	GND	Y20	
N/A	GND	W20	
N/A	GND	V20	
N/A	GND	U20	
N/A	GND	J20	
N/A	GND	E20	
N/A	GND	A20	
N/A	GND	AL19	
N/A	GND	AF19	
N/A	GND	AE19	