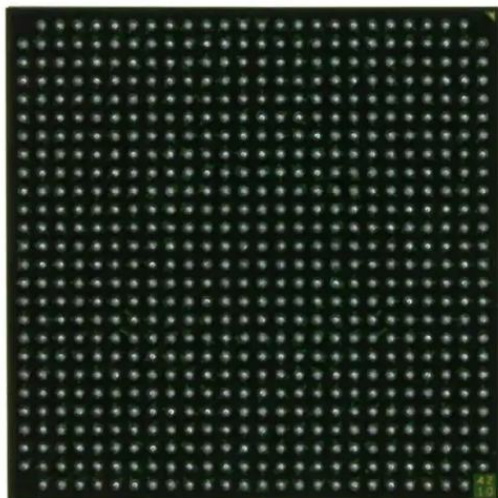




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

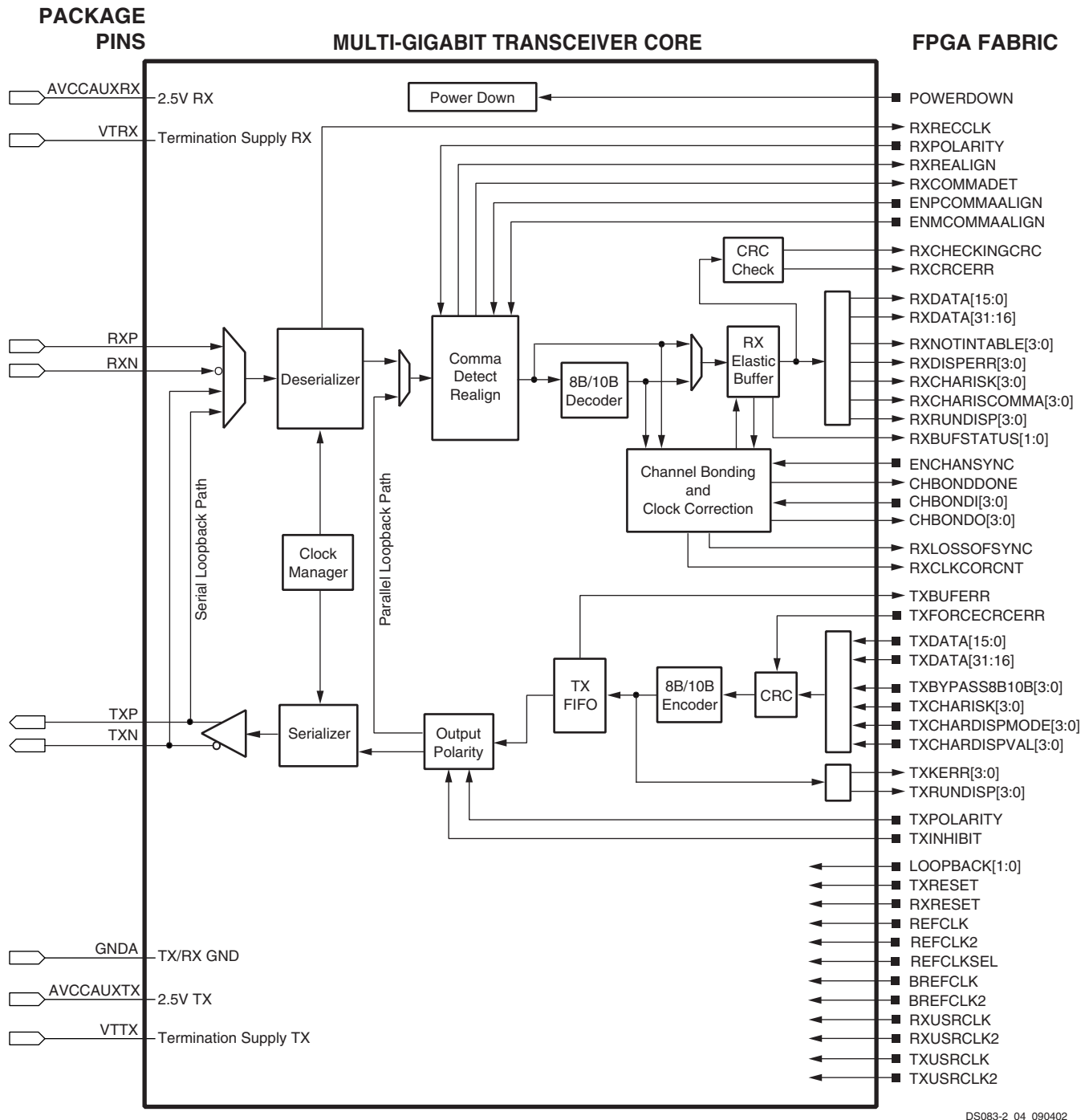
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	352
Number of Logic Elements/Cells	3168
Total RAM Bits	221184
Number of I/O	204
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp2-6ffg672c



DS083-2_04_090402

Figure 10: RocketIO Transceiver Block Diagram

Output Swing and Pre-emphasis

The output swing and pre-emphasis levels of the RocketIO MGTs are fully programmable. Each is controlled via attributes at configuration, but can be modified via partial reconfiguration.

The programmable output swing control can adjust the differential output level between 400 mV and 800 mV in four increments of 100 mV.

With pre-emphasis, the differential voltage swing is boosted to create a stronger rising waveform. This method compensates for high-frequency loss in the transmission media that would otherwise limit the magnitude of this waveform. Lossy transmission lines cause the dissipation of electrical energy. This pre-emphasis technique extends the distance that signals can be driven down lossy line media and increases the signal-to-noise ratio at the receiver.

- The double lines route signals to every first or second block away in all four directions. Organized in a staggered pattern, double lines can be driven only at their endpoints. Double-line signals can be accessed either at the endpoints or at the midpoint (one block from the source).
- The direct connect lines route signals to neighboring blocks: vertically, horizontally, and diagonally.
- The fast connect lines are the internal CLB local interconnections from LUT outputs to LUT inputs.
- Horizontal routing resources are provided for on-chip 3-state buses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row. (See [3-State Buffers](#), page 43.)
- Two dedicated carry-chain resources per slice column (two per CLB column) propagate carry-chain MUXCY output signals vertically to the adjacent slice. (See [CLB/Slice Configurations](#), page 44.)
- One dedicated SOP chain per slice row (two per CLB row) propagate ORCY output logic signals horizontally to the adjacent slice. (See [Sum of Products](#), page 42.)
- One dedicated shift-chain per CLB connects the output of LUTs in shift-register mode to the input of the next LUT in shift-register mode (vertically) inside the CLB. (See [Shift Registers](#), page 39.)

Dedicated Routing

In addition to the global and local routing resources, dedicated signals are available.

- There are eight global clock nets per quadrant. (See [Global Clock Multiplexer Buffers](#), page 48.)

Table 17: Processor Block Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Setup and Hold Relative to Clock (CPMC405CLOCK)					
Device Control Register Bus control inputs	T _{P_{CC}K_DCR} /T _{P_{CK}C_DCR}	0.38/−0.18	0.44/−0.20	0.48/−0.23	ns, min
Device Control Register Bus data inputs	T _{P_{DC}K_DCR} /T _{P_{CK}D_DCR}	0.65/−0.01	0.75/−0.01	0.82/−0.02	ns, min
Clock and Power Management control inputs	T _{P_{CC}K_CPM} /T _{P_{CK}C_CPM}	0.16/ 0.03	0.19/ 0.03	0.20/ 0.03	ns, min
Reset control inputs	T _{P_{CC}K_RST} /T _{P_{CK}C_RST}	0.16/ 0.03	0.19/ 0.03	0.20/ 0.03	ns, min
Debug control inputs	T _{P_{CC}K_DBG} /T _{P_{CK}C_DBG}	0.27/ 0.30	0.31/ 0.35	0.34/ 0.38	ns, min
Trace control inputs	T _{P_{CC}K_TRC} /T _{P_{CK}C_TRC}	1.37/−0.41	1.57/−0.48	1.73/−0.52	ns, min
External Interrupt Controller control inputs	T _{P_{CC}K_EIC} /T _{P_{CK}C_EIC}	0.57/−0.22	0.66/−0.25	0.72/−0.27	ns, min
Clock to Out					
Device Control Register Bus control outputs	T _{P_{CK}CO_DCR}	1.32	1.52	1.67	ns, max
Device Control Register Bus address outputs	T _{P_{CK}AO_DCR}	1.72	1.98	2.17	ns, max
Device Control Register Bus data outputs	T _{P_{CK}DO_DCR}	1.76	2.02	2.22	ns, max
Clock and Power Management control outputs	T _{P_{CK}CO_CPM}	1.26	1.45	1.59	ns, max
Reset control outputs	T _{P_{CK}CO_RST}	1.32	1.51	1.66	ns, max
Debug control outputs	T _{P_{CK}CO_DBG}	1.94	2.22	2.44	ns, max
Trace control outputs	T _{P_{CK}CO_TRC}	1.35	1.56	1.71	ns, max
Clock					
CPMC405CLOCK minimum pulse width, high	T _{CPWH}	1.25	1.42	1.66	ns, min
CPMC405CLOCK minimum pulse width, low	T _{CPWL}	1.25	1.42	1.66	ns, min

Table 18: Processor Block PLB Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Setup and Hold Relative to Clock (PLBCLK)					
Processor Local Bus(ICU/DCU) control inputs	T _{PCCK} _PLB/T _{PCKC} _PLB	0.98/ 0.18	1.12/ 0.21	1.23/ 0.23	ns, min
Processor Local Bus (ICU/DCU) data inputs	T _{PDCK} _PLB/T _{PCKD} _PLB	0.62/ 0.16	0.71/ 0.18	0.78/ 0.20	ns, min
Clock to Out					
Processor Local Bus(ICU/DCU) control outputs	T _{PCKCO} _PLB	1.34	1.54	1.69	ns, max
Processor Local Bus(ICU/DCU) address bus outputs	T _{PCKAO} _PLB	1.16	1.34	1.47	ns, max
Processor Local Bus(ICU/DCU) data bus outputs	T _{PCKDO} _PLB	1.44	1.65	1.81	ns, max

Table 35: IOB Input Switching Characteristics (Continued)

			Speed Grade			
Description	Symbol	Device	-7	-6	-5	Units
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	$T_{IOIPICK}/T_{IOICKP}$	All	0.84/−0.61	0.86/−0.63	0.90/−0.67	ns, min
Pad, with delay	$T_{IOIPICKD}/T_{IOICKPD}$	XC2VP2	2.28/−1.89	2.60/−2.15	2.95/−2.43	ns, max
		XC2VP4	2.55/−2.10	2.87/−2.36	3.21/−2.65	ns, max
		XC2VP7	2.48/−2.05	2.82/−2.32	3.15/−2.60	ns, max
		XC2VP20	2.63/−2.05	3.02/−2.35	3.40/−2.66	ns, max
		XC2VPX20	2.63/−2.05	3.02/−2.35	3.40/−2.66	ns, max
		XC2VP30	2.67/−2.07	3.09/−2.42	3.49/−2.73	ns, max
		XC2VP40	3.28/−2.56	3.61/−2.83	4.01/−3.15	ns, max
		XC2VP50	3.84/−3.02	4.08/−3.21	4.42/−3.48	ns, max
		XC2VP70	3.98/−3.13	4.23/−3.33	4.55/−3.58	ns, max
		XC2VPX70	3.98/−3.13	4.23/−3.33	4.55/−3.58	ns, max
	XC2VP100	N/A	6.48/−5.13	7.04/−5.57	ns, max	
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All	0.39/ 0.01	0.44/ 0.01	0.49/ 0.01	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.52	0.57	0.75	ns, min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	1.13	1.27	1.42	ns, max
GSR to output IQ	T_{GSRQ}	All	5.87	6.75	7.43	ns, max

Notes:

1. Input timing for LVCMOS25 is measured at 1.25V. For other I/O standards, see [Table 39](#).

IOB Input Switching Characteristics Standard Adjustments

Table 36 gives all standard-specific data input delay adjustments.

Table 36: IOB Input Switching Characteristics Standard Adjustments

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	$T_{ILVTTTL}$	0.07	0.08	0.09	ns
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	$T_{ILVCMOS33}$	0.04	0.05	0.05	ns
LVC MOS, 2.5V	LVC MOS25	$T_{ILVCMOS25}$	0.00	0.00	0.00	ns
LVC MOS, 1.8V	LVC MOS18	$T_{ILVCMOS18}$	0.29	0.33	0.36	ns
LVC MOS, 1.5V	LVC MOS15	$T_{ILVCMOS15}$	0.36	0.41	0.45	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{ILVDS_25}	0.31	0.36	0.40	ns
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	$T_{ILVDSEXT_25}$	0.33	0.37	0.41	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{IULVDS_25}	0.31	0.36	0.40	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{IBLVDS_25}	0.00	0.00	0.00	ns
LDT (HyperTransport), 2.5V	LDT_25	$T_{ILD T_25}$	0.31	0.36	0.40	ns
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	$T_{ILVPECL_25}$	0.69	0.80	0.88	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{IPCI33_3}	0.14	0.16	0.18	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{IPCI66_3}	0.15	0.17	0.19	ns
PCI-X, 133 MHz, 3.3V	PCIX	T_{IPCIX}	0.12	0.13	0.15	ns
GTL (Gunning Transceiver Logic)	GTL	T_{IGTL}	0.59	0.68	0.74	ns
GTL Plus	GTLP	T_{IGTLP}	0.63	0.72	0.79	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{IHSTL_I}	0.59	0.68	0.75	ns
HSTL, Class II	HSTL_II	T_{IHSTL_II}	0.59	0.68	0.75	ns
HSTL, Class III	HSTL_III	T_{IHSTL_III}	0.57	0.66	0.72	ns
HSTL, Class IV	HSTL_IV	T_{IHSTL_IV}	0.58	0.67	0.74	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{IHSTL_I_18}$	0.57	0.65	0.72	ns
HSTL, Class II, 1.8V	HSTL_II_18	$T_{IHSTL_II_18}$	0.55	0.63	0.69	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{IHSTL_III_18}$	0.56	0.64	0.70	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{IHSTL_IV_18}$	0.57	0.65	0.71	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{ISSTL18_I}$	0.62	0.72	0.79	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{ISSTL18_II}$	0.64	0.73	0.81	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{ISSTL2_I}	0.62	0.72	0.79	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{ISSTL2_II}	0.64	0.73	0.81	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{ILVDCI_33}	-0.05	-0.05	-0.06	ns
LVDCI, 2.5V	LVDCI_25	T_{ILVDCI_25}	0.00	0.00	0.00	ns
LVDCI, 1.8V	LVDCI_18	T_{ILVDCI_18}	0.07	0.09	0.09	ns
LVDCI, 1.5V	LVDCI_15	T_{ILVDCI_15}	0.13	0.15	0.17	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{ILVDCI_DV2_25}$	0.00	0.00	0.00	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{ILVDCI_DV2_18}$	0.07	0.09	0.09	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{ILVDCI_DV2_15}$	0.13	0.15	0.17	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{IHSLVDCI_15}$	0.59	0.68	0.75	ns

Virtex-II Pro Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVCMOS25 Standard, *With DCM*

Table 55: Global Clock Set-Up and Hold for LVCMOS25 Standard, With DCM

			Speed Grade			
Description	Symbol	Device	-7	-6	-5	Units
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾ For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25 .						
No Delay Global Clock and IFF ⁽²⁾ with DCM	T _{PSDCM} /T _{PHDCM}	XC2VP2	1.54/–0.58	1.54/–0.57	1.54/–0.56	ns
		XC2VP4	1.59/–0.59	1.59/–0.58	1.59/–0.57	ns
		XC2VP7	1.66/–0.61	1.66/–0.59	1.66/–0.57	ns
		XC2VP20	1.68/–0.53	1.68/–0.53	1.68/–0.50	ns
		XC2VPX20	1.68/–0.53	1.68/–0.53	1.68/–0.50	ns
		XC2VP30	1.81/–0.74	1.81/–0.74	1.81/–0.71	ns
		XC2VP40	1.85/–0.65	1.85/–0.64	1.85/–0.60	ns
		XC2VP50	1.85/–0.57	1.85/–0.54	1.85/–0.50	ns
		XC2VP70	1.86/–0.45	1.86/–0.39	1.86/–0.30	ns
		XC2VPX70	1.86/–0.45	1.86/–0.39	1.86/–0.30	ns
		XC2VP100	N/A	1.86/–0.35	1.87/–0.28	ns

Notes:

- Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
- These measurements include:
 - CLK0 and CLK180 DCM jitter
 - Worst-case duty-cycle distortion using CLK0 and CLK180, T_{DCD_CLK180} .
- IFF = Input Flip-Flop or Latch

FF672 Flip-Chip Fine-Pitch BGA Package

As shown in [Table 8](#), XC2VP2, XC2VP4, and XC2VP7 Virtex-II Pro devices are available in the FF672 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for differences shown in the "No Connects" column. Following this table are the [FF672 Flip-Chip Fine-Pitch BGA Package Specifications \(1.00mm pitch\)](#).

Table 8: FF672 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L01N_0/VRP_0	B24			
0	IO_L01P_0/VRN_0	A24			
0	IO_L02N_0	D21			
0	IO_L02P_0	C21			
0	IO_L03N_0	E20			
0	IO_L03P_0/VREF_0	D20			
0	IO_L05_0/No_Pair	F19			
0	IO_L06N_0	E19			
0	IO_L06P_0	E18			
0	IO_L07N_0	D19			
0	IO_L07P_0	C19			
0	IO_L08N_0	B19			
0	IO_L08P_0	A19			
0	IO_L09N_0	G18			
0	IO_L09P_0/VREF_0	F18			
0	IO_L37N_0	D18	NC	NC	
0	IO_L37P_0	C18	NC	NC	
0	IO_L38N_0	G17	NC	NC	
0	IO_L38P_0	H16	NC	NC	
0	IO_L39N_0	F17	NC	NC	
0	IO_L39P_0	F16	NC	NC	
0	IO_L43N_0	E17	NC	NC	
0	IO_L43P_0	D17	NC	NC	
0	IO_L44N_0	G16	NC	NC	
0	IO_L44P_0	G15	NC	NC	
0	IO_L45N_0	E16	NC	NC	
0	IO_L45P_0/VREF_0	D16	NC	NC	
0	IO_L67N_0	F15			
0	IO_L67P_0	E15			
0	IO_L68N_0	D15			
0	IO_L68P_0	C15			
0	IO_L69N_0	H15			
0	IO_L69P_0/VREF_0	H14			

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	TXPPAD19		AK19			
N/A	TXNPAD19		AK20			
N/A	VTTXPAD19		AJ20			
N/A	AVCCAUXTX19		AJ19			
N/A	AVCCAUXRX21		AJ24			
N/A	VTRXPAD21		AJ25			
N/A	RXNPAD21		AK24			
N/A	RXPPAD21		AK25			
N/A	GNDA21		AH25			
N/A	TXPPAD21		AK26			
N/A	TXNPAD21		AK27			
N/A	VTTXPAD21		AJ27			
N/A	AVCCAUXTX21		AJ26			
N/A	VCCAUX		AK29			
N/A	VCCAUX		AK16			
N/A	VCCAUX		AK15			
N/A	VCCAUX		AK2			
N/A	VCCAUX		AJ30			
N/A	VCCAUX		AJ1			
N/A	VCCAUX		T30			
N/A	VCCAUX		T1			
N/A	VCCAUX		R30			
N/A	VCCAUX		R1			
N/A	VCCAUX		B30			
N/A	VCCAUX		B1			
N/A	VCCAUX		A29			
N/A	VCCAUX		A16			
N/A	VCCAUX		A15			
N/A	VCCAUX		A2			
N/A	VCCINT		Y19			
N/A	VCCINT		Y18			
N/A	VCCINT		Y17			
N/A	VCCINT		Y16			
N/A	VCCINT		Y15			
N/A	VCCINT		Y14			

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	GND		AG19			
N/A	GND		AG12			
N/A	GND		AG9			
N/A	GND		AG4			
N/A	GND		AF26			
N/A	GND		AF5			
N/A	GND		AE25			
N/A	GND		AE18			
N/A	GND		AE13			
N/A	GND		AE6			
N/A	GND		AC30			
N/A	GND		AC1			
N/A	GND		Y28			
N/A	GND		Y25			
N/A	GND		Y20			
N/A	GND		Y11			
N/A	GND		Y6			
N/A	GND		Y3			
N/A	GND		W19			
N/A	GND		W18			
N/A	GND		W17			
N/A	GND		W16			
N/A	GND		W15			
N/A	GND		W14			
N/A	GND		W13			
N/A	GND		W12			
N/A	GND		V19			
N/A	GND		V18			
N/A	GND		V17			
N/A	GND		V16			
N/A	GND		V15			
N/A	GND		V14			
N/A	GND		V13			
N/A	GND		V12			
N/A	GND		U25			
N/A	GND		U19			

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L38N_2	N10				
2	IO_L38P_2	N9				
2	IO_L39N_2	M7				
2	IO_L39P_2	M6				
2	IO_L40N_2/VREF_2	L2				
2	IO_L40P_2	M2				
2	IO_L41N_2	N8				
2	IO_L41P_2	N7				
2	IO_L42N_2	L4				
2	IO_L42P_2	L3				
2	IO_L43N_2	M4				
2	IO_L43P_2	M3				
2	IO_L44N_2	P10				
2	IO_L44P_2	P9				
2	IO_L45N_2	N6				
2	IO_L45P_2	N5				
2	IO_L46N_2/VREF_2	M1				
2	IO_L46P_2	N1				
2	IO_L47N_2	P8				
2	IO_L47P_2	P7				
2	IO_L48N_2	N4				
2	IO_L48P_2	N3				
2	IO_L49N_2	N2				
2	IO_L49P_2	P2				
2	IO_L50N_2	R10				
2	IO_L50P_2	R9				
2	IO_L51N_2	P6				
2	IO_L51P_2	P5				
2	IO_L52N_2/VREF_2	P4				
2	IO_L52P_2	P3				
2	IO_L53N_2	T11				
2	IO_L53P_2	U11				
2	IO_L54N_2	R7				
2	IO_L54P_2	R6				
2	IO_L55N_2	P1				
2	IO_L55P_2	R1				
2	IO_L56N_2	T10				
2	IO_L56P_2	T9				

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
2	IO_L02P_2	D9		
2	IO_L03N_2	B7		
2	IO_L03P_2	A7		
2	IO_L04N_2/VREF_2	B6		
2	IO_L04P_2	A6		
2	IO_L05N_2	E8		
2	IO_L05P_2	D8		
2	IO_L06N_2	B4		
2	IO_L06P_2	A4		
2	IO_L07N_2	B3		
2	IO_L07P_2	A3		
2	IO_L08N_2	H7		
2	IO_L08P_2	H8		
2	IO_L09N_2	C6		
2	IO_L09P_2	C7		
2	IO_L10N_2/VREF_2	C5		
2	IO_L10P_2	B5		
2	IO_L11N_2	K8		
2	IO_L11P_2	J8		
2	IO_L12N_2	C1		
2	IO_L12P_2	C2		
2	IO_L13N_2	E7		
2	IO_L13P_2	D7		
2	IO_L14N_2	J6		
2	IO_L14P_2	J7		
2	IO_L15N_2	D5		
2	IO_L15P_2	D6		
2	IO_L16N_2/VREF_2	E4		
2	IO_L16P_2	D4		
2	IO_L17N_2	L9		
2	IO_L17P_2	K9		
2	IO_L18N_2	E3		
2	IO_L18P_2	D3		
2	IO_L19N_2	D1		
2	IO_L19P_2	D2		
2	IO_L20N_2	K7		
2	IO_L20P_2	L7		
2	IO_L21N_2	F6		

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
5	IO_L69P_5	AJ18		
5	IO_L68N_5	AF18		
5	IO_L68P_5	AG18		
5	IO_L67N_5	AM19		
5	IO_L67P_5	AN19		
5	IO_L66N_5/VREF_5	AH19	NC	
5	IO_L66P_5	AJ19	NC	
5	IO_L57N_5/VREF_5	AN20		
5	IO_L57P_5	AP20		
5	IO_L56N_5	AD19		
5	IO_L56P_5	AE19		
5	IO_L55N_5	AL19		
5	IO_L55P_5	AM20		
5	IO_L54N_5	AJ20		
5	IO_L54P_5	AK20		
5	IO_L53_5/No_Pair	AG19		
5	IO_L50_5/No_Pair	AH20		
5	IO_L49N_5	AN21		
5	IO_L49P_5	AP21		
5	IO_L48N_5	AL21		
5	IO_L48P_5	AM21		
5	IO_L47N_5	AD20		
5	IO_L47P_5	AE20		
5	IO_L46N_5	AJ21		
5	IO_L46P_5	AK21		
5	IO_L45N_5/VREF_5	AG21		
5	IO_L45P_5	AH21		
5	IO_L44N_5	AD21		
5	IO_L44P_5	AE21		
5	IO_L43N_5	AM22		
5	IO_L43P_5	AN22		
5	IO_L39N_5	AH22		
5	IO_L39P_5	AJ22		
5	IO_L38N_5	AF20		
5	IO_L38P_5	AF21		
5	IO_L37N_5	AN23		
5	IO_L37P_5	AP23		
5	IO_L27N_5/VREF_5	AL22		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L34P_6	AG37		
6	IO_L34N_6	AF37		
6	IO_L35P_6	AE30		
6	IO_L35N_6	AE31		
6	IO_L36P_6	AG33		
6	IO_L36N_6	AG34		
6	IO_L37P_6	AF38		
6	IO_L37N_6	AF39		
6	IO_L38P_6	AD28		
6	IO_L38N_6	AC28		
6	IO_L39P_6	AF35		
6	IO_L39N_6/VREF_6	AF36		
6	IO_L40P_6	AF33		
6	IO_L40N_6	AF34		
6	IO_L41P_6	AD29		
6	IO_L41N_6	AD30		
6	IO_L42P_6	AE38		
6	IO_L42N_6	AE39		
6	IO_L43P_6	AE36		
6	IO_L43N_6	AE37		
6	IO_L44P_6	AC27		
6	IO_L44N_6	AB27		
6	IO_L45P_6	AE34		
6	IO_L45N_6/VREF_6	AE35		
6	IO_L46P_6	AE32		
6	IO_L46N_6	AE33		
6	IO_L47P_6	AC30		
6	IO_L47N_6	AC31		
6	IO_L48P_6	AD37		
6	IO_L48N_6	AD38		
6	IO_L49P_6	AD33		
6	IO_L49N_6	AD34		
6	IO_L50P_6	AB28		
6	IO_L50N_6	AB29		
6	IO_L51P_6	AD36		
6	IO_L51N_6/VREF_6	AC36		
6	IO_L52P_6	AD32		
6	IO_L52N_6	AC32		

FF1704 Flip-Chip Fine-Pitch BGA Package

As shown in [Table 13](#), XC2VP70 and XC2VP100 Virtex-II Pro devices are available in the FF1704 flip-chip fine-pitch BGA package. Following this table are the [FF1704 Flip-Chip Fine-Pitch BGA Package Specifications \(1.00mm pitch\)](#).

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
0	IO_L01N_0/VRP_0		G34		
0	IO_L01P_0/VRN_0		H34		
0	IO_L02N_0		F34		
0	IO_L02P_0		E34		
0	IO_L03N_0		C34		
0	IO_L03P_0/VREF_0		D34		
0	IO_L05_0/No_Pair		K32		
0	IO_L06N_0		H33		
0	IO_L06P_0		J33		
0	IO_L07N_0		F33		
0	IO_L07P_0		G33		
0	IO_L08N_0		E33		
0	IO_L08P_0		D33		
0	IO_L09N_0		H32		
0	IO_L09P_0/VREF_0		J32		
0	IO_L19N_0		E32		
0	IO_L19P_0		F32		
0	IO_L20N_0		C33		
0	IO_L20P_0		C32		
0	IO_L21N_0		K31		
0	IO_L21P_0		L31		
0	IO_L25N_0		H31		
0	IO_L25P_0		J31		
0	IO_L26N_0		G31		
0	IO_L26P_0		F31		
0	IO_L27N_0		D31		
0	IO_L27P_0/VREF_0		E31		
0	IO_L28N_0		L30		
0	IO_L28P_0		M30		
0	IO_L29N_0		J30		
0	IO_L29P_0		K30		
0	IO_L30N_0		G30		
0	IO_L30P_0		H30		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	IO_L75N_1/GCLK3P		G21		
1	IO_L75P_1/GCLK2S		F21		
1	IO_L74N_1/GCLK1P		J21		
1	IO_L74P_1/GCLK0S		K21		
1	IO_L73N_1		D20		
1	IO_L73P_1		C20		
1	IO_L69N_1/VREF_1		F20		
1	IO_L69P_1		E20		
1	IO_L68N_1		H20		
1	IO_L68P_1		J20		
1	IO_L67N_1		L20		
1	IO_L67P_1		K20		
1	IO_L66N_1/VREF_1		M20		
1	IO_L66P_1		M21		
1	IO_L65N_1		C19		
1	IO_L65P_1		D19		
1	IO_L64N_1		F19		
1	IO_L64P_1		E19		
1	IO_L60N_1		H19		
1	IO_L60P_1		G19		
1	IO_L59N_1		K19		
1	IO_L59P_1		J19		
1	IO_L58N_1		M19		
1	IO_L58P_1		L19		
1	IO_L57N_1/VREF_1		C17		
1	IO_L57P_1		C18		
1	IO_L56N_1		E18		
1	IO_L56P_1		E17		
1	IO_L55N_1		H18		
1	IO_L55P_1		G18		
1	IO_L54N_1		L18		
1	IO_L54P_1		K18		
1	IO_L53_1/No_Pair		D17		
1	IO_L50_1/No_Pair		D16		
1	IO_L49N_1		G17		
1	IO_L49P_1		F17		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L17N_3		AL9		
3	IO_L17P_3		AL10		
3	IO_L16N_3		AM1		
3	IO_L16P_3		AM2		
3	IO_L15N_3/VREF_3		AM3		
3	IO_L15P_3		AN3		
3	IO_L14N_3		AM8		
3	IO_L14P_3		AM9		
3	IO_L13N_3		AM4		
3	IO_L13P_3		AM5		
3	IO_L12N_3		AM6		
3	IO_L12P_3		AM7		
3	IO_L11N_3		AN9		
3	IO_L11P_3		AM10		
3	IO_L10N_3		AN1		
3	IO_L10P_3		AN2		
3	IO_L09N_3/VREF_3		AN5		
3	IO_L09P_3		AN6		
3	IO_L08N_3		AN7		
3	IO_L08P_3		AN8		
3	IO_L07N_3		AP1		
3	IO_L07P_3		AP2		
3	IO_L84N_3		AP4		
3	IO_L84P_3		AP5		
3	IO_L83N_3		AR7		
3	IO_L83P_3		AP8		
3	IO_L82N_3		AP6		
3	IO_L82P_3		AP7		
3	IO_L81N_3/VREF_3		AR2		
3	IO_L81P_3		AR3		
3	IO_L80N_3		AT5		
3	IO_L80P_3		AR6		
3	IO_L79N_3		AR4		
3	IO_L79P_3		AR5		
3	IO_L78N_3		AT1		
3	IO_L78P_3		AT2		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L27P_7		P33		
7	IO_L27N_7		P34		
7	IO_L26P_7		N31		
7	IO_L26N_7		N32		
7	IO_L25P_7		N41		
7	IO_L25N_7		N42		
7	IO_L24P_7		N39		
7	IO_L24N_7		N40		
7	IO_L23P_7		N33		
7	IO_L23N_7		N34		
7	IO_L22P_7		N37		
7	IO_L22N_7/VREF_7		N38		
7	IO_L21P_7		N35		
7	IO_L21N_7		N36		
7	IO_L20P_7		M38		
7	IO_L20N_7		M39		
7	IO_L19P_7		M40		
7	IO_L19N_7		M41		
7	IO_L18P_7		M33		
7	IO_L18N_7		M34		
7	IO_L17P_7		M31		
7	IO_L17N_7		M32		
7	IO_L16P_7		M35		
7	IO_L16N_7/VREF_7		M36		
7	IO_L15P_7		L41		
7	IO_L15N_7		L42		
7	IO_L14P_7		L39		
7	IO_L14N_7		L38		
7	IO_L13P_7		L40		
7	IO_L13N_7		K40		
7	IO_L12P_7		L36		
7	IO_L12N_7		L37		
7	IO_L11P_7		L34		
7	IO_L11N_7		L35		
7	IO_L10P_7		K42		
7	IO_L10N_7/VREF_7		K41		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	VCCINT		AF16		
N/A	VCCINT		AG27		
N/A	VCCINT		AG26		
N/A	VCCINT		AG25		
N/A	VCCINT		AG24		
N/A	VCCINT		AG23		
N/A	VCCINT		AG22		
N/A	VCCINT		AG21		
N/A	VCCINT		AG20		
N/A	VCCINT		AG19		
N/A	VCCINT		AG18		
N/A	VCCINT		AG17		
N/A	VCCINT		AG16		
N/A	VCCINT		AH28		
N/A	VCCINT		AH27		
N/A	VCCINT		AH26		
N/A	VCCINT		AH17		
N/A	VCCINT		AH16		
N/A	VCCINT		AH15		
N/A	VCCINT		AJ29		
N/A	VCCINT		AJ28		
N/A	VCCINT		AJ27		
N/A	VCCINT		AJ16		
N/A	VCCINT		AJ15		
N/A	VCCINT		AJ14		
N/A	VCCINT		AK30		
N/A	VCCINT		AK13		
N/A	VCCINT		AA27		
N/A	VCCINT		AA16		
N/A	VCCINT		Y27		
N/A	VCCINT		Y16		
N/A	VCCINT		W27		
N/A	VCCINT		W16		
N/A	VCCINT		V27		
N/A	VCCINT		V16		
N/A	VCCINT		U27		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AU25		
N/A	GND		AU18		
N/A	GND		AU6		
N/A	GND		AV38		
N/A	GND		AV22		
N/A	GND		AV21		
N/A	GND		AV5		
N/A	GND		AW39		
N/A	GND		AW32		
N/A	GND		AW28		
N/A	GND		AW15		
N/A	GND		AW11		
N/A	GND		AW4		
N/A	GND		AY42		
N/A	GND		AY41		
N/A	GND		AY40		
N/A	GND		AY3		
N/A	GND		AY2		
N/A	GND		AY1		
N/A	GND		BA42		
N/A	GND		BA1		
N/A	GND		AA38		
N/A	GND		AA35		
N/A	GND		AA32		
N/A	GND		AA26		
N/A	GND		AA25		
N/A	GND		AA24		
N/A	GND		AA23		
N/A	GND		AA22		
N/A	GND		AA21		
N/A	GND		AA20		
N/A	GND		AA19		
N/A	GND		AA18		
N/A	GND		AA17		
N/A	GND		AA11		
N/A	GND		AA8		

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L62N_6	AL35	
6	IO_L63P_6	AV36	
6	IO_L63N_6/VREF_6	AU36	
6	IO_L64P_6	AV35	
6	IO_L64N_6	AU35	
6	IO_L65P_6	AK35	
6	IO_L65N_6	AJ34	
6	IO_L66P_6	AU41	
6	IO_L66N_6	AU42	
6	IO_L67P_6	AU38	
6	IO_L67N_6	AT38	
6	IO_L68P_6	AK32	
6	IO_L68N_6	AK33	
6	IO_L69P_6	AU37	
6	IO_L69N_6/VREF_6	AT37	
6	IO_L70P_6	AT41	
6	IO_L70N_6	AT42	
6	IO_L71P_6	AK31	
6	IO_L71N_6	AJ31	
6	IO_L72P_6	AT39	
6	IO_L72N_6	AT40	
6	IO_L07P_6	AT35	
6	IO_L07N_6	AT36	
6	IO_L08P_6	AJ32	
6	IO_L08N_6	AJ33	
6	IO_L09P_6	AR42	
6	IO_L09N_6/VREF_6	AP41	
6	IO_L10P_6	AR40	
6	IO_L10N_6	AR41	
6	IO_L11P_6	AH34	
6	IO_L11N_6	AH35	
6	IO_L12P_6	AR38	
6	IO_L12N_6	AR39	
6	IO_L13P_6	AR36	
6	IO_L13N_6	AR37	
6	IO_L14P_6	AH32	
6	IO_L14N_6	AH33	