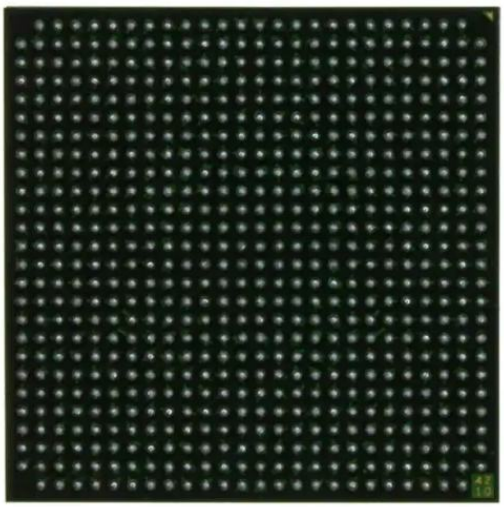


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	352
Number of Logic Elements/Cells	3168
Total RAM Bits	221184
Number of I/O	204
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp2-6ffg672i

- Programmable Receiver Equalization
- Internal AC Coupling
- On-Chip 50Ω Termination
  - Eliminates the need for external termination resistors
- Pre- and Post-Driver Serial and Parallel TX-to-RX Internal Loopback Modes for Testing Operability
- Programmable Comma Detection
  - Allows for any protocol
  - Allows for detection of any 10-bit character
- 8B/10B and 64B/66B Encoding Blocks

RocketIO Transceiver Features (All Except XC2VPX20 and XC2VPX70)

- Full-Duplex Serial Transceiver (SERDES) Capable of Baud Rates from 600 Mb/s to 3.125 Gb/s
- 100 Gb/s Duplex Data Rate (20 Channels)
- Monolithic Clock Synthesis and Clock Recovery (CDR)
- Fibre Channel, 10G Fibre Channel, Gigabit Ethernet, 10 Gb Attachment Unit Interface (XAUI), and Infiniband-Compliant Transceivers
- 8-, 16-, or 32-bit Selectable Internal FPGA Interface
- 8B/10B Encoder and Decoder (optional)
- 50Ω/75Ω on-chip Selectable Transmit and Receive Terminations
- Programmable Comma Detection
- Channel Bonding Support (from 2 to 20 Channels)
- Rate Matching via Insertion/Deletion Characters
- Four Levels of Selectable Pre-Emphasis
- Five Levels of Output Differential Voltage
- Per-Channel Internal Loopback Modes
- 2.5V Transceiver Supply Voltage

PowerPC RISC Processor Block Features (All Except XC2VP2)

- Embedded 300+ MHz Harvard Architecture Block
- Low Power Consumption: 0.9 mW/MHz
- Five-Stage Data Path Pipeline
- Hardware Multiply/Divide Unit
- Thirty-Two 32-bit General Purpose Registers
- 16 KB Two-Way Set-Associative Instruction Cache
- 16 KB Two-Way Set-Associative Data Cache
- Memory Management Unit (MMU)
  - 64-entry unified Translation Look-aside Buffers (TLB)
  - Variable page sizes (1 KB to 16 MB)
- Dedicated On-Chip Memory (OCM) Interface
- Supports IBM CoreConnect™ Bus Architecture
- Debug and Trace Support
- Timer Facilities

Virtex-II Pro Platform FPGA Technology (All Devices)

- SelectRAM+ Memory Hierarchy
  - Up to 8 Mb of True Dual-Port RAM in 18 Kb block SelectRAM+ resources
  - Up to 1,378 Kb of distributed SelectRAM+ resources
  - High-performance interfaces to external memory
- Arithmetic Functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible Logic Resources
  - Up to 88,192 internal registers/latches with Clock Enable
  - Up to 88,192 look-up tables (LUTs) or cascadable variable (1 to 16 bits) shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and Sum-of-Products support
  - Internal 3-state busing
- High-Performance Clock Management Circuitry
  - Up to twelve Digital Clock Manager (DCM) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers in all parts
- Active Interconnect Technology
  - Fourth-generation segmented routing structure
  - Fast, predictable routing delay, independent of fanout
  - Deep sub-micron noise immunity benefits
- SelectIO™-Ultra Technology
  - Up to 1,164 user I/Os
  - Twenty-two single-ended standards and ten differential standards
  - Programmable LVCMOS sink/source current (2 mA to 24 mA) per I/O
  - XCITE Digitally Controlled Impedance (DCI) I/O
  - PCI/PCI-X support (1)
  - Differential signaling
    - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
    - On-chip differential termination
    - Bus LVDS I/O

1. Refer to XAPP653 for more information.

Multiplexers

Virtex-II Pro function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II Pro slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in Figure 41. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II Pro Platform FPGA User Guide*. Any LUT can implement a 2:1 multiplexer.

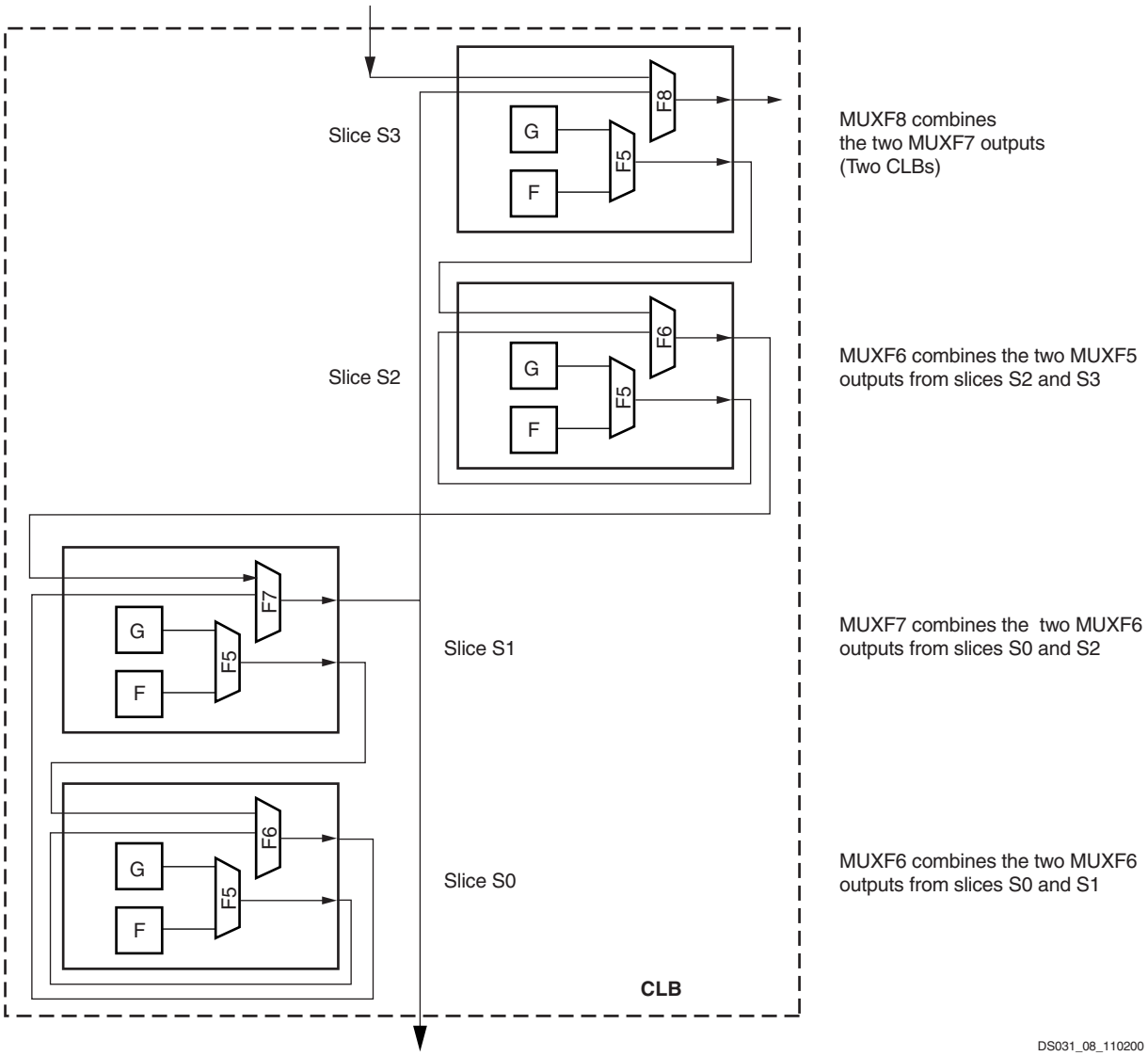


Figure 41: **MUXF5 and MUXFX multiplexers**

Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II Pro CLB has two separate carry chains, as shown in the Figure 42.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II Pro device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 34) improves the efficiency of multiplier implementation.

Each block SelectRAM+ cell is a fully synchronous memory, as illustrated in Figure 48. The two ports have independent inputs and outputs and are independently clocked.

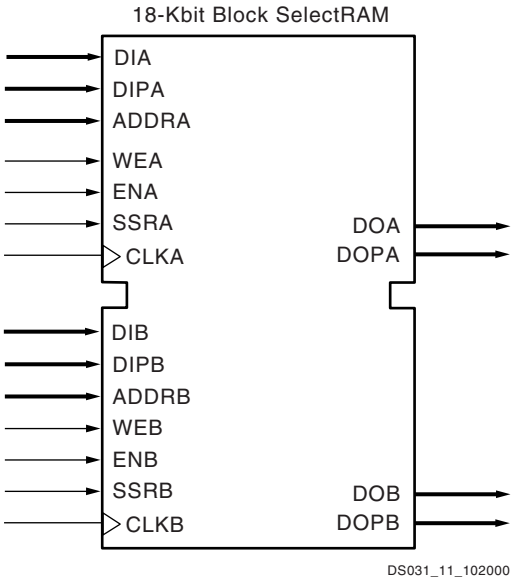


Figure 48: **18 Kb Block SelectRAM+ in Dual-Port Mode**

Port Aspect Ratios

Table 23 shows the depth and the width aspect ratios for the 18 Kb block SelectRAM+ resource. Virtex-II Pro block SelectRAM+ also includes dedicated routing resources to provide an efficient interface with CLBs, block SelectRAM+, and multipliers.

Table 23: **18 Kb Block SelectRAM+ Port Aspect Ratio**

Width	Depth	Address Bus	Data Bus	Parity Bus
1	16,384	ADDR[13:0]	DATA[0]	N/A
2	8,192	ADDR[12:0]	DATA[1:0]	N/A
4	4,096	ADDR[11:0]	DATA[3:0]	N/A
9	2,048	ADDR[10:0]	DATA[7:0]	Parity[0]
18	1,024	ADDR[9:0]	DATA[15:0]	Parity[1:0]
36	512	ADDR[8:0]	DATA[31:0]	Parity[3:0]

Read/Write Operations

The Virtex-II Pro block SelectRAM+ read operation is fully synchronous. An address is presented, and the read operation is enabled by control signal ENA or ENB. Then, depending on clock polarity, a rising or falling clock edge causes the stored data to be loaded into output registers.

The write operation is also fully synchronous. Data and address are presented, and the write operation is enabled by control signals WEA and WEB in addition to ENA or ENB. Then, again depending on the clock input mode, a rising or falling clock edge causes the data to be loaded into the memory cell addressed.

A write operation performs a simultaneous read operation. Three different options are available, selected by configuration:

1. **WRITE_FIRST**

   The WRITE_FIRST option is a transparent mode. The same clock edge that writes the data input (DI) into the memory also transfers DI into the output registers DO, as shown in Figure 49.

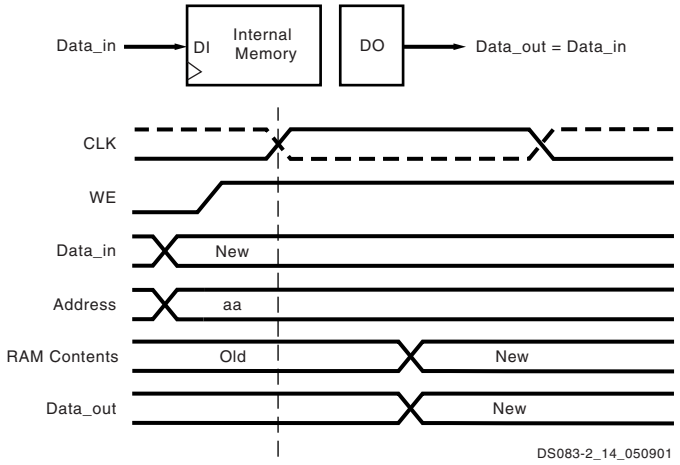


Figure 49: **WRITE_FIRST Mode**

2. **READ_FIRST**

The READ_FIRST option is a read-before-write mode.

The same clock edge that writes data input (DI) into the memory also transfers the prior content of the memory cell addressed into the data output registers DO, as shown in Figure 50.

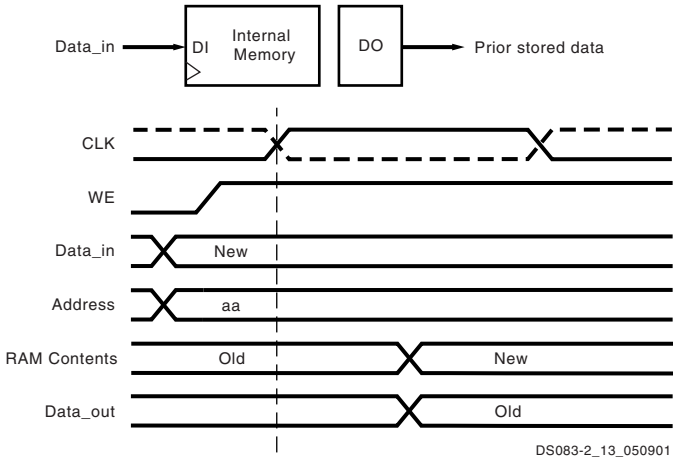


Figure 50: **READ_FIRST Mode**

Routing

DCM and MGT Locations/Organization

Virtex-II Pro DCMs and serial transceivers (MGTs) are placed on the top and bottom of each block RAM and multiplier column in some combination, as shown in Table 31. The number of DCMs and RocketIO transceivers total twice the number of block RAM columns in the device. Refer to Figure 52, page 47 for an illustration of this in the XC2VP4 device.

Table 31: **DCM and MGT Organization**

Device	Block RAM Columns	DCMs	MGTs
XC2VP2	4	4	4
XC2VP4	4	4	4
XC2VP7	6	4	8
XC2VP20	8	8	8
XC2VPX20	8	8	8
XC2VP30	8	8	8
XC2VP40	10	8	12
XC2VP50	12	8	16
XC2VP70	14	8	20
XC2VPX70	14	8	20
XC2VP100	16	12	20

Place-and-route software takes advantage of this regular array to deliver optimum system performance and fast compile times. The segmented routing resources are essential to guarantee IP cores portability and to efficiently handle an incremental design flow that is based on modular implementations. Total design time is reduced due to fewer and shorter design iterations.

Hierarchical Routing Resources

Most Virtex-II Pro signals are routed using the global routing resources, which are located in horizontal and vertical routing channels between each switch matrix.

As shown in Figure 64, page 54, Virtex-II Pro has fully buffered programmable interconnections, with a number of resources counted between any two adjacent switch matrix rows or columns. Fanout has minimal impact on the performance of each net.

- The long lines are bidirectional wires that distribute signals across the device. Vertical and horizontal long lines span the full height and width of the device.
- The hex lines route signals to every third or sixth block away in all four directions. Organized in a staggered pattern, hex lines can only be driven from one end. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source).

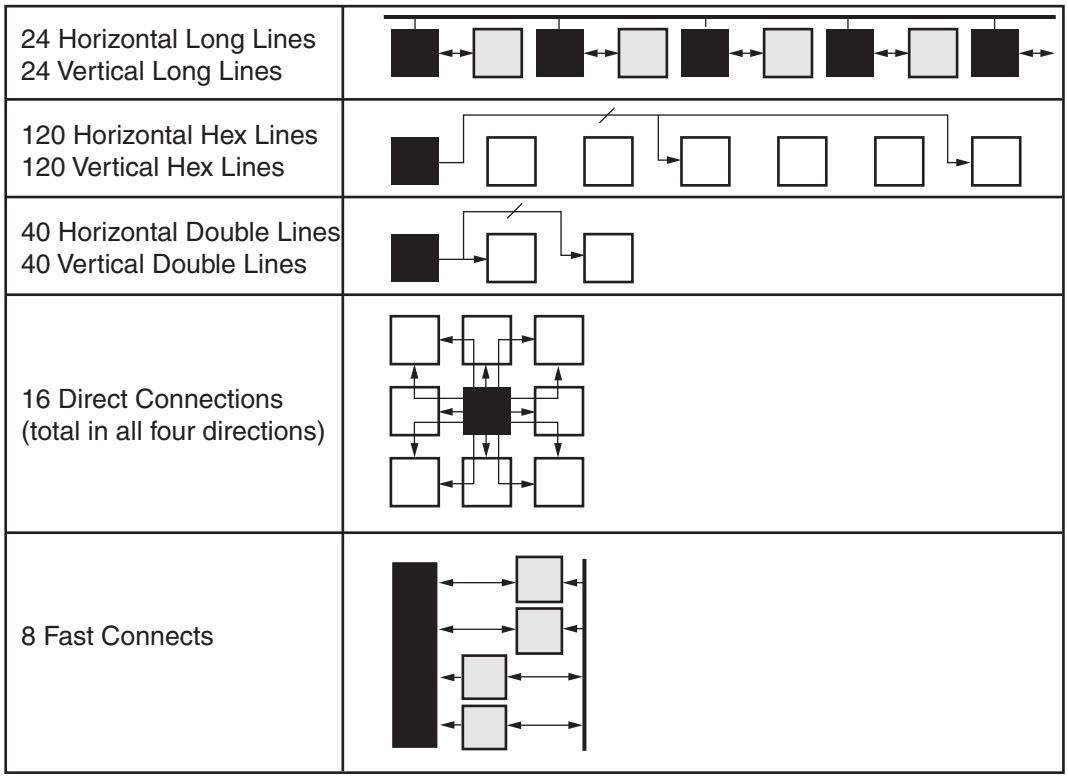


Figure 64: **Hierarchical Routing Resources**

Date	Version	Revision
09/15/05	4.4	• Table 2: Added Footnote (7) to AVCCAUXRX for RocketIO X (1.8V for all non-8B/10B-encoded data). • Table 3: - Power dissipation for 10.3125 Gb/s deleted. - Max $I_{CCAUXTX}$ and $I_{CCAUXRX}$ specifications added for Virtex-II Pro. • Table 11: Added specification for minimum p-p differential input voltage. • Table 22: - F_{GCLK}: Changed high end of range to 425 MHz. - T_{GJTT}: Changed measurement units to picoseconds and added maximum specifications for two bit rate ranges. - T_{LOCK}: Changed measurement units to microseconds and adderd typical specification. - T_{PHASE}: Changed measurement units to microseconds and adderd typical and maximum specifications. • Table 24: - All parameters: Deleted specifications for 10.3125 Gb/s. - T_{RJTOL}: Added typical specifications. - T_{JTOL}, T_{SJTOL}, and T_{DDJTOL}: Added typical and maximum specifications. • Table 26: Restructured table. Total Jitter parameter added. All jitter parameters respecified. • Table 28: Restructured table and added new specifications.
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s. • Table 15: Removed -7 designations for XC2VPX20 and XC2VPX70 devices.
03/05/07	4.6	*No changes in Module 3 for this revision.*
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner. Changed I_{TRX} typical value in Table 3.

Notice of Disclaimer

Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
3	IO_L03P_3	AC25			
3	IO_L02N_3	AC24			
3	IO_L02P_3	AD25			
3	IO_L01N_3/VRP_3	AD26			
3	IO_L01P_3/VRN_3	AE26			
4	IO_L01N_4/BUSY/DOUT(1)	AB22			
4	IO_L01P_4/INIT_B	AC22			
4	IO_L02N_4/D0/DIN(1)	AB21			
4	IO_L02P_4/D1	AC21			
4	IO_L03N_4/D2	Y20			
4	IO_L03P_4/D3	AA20			
4	IO_L05_4/No_Pair	AB20			
4	IO_L06N_4/VRP_4	AC20			
4	IO_L06P_4/VRN_4	AD20			
4	IO_L07N_4	W19			
4	IO_L07P_4/VREF_4	Y19			
4	IO_L09N_4	AA19			
4	IO_L09P_4/VREF_4	AB19			
4	IO_L37N_4	AE19			
4	IO_L37P_4	AF19			
4	IO_L39N_4	W18			
4	IO_L39P_4	Y18			
4	IO_L43N_4	AA18			
4	IO_L43P_4	AB18			
4	IO_L45N_4	AC18			
4	IO_L45P_4/VREF_4	AD18			
4	IO_L46N_4	W17			
4	IO_L46P_4	W16			
4	IO_L48N_4	AB17			
4	IO_L48P_4	AB16			
4	IO_L49N_4	AC17			
4	IO_L49P_4	AD17			
4	IO_L50_4/No_Pair	Y16			
4	IO_L53_4/No_Pair	AA16			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L52N_6	U22	NC		
6	IO_L53P_6	U23	NC		
6	IO_L53N_6	U24	NC		
6	IO_L54P_6	V26	NC		
6	IO_L54N_6	U26	NC		
6	IO_L55P_6	U20	NC		
6	IO_L55N_6	T19	NC		
6	IO_L56P_6	T20	NC		
6	IO_L56N_6	R20	NC		
6	IO_L57P_6	T21	NC		
6	IO_L57N_6/VREF_6	T22	NC		
6	IO_L58P_6	T23	NC		
6	IO_L58N_6	T24	NC		
6	IO_L59P_6	T25	NC		
6	IO_L59N_6	T26	NC		
6	IO_L60P_6	R19	NC		
6	IO_L60N_6	P19	NC		
6	IO_L85P_6	R21			
6	IO_L85N_6	R22			
6	IO_L86P_6	R23			
6	IO_L86N_6	R24			
6	IO_L87P_6	R25			
6	IO_L87N_6/VREF_6	R26			
6	IO_L88P_6	P20			
6	IO_L88N_6	P21			
6	IO_L89P_6	P22			
6	IO_L89N_6	P23			
6	IO_L90P_6	P24			
6	IO_L90N_6	P25			
7	IO_L90P_7	N25			
7	IO_L90N_7	N24			
7	IO_L89P_7	N23			
7	IO_L89N_7	N22			
7	IO_L88P_7	N21			
7	IO_L88N_7/VREF_7	N20			
7	IO_L87P_7	M26			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
3	IO_L57P_3		Y1			
3	IO_L56N_3		U7			
3	IO_L56P_3		U8			
3	IO_L55N_3		V5			
3	IO_L55P_3		V6			
3	IO_L54N_3		Y2			
3	IO_L54P_3		AA2			
3	IO_L53N_3		V7			
3	IO_L53P_3		V8			
3	IO_L52N_3		W3			
3	IO_L52P_3		W4			
3	IO_L51N_3/VREF_3		AA1			
3	IO_L51P_3		AB1			
3	IO_L50N_3		W5			
3	IO_L50P_3		W6			
3	IO_L49N_3		Y4			
3	IO_L49P_3		Y5			
3	IO_L48N_3		AA3			
3	IO_L48P_3		AA4			
3	IO_L47N_3		W7			
3	IO_L47P_3		W8			
3	IO_L46N_3		AB3			
3	IO_L46P_3		AB4			
3	IO_L45N_3/VREF_3		AB2			
3	IO_L45P_3		AC2			
3	IO_L44N_3		AA5			
3	IO_L44P_3		AA6			
3	IO_L43N_3		AC3			
3	IO_L43P_3		AC4			
3	IO_L42N_3		AD1	NC		
3	IO_L42P_3		AD2	NC		
3	IO_L41N_3		Y7	NC		
3	IO_L41P_3		Y8	NC		
3	IO_L40N_3		AB5	NC		
3	IO_L40P_3		AB6	NC		
3	IO_L39N_3/VREF_3		AE1	NC		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
3	IO_L17N_3	AH9		
3	IO_L17P_3	AJ9		
3	IO_L16N_3	AK7		
3	IO_L16P_3	AL7		
3	IO_L15N_3/VREF_3	AK4		
3	IO_L15P_3	AL4		
3	IO_L14N_3	AJ7		
3	IO_L14P_3	AJ8		
3	IO_L13N_3	AK3		
3	IO_L13P_3	AL3		
3	IO_L12N_3	AL5		
3	IO_L12P_3	AL6		
3	IO_L11N_3	AK8		
3	IO_L11P_3	AL8		
3	IO_L10N_3	AL1		
3	IO_L10P_3	AL2		
3	IO_L09N_3/VREF_3	AM6		
3	IO_L09P_3	AM7		
3	IO_L08N_3	AL9		
3	IO_L08P_3	AM9		
3	IO_L07N_3	AM5		
3	IO_L07P_3	AN5		
3	IO_L06N_3	AM1		
3	IO_L06P_3	AM2		
3	IO_L05N_3	AN8		
3	IO_L05P_3	AN9		
3	IO_L04N_3	AN6		
3	IO_L04P_3	AP6		
3	IO_L03N_3/VREF_3	AN4		
3	IO_L03P_3	AP4		
3	IO_L02N_3	AN7		
3	IO_L02P_3	AP7		
3	IO_L01N_3/VRP_3	AN3		
3	IO_L01P_3/VRN_3	AP3		
4	IO_L01N_4/BUSY/DOUT(1)	AK10		
4	IO_L01P_4/INIT_B	AJ10		
4	IO_L02N_4/D0/DIN(1)	AF11		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
7	IO_L51P_7	N31		
7	IO_L51N_7	P31		
7	IO_L50P_7	T27		
7	IO_L50N_7	R28		
7	IO_L49P_7	M33		
7	IO_L49N_7	M34		
7	IO_L48P_7	M31		
7	IO_L48N_7	M32		
7	IO_L47P_7	R24		
7	IO_L47N_7	R25		
7	IO_L46P_7	M29		
7	IO_L46N_7/VREF_7	M30		
7	IO_L45P_7	L33		
7	IO_L45N_7	L34		
7	IO_L44P_7	P27		
7	IO_L44N_7	P28		
7	IO_L43P_7	L29		
7	IO_L43N_7	L30		
7	IO_L42P_7	K33		
7	IO_L42N_7	K34		
7	IO_L41P_7	P26		
7	IO_L41N_7	R26		
7	IO_L40P_7	K32		
7	IO_L40N_7/VREF_7	L32		
7	IO_L39P_7	K29		
7	IO_L39N_7	K30		
7	IO_L38P_7	P24		
7	IO_L38N_7	P25		
7	IO_L37P_7	J32		
7	IO_L37N_7	J33		
7	IO_L36P_7	J31		
7	IO_L36N_7	K31		
7	IO_L35P_7	N28		
7	IO_L35N_7	N29		
7	IO_L34P_7	H32		
7	IO_L34N_7/VREF_7	H33		
7	IO_L33P_7	H29		
7	IO_L33N_7	H30		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	VCCINT	M12		
N/A	VCCINT	AD11		
N/A	VCCINT	L11		
N/A	VCCAUX	AN34		
N/A	VCCAUX	AG34		
N/A	VCCAUX	U34		
N/A	VCCAUX	H34		
N/A	VCCAUX	B34		
N/A	VCCAUX	AP33		
N/A	VCCAUX	A33		
N/A	VCCAUX	AP27		
N/A	VCCAUX	A27		
N/A	VCCAUX	AP17		
N/A	VCCAUX	A17		
N/A	VCCAUX	AP8		
N/A	VCCAUX	A8		
N/A	VCCAUX	AP2		
N/A	VCCAUX	A2		
N/A	VCCAUX	AN1		
N/A	VCCAUX	AG1		
N/A	VCCAUX	U1		
N/A	VCCAUX	H1		
N/A	VCCAUX	B1		
N/A	GND	AK34		
N/A	GND	AF34		
N/A	GND	AB34		
N/A	GND	W34		
N/A	GND	V34		
N/A	GND	T34		
N/A	GND	N34		
N/A	GND	J34		
N/A	GND	E34		
N/A	GND	AN33		
N/A	GND	B33		
N/A	GND	AM32		
N/A	GND	C32		
N/A	GND	AP30		
N/A	GND	AK30		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	GND	W18		
N/A	GND	V18		
N/A	GND	U18		
N/A	GND	T18		
N/A	GND	AD17		
N/A	GND	AC17		
N/A	GND	AB17		
N/A	GND	AA17		
N/A	GND	Y17		
N/A	GND	W17		
N/A	GND	V17		
N/A	GND	U17		
N/A	GND	P20		
N/A	GND	L20		
N/A	GND	G20		
N/A	GND	C20		
N/A	GND	AD19		
N/A	GND	AC19		
N/A	GND	AB19		
N/A	GND	AA19		
N/A	GND	Y19		
N/A	GND	W19		
N/A	GND	V19		
N/A	GND	U19		
N/A	GND	T19		
N/A	GND	AD18		
N/A	GND	AC18		
N/A	GND	U21		
N/A	GND	T21		
N/A	GND	AU20		
N/A	GND	AN20		
N/A	GND	AJ20		
N/A	GND	AF20		
N/A	GND	AD20		
N/A	GND	AC20		
N/A	GND	AB20		
N/A	GND	AA20		
N/A	GND	Y20		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
0	IO_L34N_0		E30		
0	IO_L34P_0		F30		
0	IO_L35N_0		D30		
0	IO_L35P_0		C30		
0	IO_L36N_0		M28		
0	IO_L36P_0/VREF_0		M29		
0	IO_L78N_0		K29	NC	
0	IO_L78P_0		L29	NC	
0	IO_L83_0/No_Pair		H29	NC	
0	IO_L84N_0		F29	NC	
0	IO_L84P_0		G29	NC	
0	IO_L85N_0		D29	NC	
0	IO_L85P_0		E29	NC	
0	IO_L86N_0		L28	NC	
0	IO_L86P_0		K28	NC	
0	IO_L87N_0		H28	NC	
0	IO_L87P_0/VREF_0		J28	NC	
0	IO_L37N_0		E28		
0	IO_L37P_0		F28		
0	IO_L38N_0		C29		
0	IO_L38P_0		C28		
0	IO_L39N_0		L27		
0	IO_L39P_0		M27		
0	IO_L43N_0		J27		
0	IO_L43P_0		K27		
0	IO_L44N_0		H27		
0	IO_L44P_0		G27		
0	IO_L45N_0		E27		
0	IO_L45P_0/VREF_0		F27		
0	IO_L46N_0		M25		
0	IO_L46P_0		M26		
0	IO_L47N_0		L26		
0	IO_L47P_0		K26		
0	IO_L48N_0		H26		
0	IO_L48P_0		J26		
0	IO_L49N_0		F26		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
0	IO_L11N_0	M25	NC
0	IO_L11P_0	M26	NC
0	IO_L12N_0	F26	NC
0	IO_L12P_0	G26	NC
0	IO_L18N_0	B26	NC
0	IO_L18P_0/VREF_0	C26	NC
0	IO_L46N_0	G24	
0	IO_L46P_0	G25	
0	IO_L47N_0	K26	
0	IO_L47P_0	L26	
0	IO_L48N_0	E25	
0	IO_L48P_0	F25	
0	IO_L49N_0	C24	
0	IO_L49P_0	C25	
0	IO_L50_0/No_Pair	L24	
0	IO_L53_0/No_Pair	L25	
0	IO_L54N_0	A25	
0	IO_L54P_0	B25	
0	IO_L55N_0	H23	
0	IO_L55P_0	H24	
0	IO_L56N_0	J25	
0	IO_L56P_0	K25	
0	IO_L57N_0	E24	
0	IO_L57P_0/VREF_0	F24	
0	IO_L58N_0	D23	
0	IO_L58P_0	D24	
0	IO_L59N_0	J24	
0	IO_L59P_0	K24	
0	IO_L60N_0	A24	
0	IO_L60P_0	B24	
0	IO_L64N_0	F23	
0	IO_L64P_0	G23	
0	IO_L65N_0	M22	
0	IO_L65P_0	M23	
0	IO_L66N_0	B23	
0	IO_L66P_0/VREF_0	C23	
0	IO_L67N_0	H22	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
1	IO_L57P_1	E19	
1	IO_L56N_1	K18	
1	IO_L56P_1	J18	
1	IO_L55N_1	H19	
1	IO_L55P_1	H20	
1	IO_L54N_1	B18	
1	IO_L54P_1	A18	
1	IO_L53_1/No_Pair	L18	
1	IO_L50_1/No_Pair	L19	
1	IO_L49N_1	C18	
1	IO_L49P_1	C19	
1	IO_L48N_1	F18	
1	IO_L48P_1	E18	
1	IO_L47N_1	L17	
1	IO_L47P_1	K17	
1	IO_L46N_1	G18	
1	IO_L46P_1	G19	
1	IO_L18N_1/VREF_1	C17	NC
1	IO_L18P_1	B17	NC
1	IO_L12N_1	G17	NC
1	IO_L12P_1	F17	NC
1	IO_L11N_1	M17	NC
1	IO_L11P_1	M18	NC
1	IO_L10N_1	B16	NC
1	IO_L10P_1	A16	NC
1	IO_L45N_1/VREF_1	D16	
1	IO_L45P_1	D17	
1	IO_L44N_1	K16	
1	IO_L44P_1	J16	
1	IO_L43N_1	F16	
1	IO_L43P_1	E16	
1	IO_L39N_1	H16	
1	IO_L39P_1	H17	
1	IO_L38N_1	M16	
1	IO_L38P_1	L16	
1	IO_L37N_1	B15	
1	IO_L37P_1	A15	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L06N_3	BA8	
3	IO_L06P_3	BB8	
3	IO_L05N_3	AW8	
3	IO_L05P_3	AW9	
3	IO_L04N_3	BA7	
3	IO_L04P_3	BB7	
3	IO_L03N_3/VREF_3	BA6	
3	IO_L03P_3	BB6	
3	IO_L02N_3	AY9	
3	IO_L02P_3	BA9	
3	IO_L01N_3/VRP_3	BA4	
3	IO_L01P_3/VRN_3	BB4	
4	IO_L01N_4/BUSY/DOUT(1)	AL11	
4	IO_L01P_4/INIT_B	AL12	
4	IO_L02N_4/D0/DIN(1)	AV10	
4	IO_L02P_4/D1	AU10	
4	IO_L03N_4/D2	AN11	
4	IO_L03P_4/D3	AM11	
4	IO_L05_4/No_Pair	AT10	
4	IO_L06N_4/VRP_4	AY11	
4	IO_L06P_4/VRN_4	AY10	
4	IO_L07N_4	BB10	
4	IO_L07P_4/VREF_4	BA10	
4	IO_L08N_4	AU11	
4	IO_L08P_4	AT11	
4	IO_L09N_4	AR11	
4	IO_L09P_4/VREF_4	AP11	
4	IO_L19N_4	AW11	
4	IO_L19P_4	AV11	
4	IO_L20N_4	BB11	
4	IO_L20P_4	BA11	
4	IO_L21N_4	AN12	
4	IO_L21P_4	AM12	
4	IO_L25N_4	AR13	
4	IO_L25P_4	AT12	
4	IO_L26N_4	AV12	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
4	IO_L26P_4	AU12	
4	IO_L27N_4	AR12	
4	IO_L27P_4/VREF_4	AP12	
4	IO_L28N_4	AW13	
4	IO_L28P_4	AW12	
4	IO_L29N_4	BA12	
4	IO_L29P_4	AY12	
4	IO_L30N_4	AN13	
4	IO_L30P_4	AM13	
4	IO_L34N_4	AU13	
4	IO_L34P_4	AT13	
4	IO_L35N_4	BA13	
4	IO_L35P_4	AY13	
4	IO_L36N_4	AM14	
4	IO_L36P_4/VREF_4	AL14	
4	IO_L76N_4	AR15	
4	IO_L76P_4	AT14	
4	IO_L77N_4	AV14	
4	IO_L77P_4	AU14	
4	IO_L78N_4	AP14	
4	IO_L78P_4	AN14	
4	IO_L79N_4	AW15	
4	IO_L79P_4	AY14	
4	IO_L80_4/No_Pair	BB14	
4	IO_L83_4/No_Pair	BA14	
4	IO_L84N_4	AM15	
4	IO_L84P_4	AL15	
4	IO_L85N_4	AT16	
4	IO_L85P_4	AT15	
4	IO_L86N_4	AV15	
4	IO_L86P_4	AU15	
4	IO_L87N_4	AP15	
4	IO_L87P_4/VREF_4	AN15	
4	IO_L37N_4	AY16	
4	IO_L37P_4	AY15	
4	IO_L38N_4	BB15	
4	IO_L38P_4	BA15	

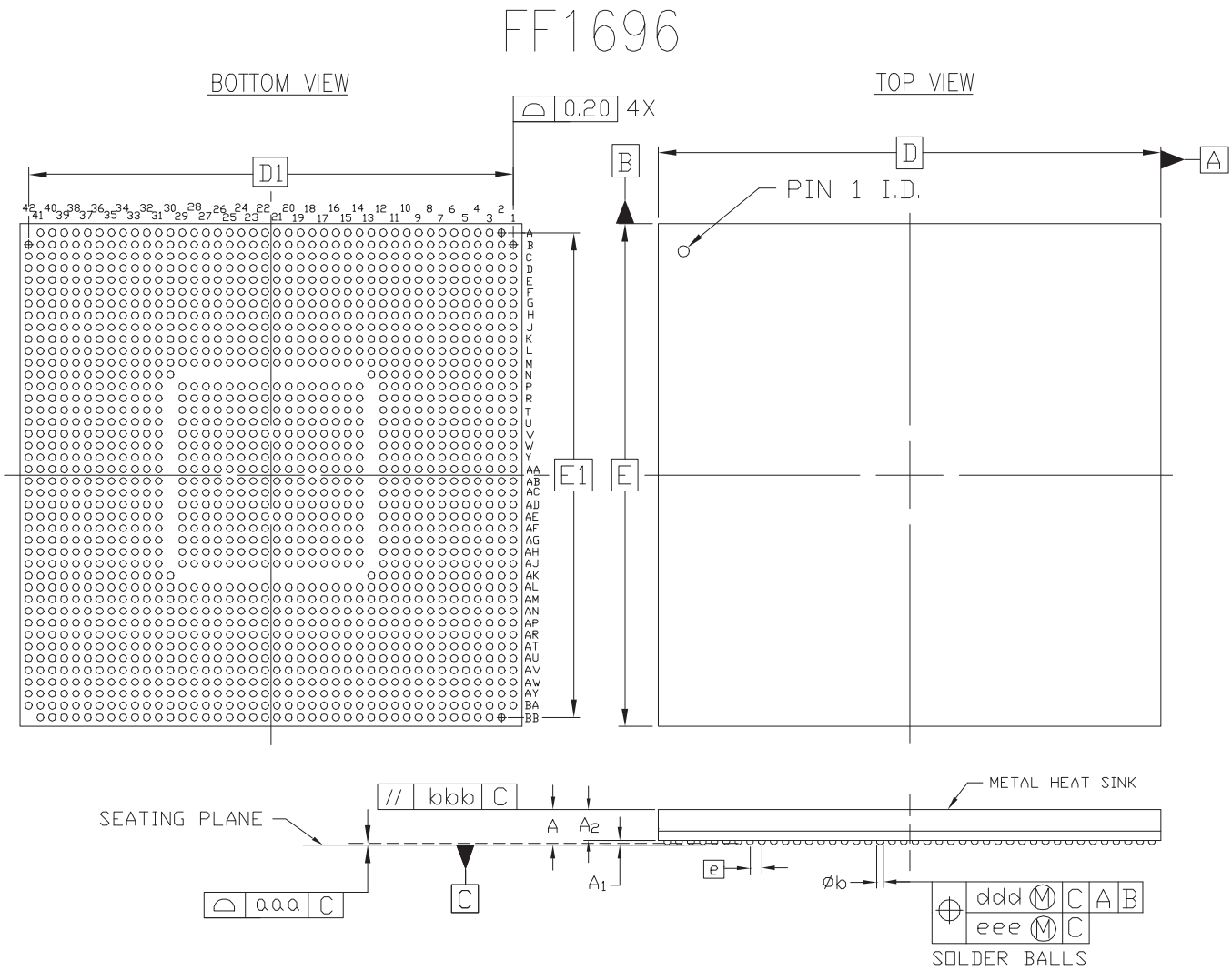
Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
4	IO_L39N_4	AM16	
4	IO_L39P_4	AL16	
4	IO_L43N_4	AR17	
4	IO_L43P_4	AR16	
4	IO_L44N_4	AV16	
4	IO_L44P_4	AU16	
4	IO_L45N_4	AP16	
4	IO_L45P_4/VREF_4	AN16	
4	IO_L10N_4	AW17	NC
4	IO_L10P_4	AW16	NC
4	IO_L11N_4	BB16	NC
4	IO_L11P_4	BA16	NC
4	IO_L12N_4	AL18	NC
4	IO_L12P_4	AL17	NC
4	IO_L16N_4	AU17	NC
4	IO_L16P_4	AT17	NC
4	IO_L18N_4	BA17	NC
4	IO_L18P_4/VREF_4	AY17	NC
4	IO_L46N_4	AT19	
4	IO_L46P_4	AT18	
4	IO_L47N_4	AN17	
4	IO_L47P_4	AM17	
4	IO_L48N_4	AV18	
4	IO_L48P_4	AU18	
4	IO_L49N_4	AY19	
4	IO_L49P_4	AY18	
4	IO_L50_4/No_Pair	AM19	
4	IO_L53_4/No_Pair	AM18	
4	IO_L54N_4	BB18	
4	IO_L54P_4	BA18	
4	IO_L55N_4	AR20	
4	IO_L55P_4	AR19	
4	IO_L56N_4	AP18	
4	IO_L56P_4	AN18	
4	IO_L57N_4	AV19	
4	IO_L57P_4/VREF_4	AU19	
4	IO_L58N_4	AW20	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L15P_6	AP39	
6	IO_L15N_6/VREF_6	AP40	
6	IO_L16P_6	AP36	
6	IO_L16N_6	AP37	
6	IO_L17P_6	AH31	
6	IO_L17N_6	AG31	
6	IO_L18P_6	AN41	
6	IO_L18N_6	AN42	
6	IO_L19P_6	AN40	
6	IO_L19N_6	AM40	
6	IO_L20P_6	AG34	
6	IO_L20N_6	AG35	
6	IO_L21P_6	AN37	
6	IO_L21N_6/VREF_6	AN38	
6	IO_L22P_6	AN36	
6	IO_L22N_6	AM36	
6	IO_L23P_6	AG32	
6	IO_L23N_6	AG33	
6	IO_L24P_6	AM41	
6	IO_L24N_6	AM42	
6	IO_L25P_6	AM38	
6	IO_L25N_6	AM39	
6	IO_L26P_6	AF35	
6	IO_L26N_6	AF36	
6	IO_L27P_6	AM37	
6	IO_L27N_6/VREF_6	AL36	
6	IO_L28P_6	AL41	
6	IO_L28N_6	AK41	
6	IO_L29P_6	AF32	
6	IO_L29N_6	AF33	
6	IO_L30P_6	AL39	
6	IO_L30N_6	AL40	
6	IO_L31P_6	AL37	
6	IO_L31N_6	AL38	
6	IO_L32P_6	AF31	
6	IO_L32N_6	AE31	
6	IO_L33P_6	AK39	

FF1696 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.45	
A_1	0.40	0.50	0.60	
A_2			2.85	
D/E	42.50 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M		42		2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)

Figure 10: **FF1696 Flip-Chip Fine-Pitch BGA Package Specifications**