AMD Xilinx - XC2VP2-6FG256C Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	352
Number of Logic Elements/Cells	3168
Total RAM Bits	221184
Number of I/O	140
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp2-6fg256c

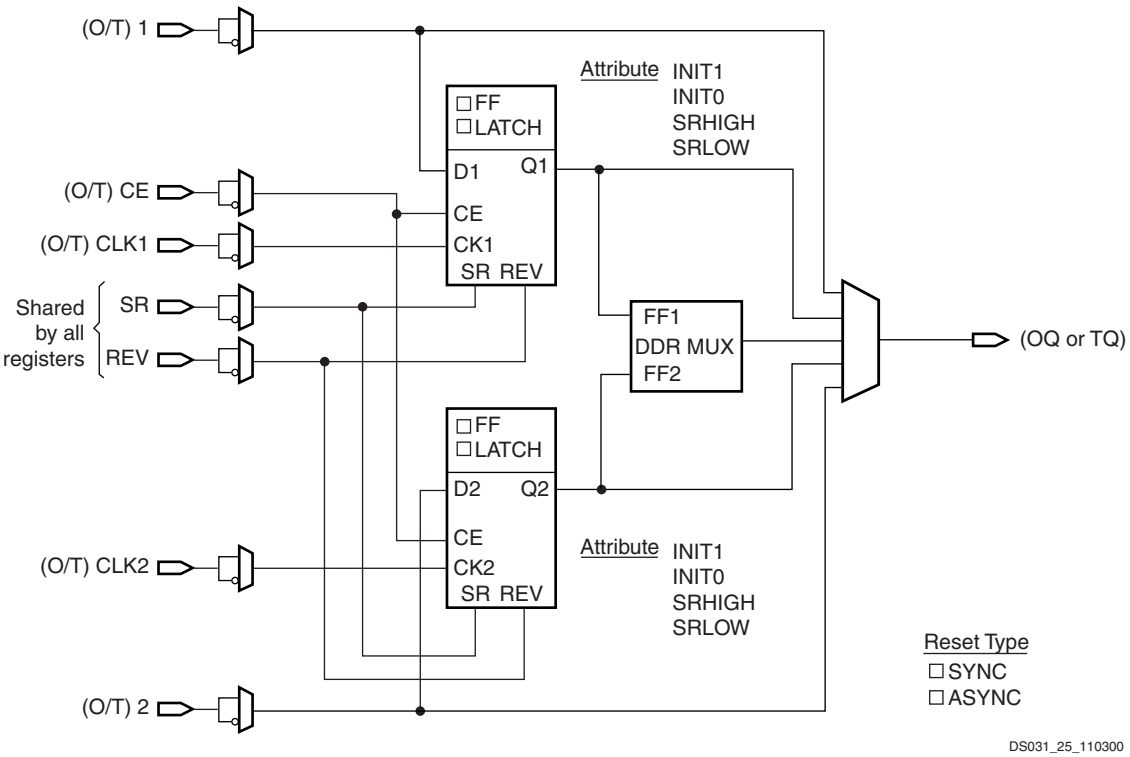


Figure 21: **Register / Latch Configuration in an IOB Block**

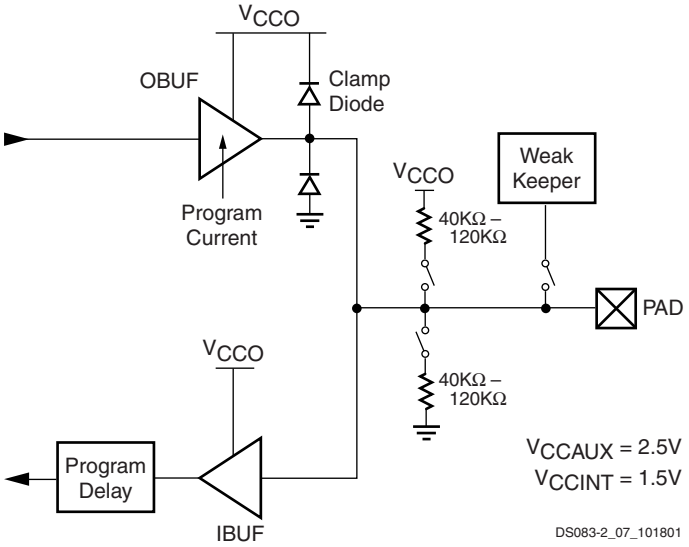


Figure 22: **LVTTL, LVCMOS, or PCI SelectIO-Ultra Standard**

Input/Output Individual Options

Each device pad has optional pull-up/pull-down resistors and weak-keeper circuit in the LVTTL, LVCMOS, and PCI SelectIO-Ultra configurations, as illustrated in Figure 22. Values of the optional pull-up and pull-down resistors fall within a range of 40 KΩ to 120 KΩ when V_{CCO} = 2.5V (from 2.38V to 2.63V only). The clamp diodes are always present, even when power is not.

The optional weak-keeper circuit is connected to each user I/O pad. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low. If the pin is connected to a multiple-source signal, the weak-keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter. An enabled pull-up or pull-down overrides the weak-keeper circuit.

LVCMOS25 sinks and sources current up to 24 mA. The current is programmable (see Table 11). Drive strength and slew rate controls for each output driver minimize bus transients. For LVDCI and LVDCI_DV2 standards, drive strength and slew rate controls are not available.

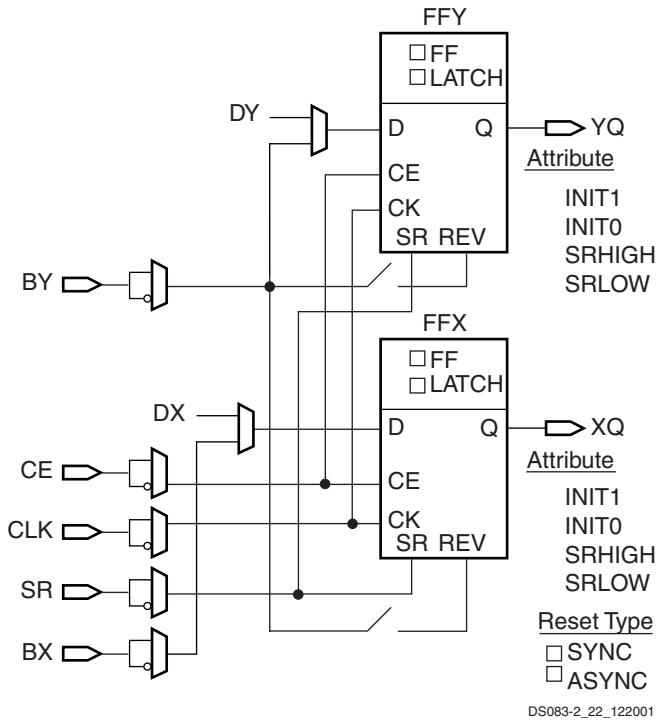


Figure 35: **Register / Latch Configuration in a Slice**

The set and reset functionality of a register or a latch can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

Distributed SelectRAM+ Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM+ element. SelectRAM+ elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8-bit RAM
- Single-Port 32 x 4-bit RAM
- Single-Port 64 x 2-bit RAM
- Single-Port 128 x 1-bit RAM
- Dual-Port 16 x 4-bit RAM
- Dual-Port 32 x 2-bit RAM
- Dual-Port 64 x 1-bit RAM

Distributed SelectRAM+ memory modules are synchronous (write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM+ memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.

Table 16 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM+ configuration.

Table 16: **Distributed SelectRAM+ Configurations**

RAM	Number of LUTs
16 x 1S	1
16 x 1D	2
32 x 1S	2
32 x 1D	4
64 x 1S	4
64 x 1D	8
128 x 1S	8

Notes:
1. S = single-port configuration; D = dual-port configuration

For single-port configurations, distributed SelectRAM+ memory has one address port for synchronous writes and asynchronous reads.

For dual-port configurations, distributed SelectRAM+ memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).

In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port

Figure 36, Figure 37, and Figure 38 illustrate various example configurations.

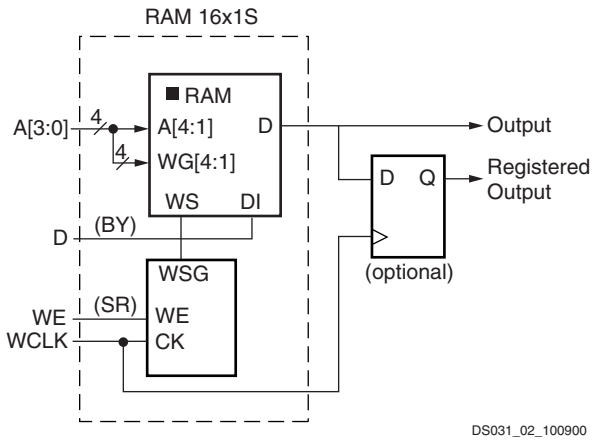


Figure 36: **Distributed SelectRAM+ (RAM16x1S)**

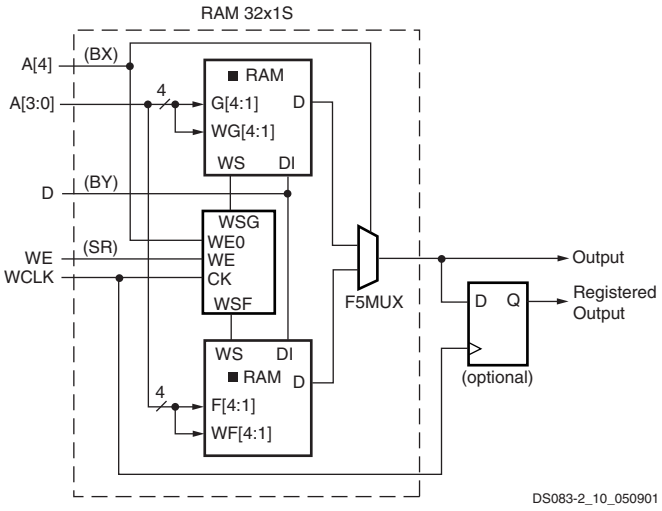


Figure 37: **Single-Port Distributed SelectRAM+ (RAM32x1S)**

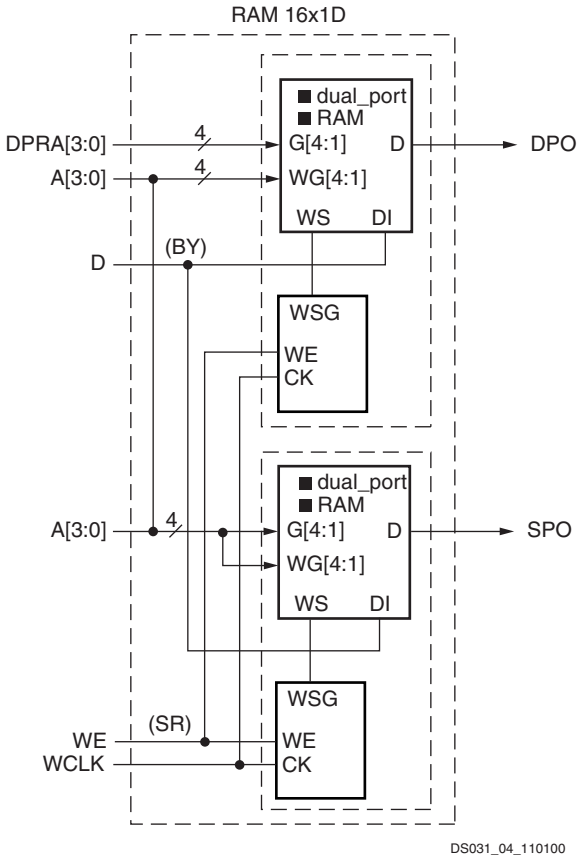


Figure 38: **Dual-Port Distributed SelectRAM+ (RAM16x1D)**

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 17 shows the number of LUTs occupied by each configuration.

Table 17: **ROM Configuration**

ROM	Number of LUTs
16 x 1	1
32 x 1	2
64 x 1	4
128 x 1	8 (1 CLB)
256 x 1	16 (2 CLBs)

Table 17: **Processor Block Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (CPMC405CLOCK)					
Device Control Register Bus control inputs	$T_{PCCK\_}DCR/T_{PCKC\_}DCR$	0.38/–0.18	0.44/–0.20	0.48/–0.23	ns, min
Device Control Register Bus data inputs	$T_{PDCK\_}DCR/T_{PCKD\_}DCR$	0.65/–0.01	0.75/–0.01	0.82/–0.02	ns, min
Clock and Power Management control inputs	$T_{PCCK\_}CPM/T_{PCKC\_}CPM$	0.16/ 0.03	0.19/ 0.03	0.20/ 0.03	ns, min
Reset control inputs	$T_{PCCK\_}RST/T_{PCKC\_}RST$	0.16/ 0.03	0.19/ 0.03	0.20/ 0.03	ns, min
Debug control inputs	$T_{PCCK\_}DBG/T_{PCKC\_}DBG$	0.27/ 0.30	0.31/ 0.35	0.34/ 0.38	ns, min
Trace control inputs	$T_{PCCK\_}TRC/T_{PCKC\_}TRC$	1.37/–0.41	1.57/–0.48	1.73/–0.52	ns, min
External Interrupt Controller control inputs	$T_{PCCK\_}EIC/T_{PCKC\_}EIC$	0.57/–0.22	0.66/–0.25	0.72/–0.27	ns, min
Clock to Out					
Device Control Register Bus control outputs	$T_{PCKCO\_}DCR$	1.32	1.52	1.67	ns, max
Device Control Register Bus address outputs	$T_{PCKAO\_}DCR$	1.72	1.98	2.17	ns, max
Device Control Register Bus data outputs	$T_{PCKDO\_}DCR$	1.76	2.02	2.22	ns, max
Clock and Power Management control outputs	$T_{PCKCO\_}CPM$	1.26	1.45	1.59	ns, max
Reset control outputs	$T_{PCKCO\_}RST$	1.32	1.51	1.66	ns, max
Debug control outputs	$T_{PCKCO\_}DBG$	1.94	2.22	2.44	ns, max
Trace control outputs	$T_{PCKCO\_}TRC$	1.35	1.56	1.71	ns, max
Clock					
CPMC405CLOCK minimum pulse width, high	T_{CPWH}	1.25	1.42	1.66	ns, min
CPMC405CLOCK minimum pulse width, low	T_{CPWL}	1.25	1.42	1.66	ns, min

Table 18: **Processor Block PLB Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (PLBCLK)					
Processor Local Bus(ICU/DCU) control inputs	$T_{PCCK\_}PLB/T_{PCKC\_}PLB$	0.98/ 0.18	1.12/ 0.21	1.23/ 0.23	ns, min
Processor Local Bus (ICU/DCU) data inputs	$T_{PDCK\_}PLB/T_{PCKD\_}PLB$	0.62/ 0.16	0.71/ 0.18	0.78/ 0.20	ns, min
Clock to Out					
Processor Local Bus(ICU/DCU) control outputs	$T_{PCKCO\_}PLB$	1.34	1.54	1.69	ns, max
Processor Local Bus(ICU/DCU) address bus outputs	$T_{PCKAO\_}PLB$	1.16	1.34	1.47	ns, max
Processor Local Bus(ICU/DCU) data bus outputs	$T_{PCKDO\_}PLB$	1.44	1.65	1.81	ns, max

Configuration Timing

Configuration Memory Clearing Parameters

Power-up timing of configuration signals is shown in Figure 7; corresponding timing characteristics are listed in Table 49.

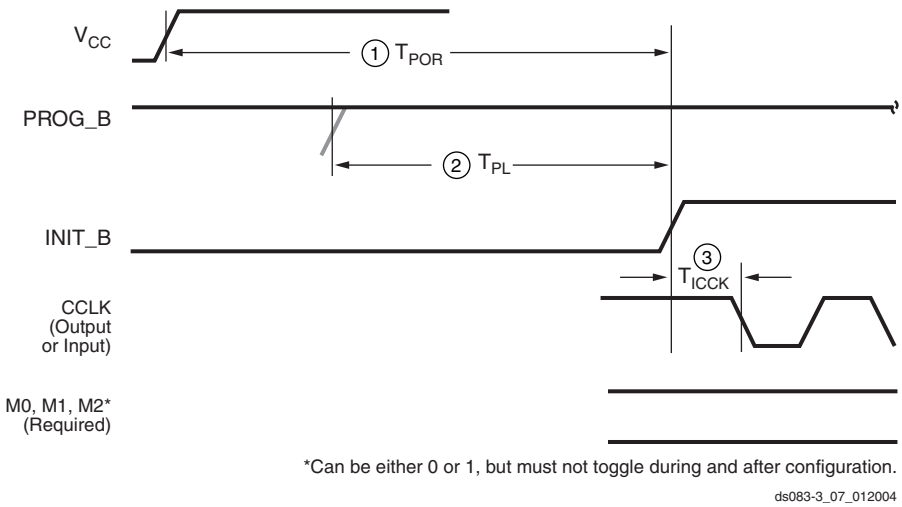


Figure 7: **Configuration Power-Up Timing**

Table 49: **Power-Up Timing Characteristics**

Description	Figure References	Symbol	Value	Units
Power-on reset	1	T_{POR}	T_{PL} + 2	ms, max
Program latency	2	T_{PL}	4	µs per frame, max
CCLK (output) delay	3	T_{ICCK}	0.25	µs, min
			4.00	µs, max
Program pulse width		$T_{PROGRAM}$	300	ns, min

Notes:
1. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	VCCO_7	K7			
7	VCCO_7	J7			
7	VCCO_7	H6			
7	VCCO_7	G6			
N/A	CCLK	W20			
N/A	PROG_B	B1			
N/A	DONE	Y18			
N/A	M0	Y4			
N/A	M1	W3			
N/A	M2	Y5			
N/A	TCK	B22			
N/A	TDI	D3			
N/A	TDO	D20			
N/A	TMS	A21			
N/A	PWRDWN_B	Y19			
N/A	HSWAP_EN	A2			
N/A	RSVD	C18			
N/A	VBATT	C19			
N/A	DXP	C4			
N/A	DXN	C5			
N/A	AVCCAUXTX4	B4	NC	NC	
N/A	VTTXPAD4	B3	NC	NC	
N/A	TXNPAD4	A3	NC	NC	
N/A	TXPPAD4	A4	NC	NC	
N/A	GNDA4	C6	NC	NC	
N/A	RXPPAD4	A5	NC	NC	
N/A	RXNPAD4	A6	NC	NC	
N/A	VTRXPAD4	B5	NC	NC	
N/A	AVCCAUXRX4	B6	NC	NC	
N/A	AVCCAUXTX6	B8			
N/A	VTTXPAD6	B7			
N/A	TXNPAD6	A7			
N/A	TXPPAD6	A8			
N/A	GNDA6	C9			
N/A	RXPPAD6	A9			
N/A	RXNPAD6	A10			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
4	IO_L05_4/No_Pair	Y8			
4	IO_L06N_4/VRP_4	AB8			
4	IO_L06P_4/VRN_4	AB9			
4	IO_L07N_4	AC8			
4	IO_L07P_4/VREF_4	AD8			
4	IO_L08N_4	AE8			
4	IO_L08P_4	AF8			
4	IO_L09N_4	Y9			
4	IO_L09P_4/VREF_4	AA9			
4	IO_L37N_4	AC9	NC	NC	
4	IO_L37P_4	AD9	NC	NC	
4	IO_L38N_4	Y10	NC	NC	
4	IO_L38P_4	W11	NC	NC	
4	IO_L39N_4	AA10	NC	NC	
4	IO_L39P_4	AA11	NC	NC	
4	IO_L43N_4	AB10	NC	NC	
4	IO_L43P_4	AC10	NC	NC	
4	IO_L44N_4	Y11	NC	NC	
4	IO_L44P_4	Y12	NC	NC	
4	IO_L45N_4	AB11	NC	NC	
4	IO_L45P_4/VREF_4	AC11	NC	NC	
4	IO_L67N_4	AA12			
4	IO_L67P_4	AB12			
4	IO_L68N_4	AC12			
4	IO_L68P_4	AD12			
4	IO_L69N_4	W12			
4	IO_L69P_4/VREF_4	W13			
4	IO_L73N_4	Y13			
4	IO_L73P_4	AA13			
4	IO_L74N_4/GCLK3S	AB13			
4	IO_L74P_4/GCLK2P	AC13			
4	IO_L75N_4/GCLK1S	AD13			
4	IO_L75P_4/GCLK0P	AE13			
5	IO_L75N_5/GCLK7S	AE14			
5	IO_L75P_5/GCLK6P	AD14			
5	IO_L74N_5/GCLK5S	AC14			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L52N_6	U22	NC		
6	IO_L53P_6	U23	NC		
6	IO_L53N_6	U24	NC		
6	IO_L54P_6	V26	NC		
6	IO_L54N_6	U26	NC		
6	IO_L55P_6	U20	NC		
6	IO_L55N_6	T19	NC		
6	IO_L56P_6	T20	NC		
6	IO_L56N_6	R20	NC		
6	IO_L57P_6	T21	NC		
6	IO_L57N_6/VREF_6	T22	NC		
6	IO_L58P_6	T23	NC		
6	IO_L58N_6	T24	NC		
6	IO_L59P_6	T25	NC		
6	IO_L59N_6	T26	NC		
6	IO_L60P_6	R19	NC		
6	IO_L60N_6	P19	NC		
6	IO_L85P_6	R21			
6	IO_L85N_6	R22			
6	IO_L86P_6	R23			
6	IO_L86N_6	R24			
6	IO_L87P_6	R25			
6	IO_L87N_6/VREF_6	R26			
6	IO_L88P_6	P20			
6	IO_L88N_6	P21			
6	IO_L89P_6	P22			
6	IO_L89N_6	P23			
6	IO_L90P_6	P24			
6	IO_L90N_6	P25			
7	IO_L90P_7	N25			
7	IO_L90N_7	N24			
7	IO_L89P_7	N23			
7	IO_L89N_7	N22			
7	IO_L88P_7	N21			
7	IO_L88N_7/VREF_7	N20			
7	IO_L87P_7	M26			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
3	IO_L39P_3		AE2	NC		
3	IO_L38N_3		AA7	NC		
3	IO_L38P_3		AA8	NC		
3	IO_L37N_3		AD3	NC		
3	IO_L37P_3		AD4	NC		
3	IO_L36N_3		AF1	NC		
3	IO_L36P_3		AF2	NC		
3	IO_L35N_3		AC5	NC		
3	IO_L35P_3		AC6	NC		
3	IO_L34N_3		AF3	NC		
3	IO_L34P_3		AF4	NC		
3	IO_L33N_3/VREF_3		AE3	NC		
3	IO_L33P_3		AE4	NC		
3	IO_L32N_3		AB7	NC		
3	IO_L32P_3		AB8	NC		
3	IO_L31N_3		AE5	NC		
3	IO_L31P_3		AF6	NC		
3	IO_L06N_3		AG1			
3	IO_L06P_3		AG2			
3	IO_L05N_3		AD5			
3	IO_L05P_3		AD6			
3	IO_L04N_3		AG3			
3	IO_L04P_3		AH4			
3	IO_L03N_3/VREF_3		AH1			
3	IO_L03P_3		AH2			
3	IO_L02N_3		AG5			
3	IO_L02P_3		AH5			
3	IO_L01N_3/VRP_3		AJ3			
3	IO_L01P_3/VRN_3		AK3			
4	IO_L01N_4/BUSY/DOUT(1)		AG6			
4	IO_L01P_4/INIT_B		AF7			
4	IO_L02N_4/D0/DIN(1)		AC9			
4	IO_L02P_4/D1		AD9			
4	IO_L03N_4/D2		AG7			
4	IO_L03P_4/D3		AH7			

FF1152 Flip-Chip Fine-Pitch BGA Package

As shown in Table 10, XC2VP20, XC2VP30, XC2VP40, and XC2VP50 Virtex-II Pro devices are available in the FF1152 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
0	IO_L01N_0/VRP_0	E29				
0	IO_L01P_0/VRN_0	E28				
0	IO_L02N_0	H26				
0	IO_L02P_0	G26				
0	IO_L03N_0	H25				
0	IO_L03P_0/VREF_0	G25				
0	IO_L05_0/No_Pair	J25				
0	IO_L06N_0	K24				
0	IO_L06P_0	J24				
0	IO_L07N_0	F26				
0	IO_L07P_0	E26				
0	IO_L08N_0	D30				
0	IO_L08P_0	D29				
0	IO_L09N_0	K23				
0	IO_L09P_0/VREF_0	J23				
0	IO_L19N_0	F24	NC	NC		
0	IO_L19P_0	E24	NC	NC		
0	IO_L20N_0	D28	NC	NC		
0	IO_L20P_0	C28	NC	NC		
0	IO_L21N_0	H24	NC	NC		
0	IO_L21P_0	G24	NC	NC		
0	IO_L25N_0	G23	NC	NC		
0	IO_L25P_0	F23	NC	NC		
0	IO_L26N_0	E27	NC	NC		
0	IO_L26P_0	D27	NC	NC		
0	IO_L27N_0	K22	NC	NC		
0	IO_L27P_0/VREF_0	J22	NC	NC		
0	IO_L37N_0	H22				
0	IO_L37P_0	G22				
0	IO_L38N_0	D26				
0	IO_L38P_0	C26				
0	IO_L39N_0	K21				
0	IO_L39P_0	J21				
0	IO_L43N_0	F22				

FF1148 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, XC2VP40 and XC2VP50 Virtex-II Pro devices are available in the FF1148 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the FF1148 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

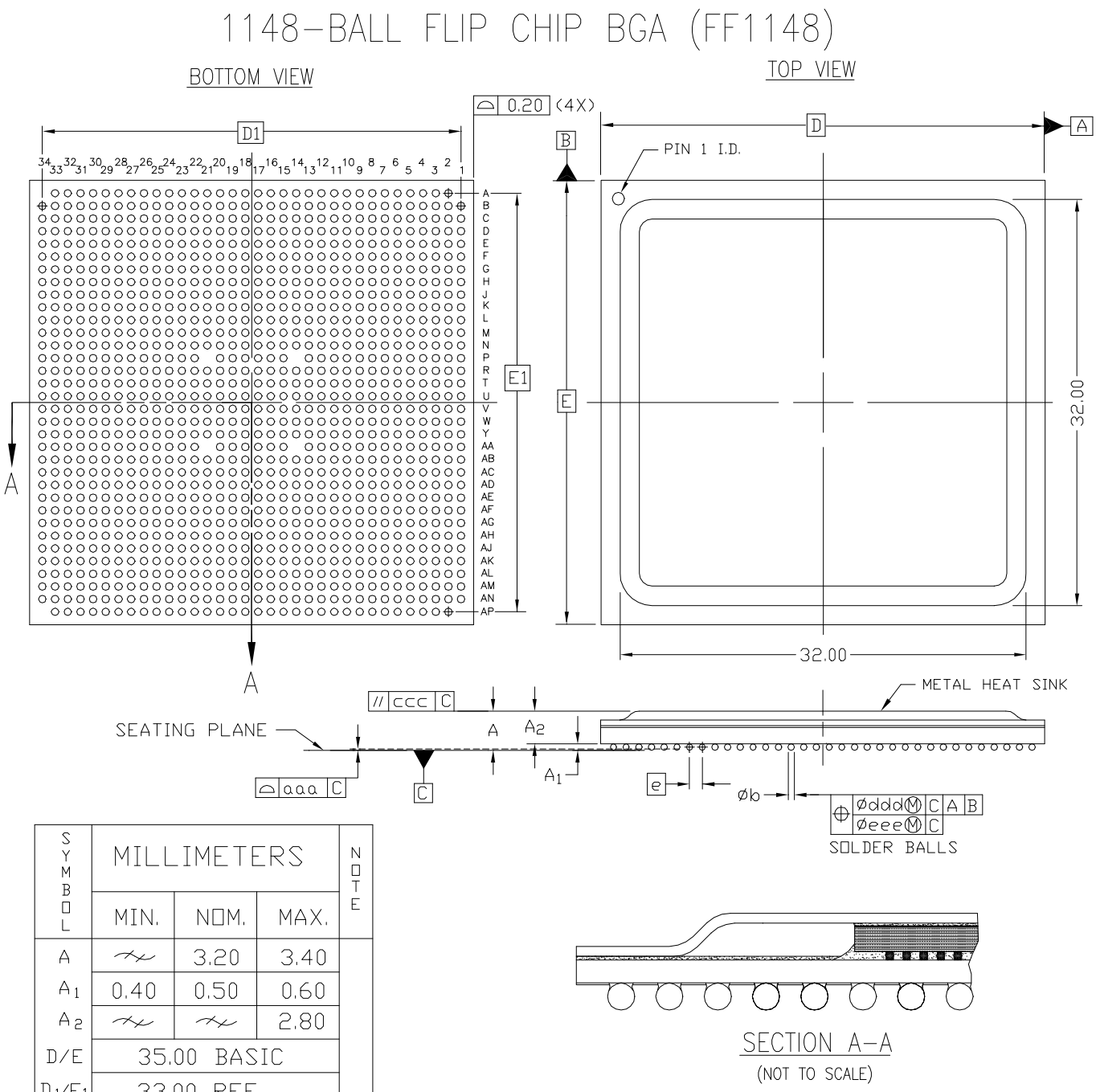
Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L01N_0/VRP_0	E25		
0	IO_L01P_0/VRN_0	F25		
0	IO_L02N_0	J24		
0	IO_L02P_0	K24		
0	IO_L03N_0	C25		
0	IO_L03P_0/VREF_0	D25		
0	IO_L05_0/No_Pair	G25		
0	IO_L06N_0	A25		
0	IO_L06P_0	B25		
0	IO_L07N_0	G24		
0	IO_L07P_0	G23		
0	IO_L08N_0	H23		
0	IO_L08P_0	H22		
0	IO_L09N_0	E24		
0	IO_L09P_0/VREF_0	F24		
0	IO_L19N_0	C24		
0	IO_L19P_0	C23		
0	IO_L20N_0	J23		
0	IO_L20P_0	K23		
0	IO_L21N_0	A24		
0	IO_L21P_0	B24		
0	IO_L25N_0	E23		
0	IO_L25P_0	F23		
0	IO_L26N_0	K22		
0	IO_L26P_0	L22		
0	IO_L27N_0	D23		
0	IO_L27P_0/VREF_0	D22		
0	IO_L37N_0	A23		
0	IO_L37P_0	B23		
0	IO_L38N_0	J21		
0	IO_L38P_0	J20		
0	IO_L39N_0	F22		
0	IO_L39P_0	G22		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	VCCINT	M12		
N/A	VCCINT	AD11		
N/A	VCCINT	L11		
N/A	VCCAUX	AN34		
N/A	VCCAUX	AG34		
N/A	VCCAUX	U34		
N/A	VCCAUX	H34		
N/A	VCCAUX	B34		
N/A	VCCAUX	AP33		
N/A	VCCAUX	A33		
N/A	VCCAUX	AP27		
N/A	VCCAUX	A27		
N/A	VCCAUX	AP17		
N/A	VCCAUX	A17		
N/A	VCCAUX	AP8		
N/A	VCCAUX	A8		
N/A	VCCAUX	AP2		
N/A	VCCAUX	A2		
N/A	VCCAUX	AN1		
N/A	VCCAUX	AG1		
N/A	VCCAUX	U1		
N/A	VCCAUX	H1		
N/A	VCCAUX	B1		
N/A	GND	AK34		
N/A	GND	AF34		
N/A	GND	AB34		
N/A	GND	W34		
N/A	GND	V34		
N/A	GND	T34		
N/A	GND	N34		
N/A	GND	J34		
N/A	GND	E34		
N/A	GND	AN33		
N/A	GND	B33		
N/A	GND	AM32		
N/A	GND	C32		
N/A	GND	AP30		
N/A	GND	AK30		

FF1148 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	---	3.20	3.40	
A_1	0.40	0.50	0.60	
A_2	---	---	2.80	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	---	---	0.20	
ccc	---	---	0.35	
ddd	---	---	0.30	
eee	---	---	0.10	
M	34			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAR-1 (DEPOPULATED)

Figure 7: **FF1148 Flip-Chip Fine-Pitch BGA Package Specifications**

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
1	IO_L01P_1/VRN_1	D9		
2	IO_L01N_2/VRP_2	C7		
2	IO_L01P_2/VRN_2	D7		
2	IO_L02N_2	G9		
2	IO_L02P_2	H9		
2	IO_L03N_2	C5		
2	IO_L03P_2	D5		
2	IO_L04N_2/VREF_2	D6		
2	IO_L04P_2	E6		
2	IO_L05N_2	H8		
2	IO_L05P_2	J9		
2	IO_L06N_2	E7		
2	IO_L06P_2	F7		
2	IO_L73N_2	D1	NC	
2	IO_L73P_2	D2	NC	
2	IO_L75N_2	E2	NC	
2	IO_L75P_2	E3	NC	
2	IO_L76N_2/VREF_2	F5	NC	
2	IO_L76P_2	G5	NC	
2	IO_L78N_2	F3	NC	
2	IO_L78P_2	F4	NC	
2	IO_L79N_2	F1	NC	
2	IO_L79P_2	F2	NC	
2	IO_L81N_2	G6	NC	
2	IO_L81P_2	G7	NC	
2	IO_L82N_2/VREF_2	G3	NC	
2	IO_L82P_2	G4	NC	
2	IO_L84N_2	G1	NC	
2	IO_L84P_2	G2	NC	
2	IO_L07N_2	H6		
2	IO_L07P_2	H7		
2	IO_L08N_2	K8		
2	IO_L08P_2	K9		
2	IO_L09N_2	H2		
2	IO_L09P_2	H3		
2	IO_L10N_2/VREF_2	J6		
2	IO_L10P_2	J7		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L86N_7	W28		
7	IO_L85P_7	W34		
7	IO_L85N_7	W35		
7	IO_L60P_7	W32		
7	IO_L60N_7	W33		
7	IO_L59P_7	W29		
7	IO_L59N_7	W30		
7	IO_L58P_7	V38		
7	IO_L58N_7/VREF_7	V39		
7	IO_L57P_7	V36		
7	IO_L57N_7	V37		
7	IO_L56P_7	V28		
7	IO_L56N_7	V29		
7	IO_L55P_7	V34		
7	IO_L55N_7	V35		
7	IO_L54P_7	V32		
7	IO_L54N_7	V33		
7	IO_L53P_7	V30		
7	IO_L53N_7	V31		
7	IO_L52P_7	U38		
7	IO_L52N_7/VREF_7	U39		
7	IO_L51P_7	T36		
7	IO_L51N_7	U36		
7	IO_L50P_7	V27		
7	IO_L50N_7	U27		
7	IO_L49P_7	U34		
7	IO_L49N_7	U35		
7	IO_L48P_7	T37		
7	IO_L48N_7	T38		
7	IO_L47P_7	U30		
7	IO_L47N_7	U31		
7	IO_L46P_7	T33		
7	IO_L46N_7/VREF_7	T34		
7	IO_L45P_7	R38		
7	IO_L45N_7	R39		
7	IO_L44P_7	T32		
7	IO_L44N_7	U32		
7	IO_L43P_7	R36		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L34N_6		AH38		
6	IO_L35P_6		AH31		
6	IO_L35N_6		AH32		
6	IO_L36P_6		AJ40		
6	IO_L36N_6		AH40		
6	IO_L37P_6		AH41		
6	IO_L37N_6		AH42		
6	IO_L38P_6		AH35		
6	IO_L38N_6		AG35		
6	IO_L39P_6		AG36		
6	IO_L39N_6/VREF_6		AG37		
6	IO_L40P_6		AG38		
6	IO_L40N_6		AG39		
6	IO_L41P_6		AG32		
6	IO_L41N_6		AG33		
6	IO_L42P_6		AG40		
6	IO_L42N_6		AG41		
6	IO_L43P_6		AF33		
6	IO_L43N_6		AF34		
6	IO_L44P_6		AF35		
6	IO_L44N_6		AF36		
6	IO_L45P_6		AF37		
6	IO_L45N_6/VREF_6		AF38		
6	IO_L46P_6		AF39		
6	IO_L46N_6		AF40		
6	IO_L47P_6		AF31		
6	IO_L47N_6		AG31		
6	IO_L48P_6		AF41		
6	IO_L48N_6		AF42		
6	IO_L49P_6		AE35		
6	IO_L49N_6		AE36		
6	IO_L50P_6		AE31		
6	IO_L50N_6		AF32		
6	IO_L51P_6		AE38		
6	IO_L51N_6/VREF_6		AE39		
6	IO_L52P_6		AE41		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	TXPPAD7		A20		
N/A	GNDA7		C21		
N/A	RXPPAD7		A19		
N/A	RXNPAD7		A18		
N/A	VTRXPAD7		B19		
N/A	AVCCAUXRX7		B18		
N/A	AVCCAUXTX8		B16		
N/A	VTTXPAD8		B17		
N/A	TXNPAD8		A17		
N/A	TXPPAD8		A16		
N/A	GNDA8		C16		
N/A	RXPPAD8		A15		
N/A	RXNPAD8		A14		
N/A	VTRXPAD8		B15		
N/A	AVCCAUXRX8		B14		
N/A	AVCCAUXTX9		B12		
N/A	VTTXPAD9		B13		
N/A	TXNPAD9		A13		
N/A	TXPPAD9		A12		
N/A	GNDA9		C12		
N/A	RXPPAD9		A11		
N/A	RXNPAD9		A10		
N/A	VTRXPAD9		B11		
N/A	AVCCAUXRX9		B10		
N/A	AVCCAUXTX10		B8		
N/A	VTTXPAD10		B9		
N/A	TXNPAD10		A9		
N/A	TXPPAD10		A8		
N/A	GNDA10		C8		
N/A	RXPPAD10		A7		
N/A	RXNPAD10		A6		
N/A	VTRXPAD10		B7		
N/A	AVCCAUXRX10		B6		
N/A	AVCCAUXTX11		B4		
N/A	VTTXPAD11		B5		
N/A	TXNPAD11		A5		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	VCCINT		U26		
N/A	VCCINT		U17		
N/A	VCCINT		U16		
N/A	VCCINT		T27		
N/A	VCCINT		T26		
N/A	VCCINT		T25		
N/A	VCCINT		T24		
N/A	VCCINT		T23		
N/A	VCCINT		T22		
N/A	VCCINT		T21		
N/A	VCCINT		T20		
N/A	VCCINT		T19		
N/A	VCCINT		T18		
N/A	VCCINT		T17		
N/A	VCCINT		T16		
N/A	VCCINT		R28		
N/A	VCCINT		R27		
N/A	VCCINT		R26		
N/A	VCCINT		R17		
N/A	VCCINT		R16		
N/A	VCCINT		R15		
N/A	VCCINT		P29		
N/A	VCCINT		P28		
N/A	VCCINT		P27		
N/A	VCCINT		P16		
N/A	VCCINT		P15		
N/A	VCCINT		P14		
N/A	VCCINT		N30		
N/A	VCCINT		N13		
N/A	VCCAUX		AB42		
N/A	VCCAUX		AB41		
N/A	VCCAUX		AB2		
N/A	VCCAUX		AB1		
N/A	VCCAUX		AC42		
N/A	VCCAUX		AC1		
N/A	VCCAUX		AM32		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L67P_3	AU5	
3	IO_L66N_3	AU1	
3	IO_L66P_3	AU2	
3	IO_L65N_3	AJ9	
3	IO_L65P_3	AK8	
3	IO_L64N_3	AU8	
3	IO_L64P_3	AV8	
3	IO_L63N_3/VREF_3	AU7	
3	IO_L63P_3	AV7	
3	IO_L62N_3	AL8	
3	IO_L62P_3	AL9	
3	IO_L61N_3	AU3	
3	IO_L61P_3	AV2	
3	IO_L84N_3	AV6	
3	IO_L84P_3	AW5	
3	IO_L83N_3	AM8	
3	IO_L83P_3	AM9	
3	IO_L82N_3	AV4	
3	IO_L82P_3	AW4	
3	IO_L81N_3/VREF_3	AV3	
3	IO_L81P_3	AW3	
3	IO_L80N_3	AN9	
3	IO_L80P_3	AP8	
3	IO_L79N_3	AW1	
3	IO_L79P_3	AW2	
3	IO_L78N_3	AY7	
3	IO_L78P_3	AY8	
3	IO_L77N_3	AR8	
3	IO_L77P_3	AR9	
3	IO_L76N_3	AW7	
3	IO_L76P_3	AY6	
3	IO_L75N_3/VREF_3	AY3	
3	IO_L75P_3	AY4	
3	IO_L74N_3	AT9	
3	IO_L74P_3	AU9	
3	IO_L73N_3	AY5	
3	IO_L73P_3	BA5	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
4	IO_L58P_4	AW19	
4	IO_L59N_4	AP19	
4	IO_L59P_4	AN19	
4	IO_L60N_4	BB19	
4	IO_L60P_4	BA19	
4	IO_L64N_4	AU20	
4	IO_L64P_4	AT20	
4	IO_L65N_4	AL21	
4	IO_L65P_4	AL20	
4	IO_L66N_4	BA20	
4	IO_L66P_4/VREF_4	AY20	
4	IO_L67N_4	AR21	
4	IO_L67P_4	AP21	
4	IO_L68N_4	AN20	
4	IO_L68P_4	AM20	
4	IO_L69N_4	AU21	
4	IO_L69P_4/VREF_4	AT21	
4	IO_L73N_4	AW21	
4	IO_L73P_4	AV21	
4	IO_L74N_4/GCLK3S	AN21	
4	IO_L74P_4/GCLK2P	AM21	
4	IO_L75N_4/GCLK1S	BA21	
4	IO_L75P_4/GCLK0P	AY21	
5	IO_L75N_5/GCLK7S	AY22	
5	IO_L75P_5/GCLK6P	BA22	
5	IO_L74N_5/GCLK5S	AM22	
5	IO_L74P_5/GCLK4P	AN22	
5	IO_L73N_5	AV22	
5	IO_L73P_5	AW22	
5	IO_L69N_5/VREF_5	AT22	
5	IO_L69P_5	AU22	
5	IO_L68N_5	AM23	
5	IO_L68P_5	AN23	
5	IO_L67N_5	AP22	
5	IO_L67P_5	AR22	
5	IO_L66N_5/VREF_5	AY23	