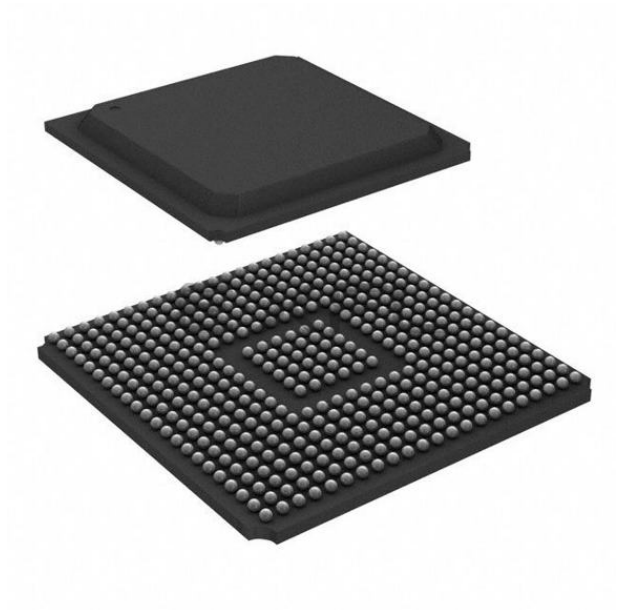

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 352 |
| Number of Logic Elements/Cells | 3168 |
| Total RAM Bits | 221184 |
| Number of I/O | 156 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 456-BBGA |
| Supplier Device Package | 456-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2vp2-6fg456c |

  - HyperTransport (LDT) I/O with current driver buffers
  - Built-in DDR input and output registers
- Proprietary high-performance SelectLink technology for communications between Xilinx devices
  - High-bandwidth data path
  - Double Data Rate (DDR) link
  - Web-based HDL generation methodology
- SRAM-Based In-System Configuration
  - Fast SelectMAP™ configuration
  - Triple Data Encryption Standard (DES) security option (bitstream encryption)
  - IEEE 1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Integrated VHDL and Verilog design flows
  - ChipScope™ Integrated Logic Analyzer
- 0.13 µm Nine-Layer Copper Process with 90 nm High-Speed Transistors
- 1.5V ($V_{CCINT}$) core power supply, dedicated 2.5V $V_{CCAUX}$ auxiliary and $V_{CCO}$ I/O power supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) Packages in Standard 1.00 mm Pitch.
- Wire-Bond BGA Devices Available in Pb-Free Packaging (**www.xilinx.com/pbfree)**
- Each Device 100% Factory Tested

# General Description

The Virtex-II Pro and Virtex-II Pro X families contain platform FPGAs for designs that are based on IP cores and customized modules. The family incorporates multi-gigabit transceivers and PowerPC CPU blocks in Virtex-II Pro Series FPGA architecture. It empowers complete solutions for telecommunication, wireless, networking, video, and DSP applications.

The leading-edge 0.13 µm CMOS nine-layer copper process and Virtex-II Pro architecture are optimized for high performance designs in a wide range of densities. Combining a wide variety of flexible features and IP cores, the Virtex-II Pro family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gate arrays.

# Architecture

## Array Overview

Virtex-II Pro and Virtex-II Pro X devices are user-programmable gate arrays with various configurable elements and embedded blocks optimized for high-density and high-performance system designs. Virtex-II Pro devices implement the following functionality:

- Embedded high-speed serial transceivers enable data bit rate up to 3.125 Gb/s per channel (RocketIO) or 6.25 Gb/s (RocketIO X).
- Embedded IBM PowerPC 405 RISC processor blocks provide performance up to 400 MHz.
- SelectIO-Ultra blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.
- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM+ memory modules provide large 18 Kb storage elements of True Dual-Port RAM.
- Embedded multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, and coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and supports high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

## Features

This section briefly describes Virtex-II Pro / Virtex-II Pro X features. For more details, refer to Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description.

### *RocketIO / RocketIO X MGT Cores*

The RocketIO and RocketIO X Multi-Gigabit Transceivers are flexible parallel-to-serial and serial-to-parallel embedded transceiver cores used for high-bandwidth interconnection between buses, backplanes, or other subsystems.

Multiple user instantiations in an FPGA are possible, providing up to 100 Gb/s (RocketIO) or 170 Gb/s (RocketIO X) of full-duplex raw data transfer. Each channel can be operated at a maximum data transfer rate of 3.125 Gb/s (RocketIO) or 6.25 Gb/s (RocketIO X).

RXP and RXN as shown in Figure 5. This supports multiple termination styles, including high-side, low-side, and differential (floating or active). This configuration supports receiver termination compatible to Virtex-II Pro devices, using a CML (high-side) termination to an active supply of 1.8V – 2.5V. For DC coupling of two Virtex-II Pro X devices, a 1.5V CML termination for VTRX is recommended.

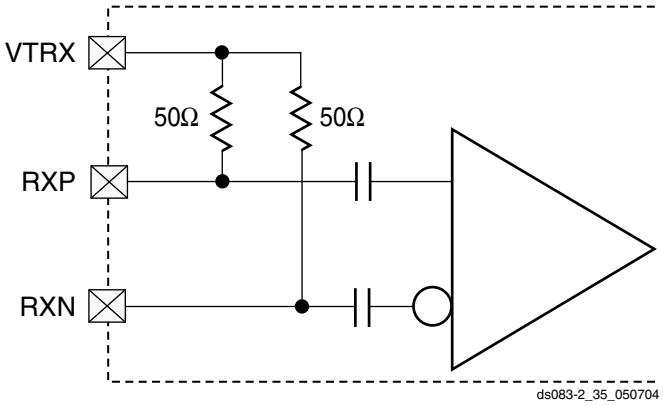


*Figure 5:* **RocketIO X Receive Termination**

## PCS

### *Fabric Data Interface*

Internally, the PCS operates in either 2-byte mode (16/20 bits) or 4-byte mode (32/40 bits). When in 2-byte mode, the FPGA fabric interface can either be 1, 2, or 4 bytes wide. When in 4-byte mode, the FPGA fabric interface can either be 4 or 8 bytes wide. When accompanied by the predefined modes of the PMA, the user thus has a large combination of protocols and data rates from which to choose.

USRCLK2 clocks data on the fabric side, while USRCLK clocks data on the PCS side. This creates distinct USRCLK/USRCLK2 frequency ratios for different combinations of fabric and internal data widths. Table 2 summarizes the USRCLK2-to-USRCLK ratios for the different possible combinations of data widths.

*Table 2:* **Clock Ratios for Various Data Widths**

| Fabric Data Width | Frequency Ratio of USRCLK:USRCLK2 | |
|---|---|---|
| | 2-Byte Internal Data Width | 4-Byte Internal Data Width |
| 1 byte | 1:2 (1) | N/A |
| 2 byte | 1:1 | N/A |
| 4 byte | 2:1 (1) | 1:1 |
| 8 byte | N/A | 2:1 (1) |

**Notes:**
1. Each edge of slower clock must align with falling edge of faster clock.

As a general guide, use 2-byte internal data width mode when the serial speed is below 5 Gb/s, and 4-byte internal data width mode when the serial speed is greater than 5 Gb/s. In 2-byte mode, the PCS processes 4-byte data every other byte.

No fixed phase relationship is assumed between REFCLK, RXRECCLK, and/or any other clock that is not tied to either of these clocks. When RXUSRCLK and RXUSRCLK2 have different frequencies, each edge of the slower clock is aligned to a falling edge of the faster clock. The same relationships apply to TXUSRCLK and TXUSRCLK2.

### *FPGA Transmit Interface*

The FPGA can send either one, two, or four characters of data to the transmitter. Each character can be either 8 bits or 10 bits wide. If 8-bit data is applied, the additional inputs become control signals for the 8B/10B encoder. When the 8B/10B encoder is bypassed, the 10-bit character order is generated as follows:

TXCHARDISPMODE[0] (first bit transmitted)
TXCHARDISPVAL[0]
TXDATA[7:0] (last bit transmitted is TXDATA[0])

### *64B/66B Encoder/Decoder*

The RocketIO X PCS features a 64B/66B encoder/decoder, scrambler/descrambler, and gearbox functions that can be bypassed as needed. The encoder is compliant with IEEE 802.3ae specifications.

### *Scrambler/Gearbox*

The bypassable scrambler operates on the read side of the transmit FIFO. The scrambler uses the following generator polynomial to scramble 64B/66B payload data:

$$G(x) = 1 + x^{39} + x^{58}$$

The scrambler works in conjunction with the gearbox, which frames 64B/66B data for the PMA. The gearbox should always be enabled when using the 64B/66B protocal.

memory protection. Working with appropriate system-level software, the MMU provides the following functions:

- Translation of the 4 GB effective address space into physical addresses
- Independent enabling of instruction and data translation/protection
- Page-level access control using the translation mechanism
- Software control of page replacement strategy
- Additional control over protection using zones
- Storage attributes for cache policy and speculative memory access control

The MMU can be disabled under software control. If the MMU is not used, the PPC405 core provides other storage control mechanisms.

### *Translation Look-Aside Buffer (TLB)*

The Translation Look-Aside Buffer (TLB) is the hardware resource that controls translation and protection. It consists of 64 entries, each specifying a page to be translated. The TLB is fully associative; a given page entry can be placed anywhere in the TLB. The translation function of the MMU occurs pre-cache. Cache tags and indexing use physical addresses.

Software manages the establishment and replacement of TLB entries. This gives system software significant flexibility in implementing a custom page replacement strategy. For example, to reduce TLB thrashing or translation delays, software can reserve several TLB entries in the TLB for globally accessible static mappings. The instruction set provides several instructions used to manage TLB entries. These instructions are privileged and require the software to be executing in supervisor state. Additional TLB instructions are provided to move TLB entry fields to and from GPRs.

The MMU divides logical storage into pages. Eight page sizes (1 KB, 4 KB, 16 KB, 64 KB, 256 KB, 1 MB, 4 MB, and 16 MB) are simultaneously supported, such that, at any given time, the TLB can contain entries for any combination of page sizes. In order for a logical to physical translation to exist, a valid entry for the page containing the logical address must be in the TLB. Addresses for which no TLB entry exists cause TLB-Miss exceptions.

To improve performance, four instruction-side and eight data-side TLB entries are kept in shadow arrays. The shadow arrays allow single-cycle address translation and also help to avoid TLB contention between load/store and instruction fetch operations. Hardware manages the replacement and invalidation of shadow-TLB entries; no system software action is required.

### *Memory Protection*

When address translation is enabled, the translation mechanism provides a basic level of protection.

The Zone Protection Register (ZPR) enables the system software to override the TLB access controls. For example, the ZPR provides a way to deny read access to application programs. The ZPR can be used to classify storage by type; access by type can be changed without manipulating individual TLB entries.

The PowerPC Architecture provides WIU0GE (write-back / write-through, cacheability, user-defined 0, guarded, endian) storage attributes that control memory accesses, using bits in the TLB or, when address translation is disabled, storage attribute control registers.

When address translation is enabled, storage attribute control bits in the TLB control the storage attributes associated with the current page. When address translation is disabled, bits in each storage attribute control register control the storage attributes associated with storage regions. Each storage attribute control register contains 32 fields. Each field sets the associated storage attribute for a 128 MB memory region.

## Timers

The embedded PPC405 core contains a 64-bit time base and three timers, as shown in Figure 17:

- Programmable Interval Timer (PIT)
- Fixed Interval Timer (FIT)
- Watchdog Timer (WDT)

The time base counter increments either by an internal signal equal to the CPU clock rate or by a separate external timer clock signal. No interrupts are generated when the time base rolls over. The three timers are synchronous with the time base.

The PIT is a 32-bit register that decrements at the same rate as the time base is incremented. The user loads the PIT register with a value to create the desired delay. When the register reaches zero, the timer stops decrementing and generates a PIT interrupt. Optionally, the PIT can be programmed to auto-reload the last value written to the PIT register, after which the PIT continues to decrement.

The FIT generates periodic interrupts based on one of four selectable bits in the time base. When the selected bit changes from 0 to 1, the PPC405 core generates a FIT interrupt.

The WDT provides a periodic critical-class interrupt based on a selected bit in the time base. This interrupt can be used for system error recovery in the event of software or system lockups. Users may select one of four time periods for the interval and the type of reset generated if the WDT expires twice without an intervening clear from software. If enabled, the watchdog timer generates a reset unless an exception handler updates the WDT status bit before the timer has completed two of the selected timer intervals.

### *Digitally Controlled Impedance (DCI)*

Today's chip output signals with fast edge rates require termination to prevent reflections and maintain signal integrity. High pin count packages (especially ball grid arrays) can not accommodate external termination resistors.

Virtex-II Pro XCITE DCI provides controlled impedance drivers and on-chip termination for single-ended and differential I/Os. This eliminates the need for external resistors and improves signal integrity. The DCI feature can be used on any IOB by selecting one of the DCI I/O standards.

When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination.

DCI operates independently on each I/O bank. When a DCI I/O standard is used in a particular I/O bank, external reference resistors must be connected to two dual-function pins on the bank. These resistors, voltage reference of N transistor (VRN) and the voltage reference of P transistor (VRP) are shown in Figure 26.

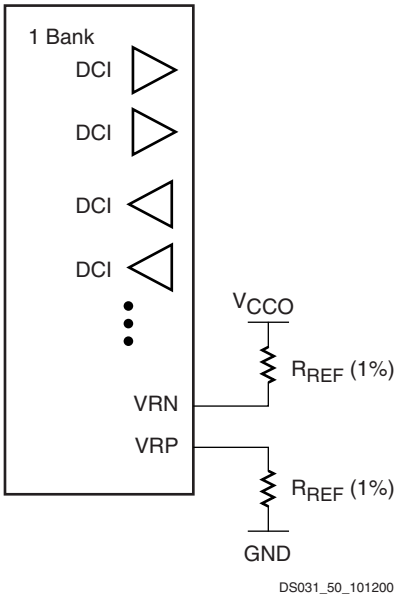


*Figure 26:* **DCI in a Virtex-II Pro Bank**

When used with a terminated I/O standard, the value of the resistors are specified by the standard (typically 50Ω). When used with a controlled impedance driver, the resistors set the output impedance of the driver within the specified range (20Ω to 100Ω). For all series and parallel terminations listed in Table 13 and Table 14, the reference resistors must have the same value for any given bank. One percent resistors are recommended.

The DCI system adjusts the I/O impedance to match the two external reference resistors, or half of the reference resistors, and compensates for impedance changes due to voltage and/or temperature fluctuations. The adjustment is done by turning parallel transistors in the IOB on or off.

#### Controlled Impedance Drivers (Series Termination)

DCI can be used to provide a buffer with a controlled output impedance. It is desirable for this output impedance to match the transmission line impedance ($Z_0$). Virtex-II Pro input buffers also support LVDCI and LVDCI_DV2.

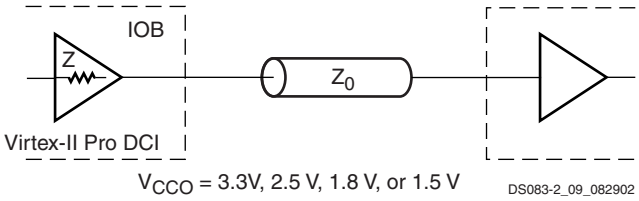


*Figure 27:* **Internal Series Termination**

*Table 13:* **SelectIO-Ultra Controlled Impedance Buffers**

| $V_{CCO}$ | DCI | DCI Half Impedance |
|---|---|---|
| 3.3V | LVDCI_33 | N/A |
| 2.5V | LVDCI_25 | LVDCI_DV2_25 |
| 1.8V | LVDCI_18 | LVDCI_DV2_18 |
| 1.5V | LVDCI_15 | LVDCI_DV2_15 |

#### Controlled Impedance Terminations (Parallel)

DCI also provides on-chip termination for SSTL2, SSTL18, HSTL (Class I, II, III, or IV), LVDS_25, LVDSEXT_25, and GTL/GTLP receivers or transmitters on bidirectional lines. Table 14 and Table 15 list the on-chip parallel terminations available in Virtex-II Pro devices. $V_{CCO}$ must be set according to Table 10. There is a $V_{CCO}$ requirement for GTL_DCI and GTLP_DCI, due to the on-chip termination resistor.

*Table 14:* **SelectIO-Ultra Buffers With On-Chip Parallel Termination**

| I/O Standard Description | IOSTANDARD Attribute | |
|---|---|---|
| | External Termination | On-Chip Termination |
| SSTL Class I, 2.5V | SSTL2_I | SSTL2_I_DCI(1) |
| SSTL Class II, 2.5V | SSTL2_II | SSTL2_II_DCI(1) |
| SSTL Class I, 1.8V | SSTL18_I | SSTL18_I_DCI |
| SSTL Class II, 1.8V | SSTL18_II | SSTL18_II_DCI |
| HSTL Class I | HSTL_I | HSTL_I_DCI |
| HSTL Class I, 1.8V | HSTL_I_18 | HSTL_I_DCI_18 |
| HSTL Class II | HSTL_II | HSTL_II_DCI |
| HSTL Class II, 1.8V | HSTL_II_18 | HSTL_II_DCI_18 |
| HSTL Class III | HSTL_III | HSTL_III_DCI |
| HSTL Class III, 1.8V | HSTL_III_18 | HSTL_III_DCI_18 |
| HSTL Class IV | HSTL_IV | HSTL_IV_DCI |
| HSTL Class IV, 1.8V | HSTL_IV_18 | HSTL_IV_DCI_18 |
| GTL | GTL | GTL_DCI |
| GTL Plus | GTLP | GTLP_DCI |

**Notes:**
1. SSTL compatible.

## IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVCMOS 2.5V levels. For other standards, adjust the delays with the values shown in IOB Input Switching Characteristics Standard Adjustments.

*Table 35:* **IOB Input Switching Characteristics**

| | | | Speed Grade | | | |
|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Device** | **-7** | **-6** | **-5** | **Units** |
| **Propagation Delays** | | | | | | |
| Pad to I output, no delay | $T_{IOPI}$ | All | 0.84 | 0.87 | 0.91 | ns, max |
| Pad to I output, with delay | $T_{IOPID}$ | XC2VP2 | 1.84 | 1.94 | 2.06 | ns, max |
| | | XC2VP4 | 1.84 | 1.94 | 2.06 | ns, max |
| | | XC2VP7 | 1.84 | 1.94 | 2.06 | ns, max |
| | | XC2VP20 | 2.14 | 2.23 | 2.37 | ns, max |
| | | XC2VPX20 | 2.14 | 2.23 | 2.37 | ns, max |
| | | XC2VP30 | 2.14 | 2.26 | 2.46 | ns, max |
| | | XC2VP40 | 2.54 | 2.67 | 2.81 | ns, max |
| | | XC2VP50 | 2.54 | 2.68 | 2.87 | ns, max |
| | | XC2VP70 | 2.54 | 2.72 | 2.91 | ns, max |
| | | XC2VPX70 | 2.54 | 2.72 | 2.91 | ns, max |
| | | XC2VP100 | N/A | 4.71 | 4.80 | ns, max |
| **Propagation Delays** | | | | | | |
| Pad to output IQ via transparent latch, no delay | $T_{IOPLI}$ | All | 0.86 | 0.89 | 0.93 | ns, max |
| Pad to output IQ via transparent latch, with delay | $T_{IOPLID}$ | XC2VP2 | 2.30 | 2.62 | 2.97 | ns, max |
| | | XC2VP4 | 2.57 | 2.89 | 3.23 | ns, max |
| | | XC2VP7 | 2.50 | 2.84 | 3.17 | ns, max |
| | | XC2VP20 | 2.65 | 3.04 | 3.42 | ns, max |
| | | XC2VPX20 | 2.65 | 3.04 | 3.42 | ns, max |
| | | XC2VP30 | 2.69 | 3.12 | 3.51 | ns, max |
| | | XC2VP40 | 3.30 | 3.63 | 4.03 | ns, max |
| | | XC2VP50 | 3.86 | 4.10 | 4.45 | ns, max |
| | | XC2VP70 | 4.00 | 4.25 | 4.57 | ns, max |
| | | XC2VPX70 | 4.00 | 4.25 | 4.57 | ns, max |
| | | XC2VP100 | N/A | 6.50 | 7.06 | ns, max |
| Clock CLK to output IQ | $T_{IOCKIQ}$ | All | 0.60 | 0.60 | 0.67 | ns, max |

*Table 38:* **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

| Description | IOSTANDARD Attribute | Timing Parameter | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -7 | -6 | -5 | |
| HSTL, Class II | HSTL_II | $T_{OHSTL\_II}$ | 0.30 | 0.35 | 0.38 | ns |
| HSTL, Class III | HSTL_III | $T_{OHSTL\_IIII}$ | 0.31 | 0.35 | 0.39 | ns |
| HSTL, Class IV | HSTL_IV | $T_{OHSTL\_IV}$ | 0.15 | 0.17 | 0.19 | ns |
| HSTL, Class I, 1.8V | HSTL_I_18 | $T_{OHSTL\_I\_18}$ | 0.56 | 0.64 | 0.70 | ns |
| HSTL, Class II, 1.8V | HSTL_II_18 | $T_{OHSTL\_II\_18}$ | 0.30 | 0.35 | 0.38 | ns |
| HSTL, Class III, 1.8V | HSTL_III_18 | $T_{OHSTL\_IIII\_18}$ | 0.36 | 0.41 | 0.45 | ns |
| HSTL, Class IV, 1.8V | HSTL_IV_18 | $T_{OHSTL\_IV\_18}$ | 0.19 | 0.22 | 0.24 | ns |
| SSTL (Stub Series Terminated Logic), Class I, 1.8V | SSTL18_I | $T_{OSSTL18\_I}$ | 0.80 | 0.92 | 1.01 | ns |
| SSTL, Class II, 1.8V | SSTL18_II | $T_{OSSTL18\_II}$ | 0.45 | 0.51 | 0.56 | ns |
| SSTL, Class I, 2.5V | SSTL2_I | $T_{OSSTL2\_I}$ | 0.63 | 0.72 | 0.79 | ns |
| SSTL, Class II, 2.5V | SSTL2_II | $T_{OSSTL2\_II}$ | 0.22 | 0.25 | 0.27 | ns |
| LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V | LVDCI_33 | $T_{OLVDCI\_33}$ | 0.72 | 0.83 | 0.91 | ns |
| LVDCI, 2.5V | LVDCI_25 | $T_{OLVDCI\_25}$ | 0.56 | 0.64 | 0.71 | ns |
| LVDCI, 1.8V | LVDCI_18 | $T_{OLVDCI\_18}$ | 0.65 | 0.75 | 0.82 | ns |
| LVDCI, 1.5V | LVDCI_15 | $T_{OLVDCI\_15}$ | 1.00 | 1.15 | 1.26 | ns |
| LVDCI, 2.5V, Half-Impedance | LVDCI_DV2_25 | $T_{OLVDCI\_DV2\_25}$ | 0.06 | 0.07 | 0.08 | ns |
| LVDCI, 1.8V, Half-Impedance | LVDCI_DV2_18 | $T_{OLVDCI\_DV2\_18}$ | 0.30 | 0.34 | 0.38 | ns |
| LVDCI, 1.5V, Half-Impedance | LVDCI_DV2_15 | $T_{OLVDCI\_DV2\_15}$ | 0.60 | 0.69 | 0.76 | ns |
| HSLVDCI (High-Speed Low-Voltage DCI), 1.5V | HSLVDCI_15 | $T_{OHSLVDCI\_15}$ | 1.00 | 1.15 | 1.26 | ns |
| HSLVDCI, 1.8V | HSLVDCI_18 | $T_{OHSLVDCI\_18}$ | 0.65 | 0.75 | 0.82 | ns |
| HSLVDCI, 2.5V | HSLVDCI_25 | $T_{OHSLVDCI\_25}$ | 0.56 | 0.64 | 0.71 | ns |
| HSLVDCI, 3.3V | HSLVDCI_33 | $T_{OHSLVDCI\_33}$ | 0.72 | 0.83 | 0.91 | ns |
| GTL (Gunning Transceiver Logic) with DCI | GTL_DCI | $T_{OGTL\_DCI}$ | 1.21 | 1.39 | 1.53 | ns |
| GTL Plus with DCI | GTLP_DCI | $T_{OGTLP\_DCI}$ | 0.05 | 0.06 | 0.07 | ns |
| HSTL (High-Speed Transceiver Logic), Class I, with DCI | HSTL_I_DCI | $T_{OHSTL\_I\_DCI}$ | 0.55 | 0.63 | 0.69 | ns |
| HSTL, Class II, with DCI | HSTL_II_DCI | $T_{OHSTL\_II\_DCI}$ | 0.47 | 0.54 | 0.60 | ns |
| HSTL, Class III, with DCI | HSTL_III_DCI | $T_{OHSTL\_III\_DCI}$ | 0.31 | 0.36 | 0.40 | ns |
| HSTL, Class IV, with DCI | HSTL_IV_DCI | $T_{OHSTL\_IV\_DCI}$ | 1.81 | 2.08 | 2.29 | ns |
| HSTL, Class I, 1.8V, with DCI | HSTL_I_DCI_18 | $T_{OHSTL\_I\_DCI\_18}$ | 0.55 | 0.63 | 0.70 | ns |
| HSTL, Class II, 1.8V, with DCI | HSTL_II_DCI_18 | $T_{OHSTL\_II\_DCI\_18}$ | 0.24 | 0.28 | 0.31 | ns |
| HSTL, Class III, 1.8V, with DCI | HSTL_III_DCI_18 | $T_{OHSTL\_III\_DCI\_18}$ | 0.35 | 0.40 | 0.44 | ns |
| HSTL, Class IV, 1.8V, with DCI | HSTL_IV_DCI_18 | $T_{OHSTL\_IV\_DCI\_18}$ | 1.48 | 1.70 | 1.87 | ns |
| SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI | SSTL18_I_DCI | $T_{OSSTL18\_I\_DCI}$ | 0.54 | 0.62 | 0.68 | ns |
| SSTL, Class II, 1.8V, with DCI | SSTL18_II_DCI | $T_{OSSTL18\_II\_DCI}$ | 0.24 | 0.28 | 0.31 | ns |
| SSTL, Class I, 2.5V, with DCI | SSTL2_I_DCI | $T_{OSSTL2\_I\_DCI}$ | 0.48 | 0.56 | 0.61 | ns |
| SSTL, Class II, 2.5V, with DCI | SSTL2_II_DCI | $T_{OSSTL2\_II\_DCI}$ | 0.48 | 0.56 | 0.61 | ns |

*Table 40:* **Output Delay Measurement Methodology**

| Description | IOSTANDARD Attribute | $R_{REF}$ (Ω) | $C_{REF}$[1] (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| SSTL (Stub Series Terminated Logic), Class I, 1.8V | SSTL18_I | 50 | 0 | $V_{REF}$ | 0.9 |
| SSTL, Class II, 1.8V | SSTL18_II | 25 | 0 | $V_{REF}$ | 0.9 |
| SSTL, Class I, 2.5V | SSTL2_I | 50 | 0 | $V_{REF}$ | 1.25 |
| SSTL, Class II, 2.5V | SSTL2_II | 25 | 0 | $V_{REF}$ | 1.25 |
| LVDS (Low-Voltage Differential Signaling), 2.5V | LVDS_25 | 50 | 0 | $V_{REF}$ | 1.2 |
| LVDSEXT (LVDS Extended Mode), 2.5V | LVDSEXT_25 | 50 | 0 | $V_{REF}$ | 1.2 |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | 1M | 0 | 1.2 | 0 |
| LDT (HyperTransport), 2.5V | LDT_25 | 50 | 0 | $V_{REF}$ | 0.6 |
| LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V | LVPECL_25 | 1M | 0 | 1.23 | 0 |
| LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V | LVDCI_33 | 1M | 0 | 1.65 | 0 |
| LVDCI/HSLVDCI, 2.5V | LVDCI_25 | 1M | 0 | 1.25 | 0 |
| LVDCI/HSLVDCI, 1.8V | LVDCI_18 | 1M | 0 | 0.9 | 0 |
| LVDCI/HSLVDCI, 1.5V | LVDCI_15 | 1M | 0 | 0.75 | 0 |
| HSTL (High-Speed Transceiver Logic), Class I & II, with DCI | HSTL_I_DCI, HSTL_II_DCI | 50 | 0 | $V_{REF}$ | 0.75 |
| HSTL, Class III & IV, with DCI | HSTL_III_DCI, HSTL_IV_DCI | 50 | 0 | 0.9 | 1.5 |
| HSTL, Class I & II, 1.8V, with DCI | HSTL_I_DCI_18, HSTL_II_DCI_18 | 50 | 0 | $V_{REF}$ | 0.9 |
| HSTL, Class III & IV, 1.8V, with DCI | HSTL_III_DCI_18, HSTL_IV_DCI_18 | 50 | 0 | 1.1 | 1.8 |
| SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI | SSTL18_I_DCI, SSTL18_II_DCI | 50 | 0 | $V_{REF}$ | 0.9 |
| SSTL, Class I & II, 2.5V, with DCI | SSTL2_I_DCI, SSTL2_II_DCI | 50 | 0 | $V_{REF}$ | 1.25 |
| GTL (Gunning Transceiver Logic) with DCI | GTL_DCI | 50 | 0 | 0.8 | 1.2 |
| GTL Plus with DCI | GTLP_DCI | 50 | 0 | 1.0 | 1.5 |

**Notes:**
1. $C_{REF}$ is the capacitance of the probe, nominally 0 pF.
2. Measured as per PCI specification.
3. Measured as per PCI-X specification.

*Table 7:* **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 |
| N/A | GND | R15 | | | |
| N/A | GND | R16 | | | |
| N/A | GND | R24 | | | |
| N/A | GND | T11 | | | |
| N/A | GND | T12 | | | |
| N/A | GND | T13 | | | |
| N/A | GND | T14 | | | |
| N/A | GND | T15 | | | |
| N/A | GND | T16 | | | |
| N/A | GND | U6 | | | |
| N/A | GND | U21 | | | |
| N/A | GND | W4 | | | |
| N/A | GND | W23 | | | |
| N/A | GND | AA10 | | | |
| N/A | GND | AA17 | | | |
| N/A | GND | AC4 | | | |
| N/A | GND | AC8 | | | |
| N/A | GND | AC19 | | | |
| N/A | GND | AC23 | | | |
| N/A | GND | AD3 | | | |
| N/A | GND | AD24 | | | |
| N/A | GND | AE2 | | | |
| N/A | GND | AE25 | | | |
| N/A | GND | AF1 | | | |
| N/A | GND | AF26 | | | |

**Notes:**
1. See Table 4 for an explanation of the signals available on this pin.

*Table 8:* **FF672 — XC2VP2, XC2VP4, and XC2VP7**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP2 | XC2VP4 | XC2VP7 |
| 5 | IO_L74P_5/GCLK4P | AB14 | | | |
| 5 | IO_L73N_5 | AA14 | | | |
| 5 | IO_L73P_5 | Y14 | | | |
| 5 | IO_L69N_5/VREF_5 | W14 | | | |
| 5 | IO_L69P_5 | W15 | | | |
| 5 | IO_L68N_5 | AD15 | | | |
| 5 | IO_L68P_5 | AC15 | | | |
| 5 | IO_L67N_5 | AB15 | | | |
| 5 | IO_L67P_5 | AA15 | | | |
| 5 | IO_L45N_5/VREF_5 | AC16 | NC | NC | |
| 5 | IO_L45P_5 | AB16 | NC | NC | |
| 5 | IO_L44N_5 | Y15 | NC | NC | |
| 5 | IO_L44P_5 | Y16 | NC | NC | |
| 5 | IO_L43N_5 | AC17 | NC | NC | |
| 5 | IO_L43P_5 | AB17 | NC | NC | |
| 5 | IO_L39N_5 | AA16 | NC | NC | |
| 5 | IO_L39P_5 | AA17 | NC | NC | |
| 5 | IO_L38N_5 | W16 | NC | NC | |
| 5 | IO_L38P_5 | Y17 | NC | NC | |
| 5 | IO_L37N_5 | AD18 | NC | NC | |
| 5 | IO_L37P_5 | AC18 | NC | NC | |
| 5 | IO_L09N_5/VREF_5 | AA18 | | | |
| 5 | IO_L09P_5 | Y18 | | | |
| 5 | IO_L08N_5 | AF19 | | | |
| 5 | IO_L08P_5 | AE19 | | | |
| 5 | IO_L07N_5/VREF_5 | AD19 | | | |
| 5 | IO_L07P_5 | AC19 | | | |
| 5 | IO_L06N_5/VRP_5 | AB18 | | | |
| 5 | IO_L06P_5/VRN_5 | AB19 | | | |
| 5 | IO_L05_5/No_Pair | Y19 | | | |
| 5 | IO_L03N_5/D4 | AA19 | | | |
| 5 | IO_L03P_5/D5 | AA20 | | | |
| 5 | IO_L02N_5/D6 | AC20 | | | |
| 5 | IO_L02P_5/D7 | AB20 | | | |
| 5 | IO_L01N_5/RDWR_B | AD21 | | | |
| 5 | IO_L01P_5/CS_B | AC21 | | | |

*Table 9:* **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

| Bank | Pin Description | | Pin Number | No Connects | | |
|---|---|---|---|---|---|---|
| | Virtex-II Pro devices | XC2VPX20 (if Different) | | XC2VP7 | XC2VP20, XC2VPX20 | XC2VP30 |
| 4 | IO_L05_4/No_Pair | | AD8 | | | |
| 4 | IO_L06N_4/VRP_4 | | AG8 | | | |
| 4 | IO_L06P_4/VRN_4 | | AH8 | | | |
| 4 | IO_L07N_4 | | AC10 | | | |
| 4 | IO_L07P_4/VREF_4 | | AD10 | | | |
| 4 | IO_L08N_4 | | AE7 | | | |
| 4 | IO_L08P_4 | | AE8 | | | |
| 4 | IO_L09N_4 | | AJ8 | | | |
| 4 | IO_L09P_4/VREF_4 | | AK8 | | | |
| 4 | IO_L37N_4 | | AC11 | | | |
| 4 | IO_L37P_4 | | AD11 | | | |
| 4 | IO_L38N_4 | | AF8 | | | |
| 4 | IO_L38P_4 | | AF9 | | | |
| 4 | IO_L39N_4 | | AF10 | | | |
| 4 | IO_L39P_4 | | AG10 | | | |
| 4 | IO_L43N_4 | | AC12 | | | |
| 4 | IO_L43P_4 | | AD12 | | | |
| 4 | IO_L44N_4 | | AE9 | | | |
| 4 | IO_L44P_4 | | AE10 | | | |
| 4 | IO_L45N_4 | | AH9 | | | |
| 4 | IO_L45P_4/VREF_4 | | AJ9 | | | |
| 4 | IO_L46N_4 | | AC13 | NC | | |
| 4 | IO_L46P_4 | | AD13 | NC | | |
| 4 | IO_L47N_4 | | AE11 | NC | | |
| 4 | IO_L47P_4 | | AE12 | NC | | |
| 4 | IO_L48N_4 | | AH10 | NC | | |
| 4 | IO_L48P_4 | | AH11 | NC | | |
| 4 | IO_L49N_4 | | AB14 | NC | | |
| 4 | IO_L49P_4 | | AC14 | NC | | |
| 4 | IO_L50_4/No_Pair | | AF11 | NC | | |
| 4 | IO_L53_4/No_Pair | | AG11 | NC | | |
| 4 | IO_L54N_4 | | AJ10 | NC | | |
| 4 | IO_L54P_4 | | AK10 | NC | | |
| 4 | IO_L56N_4 | | AF12 | NC | | |
| 4 | IO_L56P_4 | | AF13 | NC | | |
| 4 | IO_L57N_4 | | AG13 | NC | | |

*Table 9:* **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

| Bank | Pin Description | | Pin Number | No Connects | | |
|---|---|---|---|---|---|---|
| | Virtex-II Pro devices | XC2VPX20 (if Different) | | XC2VP7 | XC2VP20, XC2VPX20 | XC2VP30 |
| 4 | IO_L57P_4/VREF_4 | | AH13 | NC | | |
| 4 | IO_L67N_4 | | AB15 | | | |
| 4 | IO_L67P_4 | | AC15 | | | |
| 4 | IO_L68N_4 | | AD14 | | | |
| 4 | IO_L68P_4 | | AE14 | | | |
| 4 | IO_L69N_4 | | AF14 | | | |
| 4 | IO_L69P_4/VREF_4 | | AG14 | | | |
| 4 | IO_L73N_4 | | AD15 | | | |
| 4 | IO_L73P_4 | | AE15 | | | |
| 4 | IO_L74N_4/GCLK3S | | AF15 | | | |
| 4 | IO_L74P_4/GCLK2P | | AG15 | | | |
| 4 | IO_L75N_4/GCLK1S | | AH15 | | | |
| 4 | IO_L75P_4/GCLK0P | | AJ15 | | | |
| | | | | | | |
| 5 | IO_L75N_5/GCLK7S | BREFCLKN | AJ16 | | | |
| 5 | IO_L75P_5/GCLK6P | BREFCLKP | AH16 | | | |
| 5 | IO_L74N_5/GCLK5S | | AG16 | | | |
| 5 | IO_L74P_5/GCLK4P | | AF16 | | | |
| 5 | IO_L73N_5 | | AE16 | | | |
| 5 | IO_L73P_5 | | AD16 | | | |
| 5 | IO_L69N_5/VREF_5 | | AG17 | | | |
| 5 | IO_L69P_5 | | AF17 | | | |
| 5 | IO_L68N_5 | | AE17 | | | |
| 5 | IO_L68P_5 | | AD17 | | | |
| 5 | IO_L67N_5 | | AC16 | | | |
| 5 | IO_L67P_5 | | AB16 | | | |
| 5 | IO_L57N_5/VREF_5 | | AH18 | NC | | |
| 5 | IO_L57P_5 | | AG18 | NC | | |
| 5 | IO_L56N_5 | | AF18 | NC | | |
| 5 | IO_L56P_5 | | AF19 | NC | | |
| 5 | IO_L54N_5 | | AK21 | NC | | |
| 5 | IO_L54P_5 | | AJ21 | NC | | |
| 5 | IO_L53_5/No_Pair | | AG20 | NC | | |
| 5 | IO_L50_5/No_Pair | | AF20 | NC | | |
| 5 | IO_L49N_5 | | AC17 | NC | | |
| 5 | IO_L49P_5 | | AB17 | NC | | |

*Table 9:* **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

| Bank | Pin Description | | Pin Number | No Connects | | |
|---|---|---|---|---|---|---|
| | Virtex-II Pro devices | XC2VPX20 (if Different) | | XC2VP7 | XC2VP20, XC2VPX20 | XC2VP30 |
| 6 | IO_L86P_6 | | T23 | | | |
| 6 | IO_L86N_6 | | T24 | | | |
| 6 | IO_L87P_6 | | U28 | | | |
| 6 | IO_L87N_6/VREF_6 | | U29 | | | |
| 6 | IO_L88P_6 | | T27 | | | |
| 6 | IO_L88N_6 | | T28 | | | |
| 6 | IO_L89P_6 | | T25 | | | |
| 6 | IO_L89N_6 | | T26 | | | |
| 6 | IO_L90P_6 | | V30 | | | |
| 6 | IO_L90N_6 | | U30 | | | |
| | | | | | | |
| 7 | IO_L90P_7 | | R28 | | | |
| 7 | IO_L90N_7 | | R27 | | | |
| 7 | IO_L89P_7 | | R26 | | | |
| 7 | IO_L89N_7 | | R25 | | | |
| 7 | IO_L88P_7 | | T29 | | | |
| 7 | IO_L88N_7/VREF_7 | | R29 | | | |
| 7 | IO_L87P_7 | | P27 | | | |
| 7 | IO_L87N_7 | | P26 | | | |
| 7 | IO_L86P_7 | | R24 | | | |
| 7 | IO_L86N_7 | | R23 | | | |
| 7 | IO_L85P_7 | | P29 | | | |
| 7 | IO_L85N_7 | | P28 | | | |
| 7 | IO_L60P_7 | | N28 | | | |
| 7 | IO_L60N_7 | | N27 | | | |
| 7 | IO_L59P_7 | | P24 | | | |
| 7 | IO_L59N_7 | | P23 | | | |
| 7 | IO_L58P_7 | | P30 | | | |
| 7 | IO_L58N_7/VREF_7 | | N30 | | | |
| 7 | IO_L57P_7 | | M28 | | | |
| 7 | IO_L57N_7 | | M27 | | | |
| 7 | IO_L56P_7 | | R22 | | | |
| 7 | IO_L56N_7 | | P22 | | | |
| 7 | IO_L55P_7 | | N29 | | | |
| 7 | IO_L55N_7 | | M29 | | | |
| 7 | IO_L54P_7 | | L27 | | | |

*Table 9:* **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

| Bank | Pin Description | | Pin Number | No Connects | | |
|---|---|---|---|---|---|---|
| | Virtex-II Pro devices | XC2VPX20 (if Different) | | XC2VP7 | XC2VP20, XC2VPX20 | XC2VP30 |
| N/A | VCCINT | | Y13 | | | |
| N/A | VCCINT | | Y12 | | | |
| N/A | VCCINT | | W20 | | | |
| N/A | VCCINT | | W11 | | | |
| N/A | VCCINT | | V20 | | | |
| N/A | VCCINT | | V11 | | | |
| N/A | VCCINT | | U20 | | | |
| N/A | VCCINT | | U11 | | | |
| N/A | VCCINT | | T20 | | | |
| N/A | VCCINT | | T11 | | | |
| N/A | VCCINT | | R20 | | | |
| N/A | VCCINT | | R11 | | | |
| N/A | VCCINT | | P20 | | | |
| N/A | VCCINT | | P11 | | | |
| N/A | VCCINT | | N20 | | | |
| N/A | VCCINT | | N11 | | | |
| N/A | VCCINT | | M20 | | | |
| N/A | VCCINT | | M11 | | | |
| N/A | VCCINT | | L19 | | | |
| N/A | VCCINT | | L18 | | | |
| N/A | VCCINT | | L17 | | | |
| N/A | VCCINT | | L16 | | | |
| N/A | VCCINT | | L15 | | | |
| N/A | VCCINT | | L14 | | | |
| N/A | VCCINT | | L13 | | | |
| N/A | VCCINT | | L12 | | | |
| N/A | GND | | AK22 | | | |
| N/A | GND | | AK9 | | | |
| N/A | GND | | AJ29 | | | |
| N/A | GND | | AJ2 | | | |
| N/A | GND | | AH28 | | | |
| N/A | GND | | AH17 | | | |
| N/A | GND | | AH14 | | | |
| N/A | GND | | AH3 | | | |
| N/A | GND | | AG27 | | | |
| N/A | GND | | AG22 | | | |

*Table 10:* **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | | | |
|---|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 |
| 4 | VCCO_4 | AD15 | | | | |
| 4 | VCCO_4 | AJ10 | | | | |
| 4 | VCCO_4 | AK15 | | | | |
| 4 | VCCO_4 | AM6 | | | | |
| 5 | VCCO_5 | AC18 | | | | |
| 5 | VCCO_5 | AC19 | | | | |
| 5 | VCCO_5 | AC20 | | | | |
| 5 | VCCO_5 | AC21 | | | | |
| 5 | VCCO_5 | AC22 | | | | |
| 5 | VCCO_5 | AD20 | | | | |
| 5 | VCCO_5 | AD21 | | | | |
| 5 | VCCO_5 | AD22 | | | | |
| 5 | VCCO_5 | AD23 | | | | |
| 5 | VCCO_5 | AJ25 | | | | |
| 5 | VCCO_5 | AK20 | | | | |
| 5 | VCCO_5 | AM29 | | | | |
| 6 | VCCO_6 | V23 | | | | |
| 6 | VCCO_6 | W23 | | | | |
| 6 | VCCO_6 | Y23 | | | | |
| 6 | VCCO_6 | Y24 | | | | |
| 6 | VCCO_6 | Y30 | | | | |
| 6 | VCCO_6 | AA23 | | | | |
| 6 | VCCO_6 | AA24 | | | | |
| 6 | VCCO_6 | AB23 | | | | |
| 6 | VCCO_6 | AB24 | | | | |
| 6 | VCCO_6 | AC24 | | | | |
| 6 | VCCO_6 | AE29 | | | | |
| 6 | VCCO_6 | AJ32 | | | | |
| 7 | VCCO_7 | F32 | | | | |
| 7 | VCCO_7 | K29 | | | | |
| 7 | VCCO_7 | M24 | | | | |
| 7 | VCCO_7 | N23 | | | | |
| 7 | VCCO_7 | N24 | | | | |
| 7 | VCCO_7 | P23 | | | | |
| 7 | VCCO_7 | P24 | | | | |
| 7 | VCCO_7 | R23 | | | | |
| 7 | VCCO_7 | R24 | | | | |
| 7 | VCCO_7 | R30 | | | | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| 0 | IO_L43N_0 | B22 | | |
| 0 | IO_L43P_0 | C22 | | |
| 0 | IO_L44N_0 | K21 | | |
| 0 | IO_L44P_0 | L21 | | |
| 0 | IO_L45N_0 | G21 | | |
| 0 | IO_L45P_0/VREF_0 | H21 | | |
| 0 | IO_L46N_0 | E21 | | |
| 0 | IO_L46P_0 | F21 | | |
| 0 | IO_L47N_0 | K20 | | |
| 0 | IO_L47P_0 | L20 | | |
| 0 | IO_L48N_0 | C21 | | |
| 0 | IO_L48P_0 | D21 | | |
| 0 | IO_L49N_0 | A21 | | |
| 0 | IO_L49P_0 | B21 | | |
| 0 | IO_L50_0/No_Pair | G20 | | |
| 0 | IO_L53_0/No_Pair | H19 | | |
| 0 | IO_L54N_0 | E20 | | |
| 0 | IO_L54P_0 | F20 | | |
| 0 | IO_L55N_0 | C20 | | |
| 0 | IO_L55P_0 | D19 | | |
| 0 | IO_L56N_0 | K19 | | |
| 0 | IO_L56P_0 | L19 | | |
| 0 | IO_L57N_0 | A20 | | |
| 0 | IO_L57P_0/VREF_0 | B20 | | |
| 0 | IO_L66N_0 | F19 | NC | |
| 0 | IO_L66P_0/VREF_0 | G19 | NC | |
| 0 | IO_L67N_0 | B19 | | |
| 0 | IO_L67P_0 | C19 | | |
| 0 | IO_L68N_0 | H18 | | |
| 0 | IO_L68P_0 | J18 | | |
| 0 | IO_L69N_0 | F18 | | |
| 0 | IO_L69P_0/VREF_0 | G18 | | |
| 0 | IO_L73N_0 | D18 | | |
| 0 | IO_L73P_0 | E18 | | |
| 0 | IO_L74N_0/GCLK7P | K18 | | |
| 0 | IO_L74P_0/GCLK6S | L18 | | |
| 0 | IO_L75N_0/GCLK5P | B18 | | |
| 0 | IO_L75P_0/GCLK4S | C18 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 3 | IO_L90P_3 | AA8 | | |
| 3 | IO_L89N_3 | Y11 | | |
| 3 | IO_L89P_3 | Y12 | | |
| 3 | IO_L88N_3 | AA5 | | |
| 3 | IO_L88P_3 | AA6 | | |
| 3 | IO_L87N_3/VREF_3 | AA3 | | |
| 3 | IO_L87P_3 | AA4 | | |
| 3 | IO_L86N_3 | Y13 | | |
| 3 | IO_L86P_3 | AA13 | | |
| 3 | IO_L85N_3 | AB7 | | |
| 3 | IO_L85P_3 | AB8 | | |
| 3 | IO_L60N_3 | AB5 | | |
| 3 | IO_L60P_3 | AB6 | | |
| 3 | IO_L59N_3 | AA9 | | |
| 3 | IO_L59P_3 | AA10 | | |
| 3 | IO_L58N_3 | AB3 | | |
| 3 | IO_L58P_3 | AB4 | | |
| 3 | IO_L57N_3/VREF_3 | AB1 | | |
| 3 | IO_L57P_3 | AB2 | | |
| 3 | IO_L56N_3 | AA11 | | |
| 3 | IO_L56P_3 | AA12 | | |
| 3 | IO_L55N_3 | AC5 | | |
| 3 | IO_L55P_3 | AC6 | | |
| 3 | IO_L54N_3 | AC1 | | |
| 3 | IO_L54P_3 | AC2 | | |
| 3 | IO_L53N_3 | AB9 | | |
| 3 | IO_L53P_3 | AB10 | | |
| 3 | IO_L52N_3 | AC8 | | |
| 3 | IO_L52P_3 | AD8 | | |
| 3 | IO_L51N_3/VREF_3 | AC4 | | |
| 3 | IO_L51P_3 | AD4 | | |
| 3 | IO_L50N_3 | AB11 | | |
| 3 | IO_L50P_3 | AB12 | | |
| 3 | IO_L49N_3 | AD6 | | |
| 3 | IO_L49P_3 | AD7 | | |
| 3 | IO_L48N_3 | AD2 | | |
| 3 | IO_L48P_3 | AD3 | | |
| 3 | IO_L47N_3 | AC9 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 4 | IO_L09N_4 | | AR11 | | |
| 4 | IO_L09P_4/VREF_4 | | AP11 | | |
| 4 | IO_L19N_4 | | AV11 | | |
| 4 | IO_L19P_4 | | AU11 | | |
| 4 | IO_L20N_4 | | AY10 | | |
| 4 | IO_L20P_4 | | AY11 | | |
| 4 | IO_L21N_4 | | AN12 | | |
| 4 | IO_L21P_4 | | AM12 | | |
| 4 | IO_L25N_4 | | AR12 | | |
| 4 | IO_L25P_4 | | AP12 | | |
| 4 | IO_L26N_4 | | AT12 | | |
| 4 | IO_L26P_4 | | AU12 | | |
| 4 | IO_L27N_4 | | AW12 | | |
| 4 | IO_L27P_4/VREF_4 | | AV12 | | |
| 4 | IO_L28N_4 | | AM13 | | |
| 4 | IO_L28P_4 | | AL13 | | |
| 4 | IO_L29N_4 | | AP13 | | |
| 4 | IO_L29P_4 | | AN13 | | |
| 4 | IO_L30N_4 | | AT13 | | |
| 4 | IO_L30P_4 | | AR13 | | |
| 4 | IO_L34N_4 | | AV13 | | |
| 4 | IO_L34P_4 | | AU13 | | |
| 4 | IO_L35N_4 | | AW13 | | |
| 4 | IO_L35P_4 | | AY13 | | |
| 4 | IO_L36N_4 | | AL15 | | |
| 4 | IO_L36P_4/VREF_4 | | AL14 | | |
| 4 | IO_L78N_4 | | AN14 | NC | |
| 4 | IO_L78P_4 | | AM14 | NC | |
| 4 | IO_L83_4/No_Pair | | AR14 | NC | |
| 4 | IO_L84N_4 | | AU14 | NC | |
| 4 | IO_L84P_4 | | AT14 | NC | |
| 4 | IO_L85N_4 | | AW14 | NC | |
| 4 | IO_L85P_4 | | AV14 | NC | |
| 4 | IO_L86N_4 | | AM15 | NC | |
| 4 | IO_L86P_4 | | AN15 | NC | |
| 4 | IO_L87N_4 | | AR15 | NC | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 6 | IO_L52N_6 | | AE42 | | |
| 6 | IO_L53P_6 | | AE32 | | |
| 6 | IO_L53N_6 | | AE33 | | |
| 6 | IO_L54P_6 | | AD35 | | |
| 6 | IO_L54N_6 | | AD36 | | |
| 6 | IO_L55P_6 | | AD37 | | |
| 6 | IO_L55N_6 | | AD38 | | |
| 6 | IO_L56P_6 | | AD31 | | |
| 6 | IO_L56N_6 | | AD32 | | |
| 6 | IO_L57P_6 | | AD39 | | |
| 6 | IO_L57N_6/VREF_6 | | AD40 | | |
| 6 | IO_L58P_6 | | AD41 | | |
| 6 | IO_L58N_6 | | AD42 | | |
| 6 | IO_L59P_6 | | AD33 | | |
| 6 | IO_L59N_6 | | AD34 | | |
| 6 | IO_L60P_6 | | AC33 | | |
| 6 | IO_L60N_6 | | AC34 | | |
| 6 | IO_L85P_6 | | AC36 | | |
| 6 | IO_L85N_6 | | AC37 | | |
| 6 | IO_L86P_6 | | AC31 | | |
| 6 | IO_L86N_6 | | AC32 | | |
| 6 | IO_L87P_6 | | AC39 | | |
| 6 | IO_L87N_6/VREF_6 | | AC40 | | |
| 6 | IO_L88P_6 | | AB33 | | |
| 6 | IO_L88N_6 | | AB34 | | |
| 6 | IO_L89P_6 | | AB36 | | |
| 6 | IO_L89N_6 | | AB37 | | |
| 6 | IO_L90P_6 | | AB39 | | |
| 6 | IO_L90N_6 | | AB40 | | |
| | | | | | |
| 7 | IO_L90P_7 | | AA39 | | |
| 7 | IO_L90N_7 | | AA40 | | |
| 7 | IO_L89P_7 | | AB31 | | |
| 7 | IO_L89N_7 | | AA31 | | |
| 7 | IO_L88P_7 | | AA36 | | |
| 7 | IO_L88N_7/VREF_7 | | AA37 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 3 | VCCO_3 | | AD14 | | |
| 3 | VCCO_3 | | AC15 | | |
| 3 | VCCO_3 | | AC14 | | |
| 3 | VCCO_3 | | AC8 | | |
| 3 | VCCO_3 | | AC5 | | |
| 3 | VCCO_3 | | AB15 | | |
| 3 | VCCO_3 | | AB14 | | |
| 4 | VCCO_4 | | AW18 | | |
| 4 | VCCO_4 | | AT20 | | |
| 4 | VCCO_4 | | AT15 | | |
| 4 | VCCO_4 | | AT11 | | |
| 4 | VCCO_4 | | AP18 | | |
| 4 | VCCO_4 | | AP14 | | |
| 4 | VCCO_4 | | AJ21 | | |
| 4 | VCCO_4 | | AJ20 | | |
| 4 | VCCO_4 | | AJ19 | | |
| 4 | VCCO_4 | | AJ18 | | |
| 4 | VCCO_4 | | AJ17 | | |
| 4 | VCCO_4 | | AH21 | | |
| 4 | VCCO_4 | | AH20 | | |
| 4 | VCCO_4 | | AH19 | | |
| 4 | VCCO_4 | | AH18 | | |
| 5 | VCCO_5 | | AW25 | | |
| 5 | VCCO_5 | | AT32 | | |
| 5 | VCCO_5 | | AT28 | | |
| 5 | VCCO_5 | | AT23 | | |
| 5 | VCCO_5 | | AP29 | | |
| 5 | VCCO_5 | | AP25 | | |
| 5 | VCCO_5 | | AJ26 | | |
| 5 | VCCO_5 | | AJ25 | | |
| 5 | VCCO_5 | | AJ24 | | |
| 5 | VCCO_5 | | AJ23 | | |
| 5 | VCCO_5 | | AJ22 | | |
| 5 | VCCO_5 | | AH25 | | |
| 5 | VCCO_5 | | AH24 | | |
| 5 | VCCO_5 | | AH23 | | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 7 | IO_L87P_7 | AA37 | |
| 7 | IO_L87N_7 | AA38 | |
| 7 | IO_L86P_7 | AA33 | |
| 7 | IO_L86N_7 | AA34 | |
| 7 | IO_L85P_7 | Y40 | |
| 7 | IO_L85N_7 | Y41 | |
| 7 | IO_L60P_7 | W41 | |
| 7 | IO_L60N_7 | W42 | |
| 7 | IO_L59P_7 | AA31 | |
| 7 | IO_L59N_7 | AA32 | |
| 7 | IO_L58P_7 | V40 | |
| 7 | IO_L58N_7/VREF_7 | W40 | |
| 7 | IO_L57P_7 | W37 | |
| 7 | IO_L57N_7 | W38 | |
| 7 | IO_L56P_7 | Y36 | |
| 7 | IO_L56N_7 | Y37 | |
| 7 | IO_L55P_7 | V41 | |
| 7 | IO_L55N_7 | V42 | |
| 7 | IO_L54P_7 | V38 | |
| 7 | IO_L54N_7 | V39 | |
| 7 | IO_L53P_7 | Y31 | |
| 7 | IO_L53N_7 | Y32 | |
| 7 | IO_L52P_7 | U40 | |
| 7 | IO_L52N_7/VREF_7 | U41 | |
| 7 | IO_L51P_7 | T40 | |
| 7 | IO_L51N_7 | U39 | |
| 7 | IO_L50P_7 | Y35 | |
| 7 | IO_L50N_7 | W36 | |
| 7 | IO_L49P_7 | T37 | |
| 7 | IO_L49N_7 | U37 | |
| 7 | IO_L48P_7 | T41 | |
| 7 | IO_L48N_7 | T42 | |
| 7 | IO_L47P_7 | Y33 | |
| 7 | IO_L47N_7 | W34 | |
| 7 | IO_L46P_7 | T38 | |
| 7 | IO_L46N_7/VREF_7 | T39 | |
| 7 | IO_L45P_7 | R36 | |