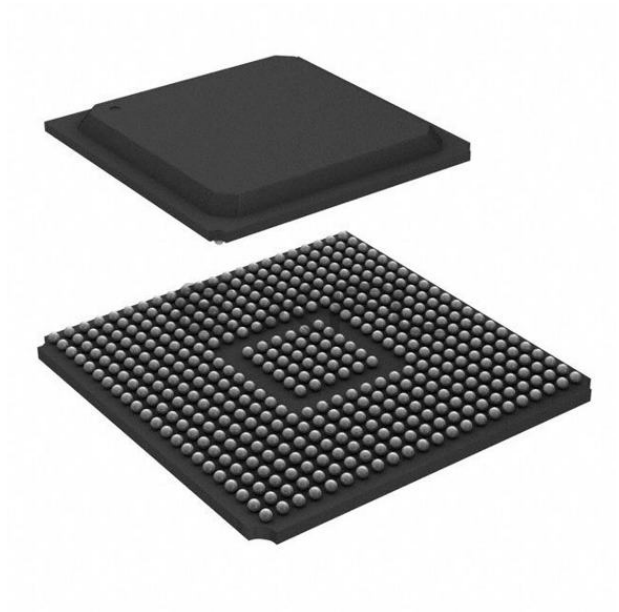
AMD Xilinx - XC2VP2-6FG456I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	352
Number of Logic Elements/Cells	3168
Total RAM Bits	221184
Number of I/O	156
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp2-6fg456i

Notice of Disclaimer

Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)

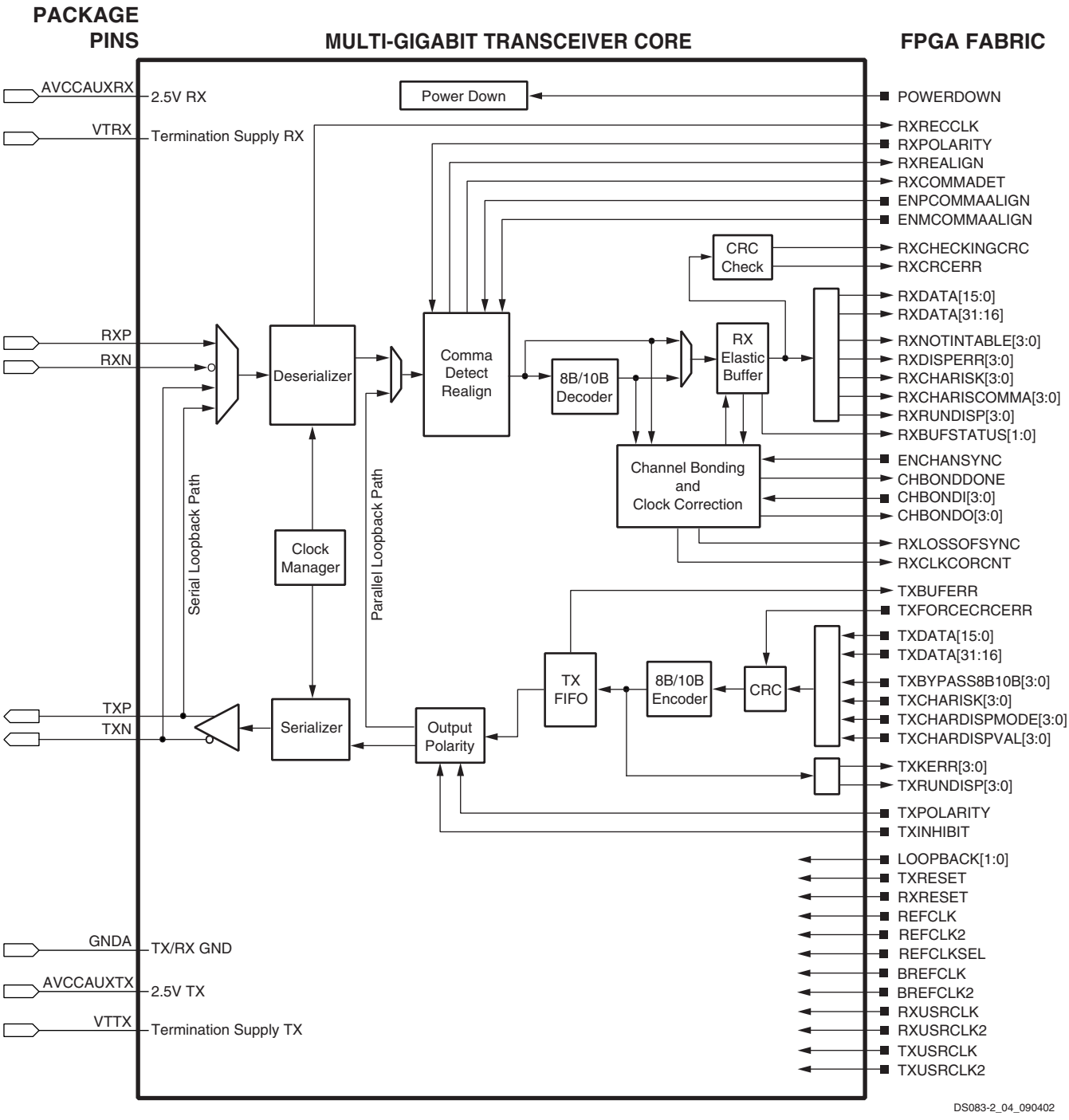

Figure 10: **RocketIO Transceiver Block Diagram**

Output Swing and Pre-emphasis

The output swing and pre-emphasis levels of the RocketIO MGTs are fully programmable. Each is controlled via attributes at configuration, but can be modified via partial reconfiguration.

The programmable output swing control can adjust the differential output level between 400 mV and 800 mV in four increments of 100 mV.

With pre-emphasis, the differential voltage swing is boosted to create a stronger rising waveform. This method compensates for high-frequency loss in the transmission media that would otherwise limit the magnitude of this waveform. Lossy transmission lines cause the dissipation of electrical energy. This pre-emphasis technique extends the distance that signals can be driven down lossy line media and increases the signal-to-noise ratio at the receiver.

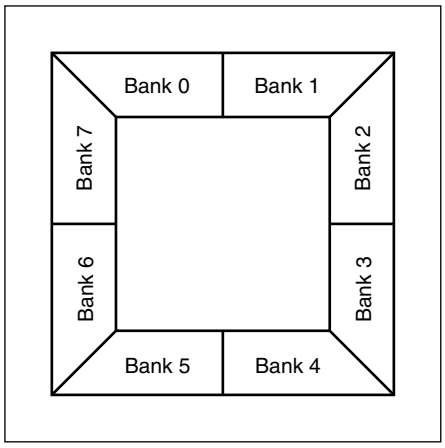

Figure 24: **I/O Banks: Wire-Bond Packages (FG) Top View**

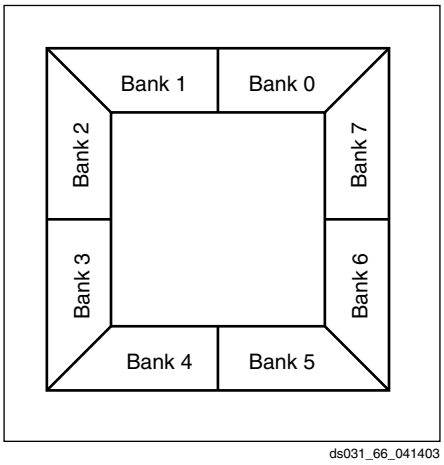

Figure 25: **I/O Banks: Flip-Chip Packages (FF) Top View**

Some input standards require a user-supplied threshold voltage (V_{REF}), and certain user-I/O pins are automatically configured as V_{REF} inputs. Approximately one in six of the I/O pins in the bank assume this role.

V_{REF} pins within a bank are interconnected internally, thus only one V_{REF} voltage can be used within each bank. However, for correct operation, all V_{REF} pins in the bank must be connected to the external reference voltage source.

The V_{CCO} and the V_{REF} pins for each bank appear in the device pinout tables. Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage and not used for I/O. In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to V_{CCO} to permit migration to a larger device.

Rules for Combining I/O Standards in the Same Bank

The following rules must be obeyed to combine different input, output, and bi-directional standards in the same bank:

1. **Combining output standards only.** Output standards with the same output V_{CCO} requirement can be combined in the same bank.
   Compatible example:
   SSTL2_I and LVDS_25 outputs
   Incompatible example:
   SSTL2_I (output V_{CCO} = 2.5V) and
   LVCMOS33 (output V_{CCO} = 3.3V) outputs
2. **Combining input standards only.** Input standards with the same input V_{CCO} and input V_{REF} requirements can be combined in the same bank.
   Compatible example:
   LVCMOS15 and HSTL_IV inputs
   Incompatible example:
   LVCMOS15 (input V_{CCO} = 1.5V) and
   LVCMOS18 (input V_{CCO} = 1.8V) inputs
   Incompatible example:
   HSTL_I_DCI_18 (V_{REF} = 0.9V) and
   HSTL_IV_DCI_18 (V_{REF} = 1.1V) inputs
3. **Combining input standards and output standards.** Input standards and output standards with the same input V_{CCO} and output V_{CCO} requirement can be combined in the same bank.
   Compatible example:
   LVDS_25 output and HSTL_I input
   Incompatible example:
   LVDS_25 output (output V_{CCO} = 2.5V) and
   HSTL_I_DCI_18 input (input V_{CCO} = 1.8V)
4. **Combining bi-directional standards with input or output standards.** When combining bi-directional I/O with other standards, make sure the bi-directional standard can meet rules 1 through 3 above.
5. **Additional rules for combining DCI I/O standards.**
   a. No more than one Single Termination type (input or output) is allowed in the same bank.
      Incompatible example:
      HSTL_IV_DCI input and HSTL_III_DCI input
   b. No more than one Split Termination type (input or output) is allowed in the same bank.
      Incompatible example:
      HSTL_I_DCI input and HSTL_II_DCI input

The implementation tools will enforce the above design rules.

Table 12, page 30, summarizes all standards and voltage supplies.

Figure 30 provides examples illustrating the use of the LVDS_25_DCI and LVDSEXT_25_DCI I/O standards. For a complete list, see the ***Virtex-II Pro Platform FPGA User Guide***.

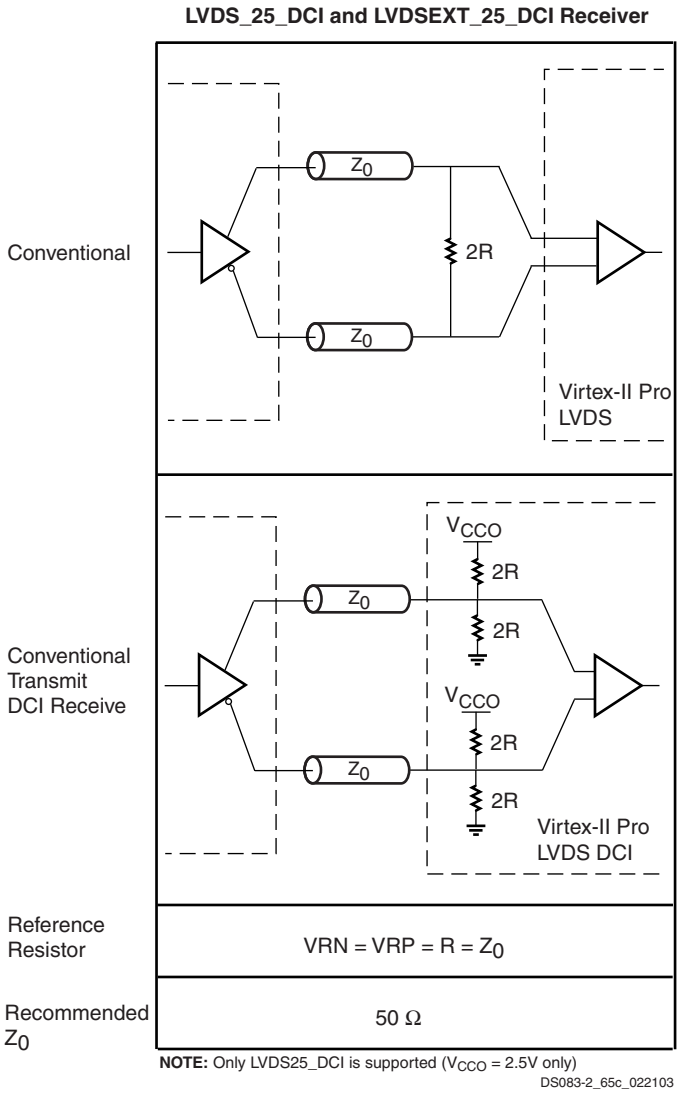

Figure 30: **LVDS DCI Usage Examples**

On-Chip Differential Termination

Virtex-II Pro provides a true 100Ω differential termination (DT) across the input differential receiver terminals. The LVDS_25_DT, LVDSEXT_25_DT, LDT_25_DT, and ULVDS_25_DT standards support on-chip differential termination.

The on-chip input differential termination in Virtex-II Pro provides major advantages over the external resistor or the DCI termination solution:

- Eliminates the stub at the receiver completely and therefore greatly improve signal integrity
- Consumes less power than DCI termination
- Supports LDT (not supported by DCI termination)
- Frees up VRP/VRN pins

Figure 31 provides examples illustrating the use of the LVDS_25_DT, LVDSEXT_25_DT, LDT_25_DT, and ULVDS_25_DT I/O standards. For further details, refer to **Solution Record 17244**. Also see the ***Virtex-II Pro Platform FPGA User Guide*** for more design information.

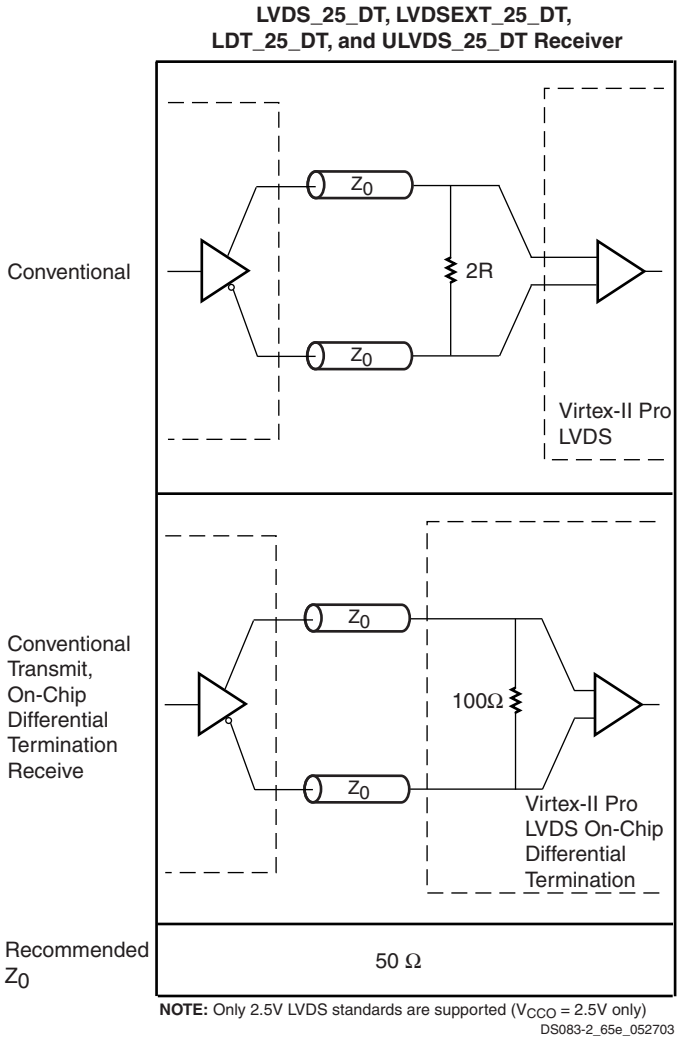

Figure 31: **LVDS Differential Termination Usage Examples**

Date	Version	Revision
03/24/03	2.5.1	• Table 10: Corrected I/O standard names SSTL18_I and SSTL18_II to SSTL18_I_DCI and SSTL18_II_DCI respectively. • Figure 61, text below: Corrected wording of criteria for clock switching.
05/27/03	2.6	• Removed Compatible Output Standards and Compatible Input Standards tables. • Added new Table 12, Summary of Voltage Supply Requirements for All Input and Output Standards. This table replaces deleted I/O standards tables. • Corrected sentence in section Input/Output Individual Options, page 27, to read “The optional weak-keeper circuit is connected to each *user I/O pad*.” • Added section Rules for Combining I/O Standards in the Same Bank, page 29.
06/02/03	2.7	• Added four Differential Termination I/O standards to Table 9 and Table 12. • Added section On-Chip Differential Termination and Figure 31, page 34.
08/25/03	2.7.1	• Added footnote referring to XAPP659 to 3.3V I/O callouts in Table 8 and Table 12.
09/10/03	2.8	• Section Configuration, page 56: Added text indicating that the mode pins M0-M2 must be held to a constant DC level during and after configuration.
10/14/03	2.9	• Deleted section Functional Description: RocketIO Multi-Gigabit Transceiver (MGT), page 10. Added section Local Clocking, page 51. • Sections Slave-Serial Mode and Master-Serial Mode, page 56: Changed "rising" to "falling" edge with respect to DOUT. • Table 8, page 24 and Table 10, page 25: Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Section BUFGMUX, page 50: Corrected the definition of the "presently selected clock" to be I0 or I1. Corrected signal names in Figure 61 and associated text from CLK0 and CLK1 to I0 and I1.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
04/22/04	3.2	• Section Clock De-skew, page 52: Removed reference to CLK2X as an option for DCM clock feedback.
06/30/04	4.0	Merged in DS110-2 (Module 2 of Virtex-II Pro X data sheet). Separate RocketIO and RocketIO X sections created.
11/17/04	4.1	• Figure 11, page 12: Corrected figure by removing coupling capacitors from input. • Section Rules for Combining I/O Standards in the Same Bank, page 29: Corrected I/O standard in the first example from LVDS_25_DCI to LVDS_25.
03/01/05	4.2	• Reassigned heading hierarchies for better agreement with content. • Table 7: Corrected VCCAUXTX and VCCAUXRX to AVCCAUXTX and AVCCAUXRX respectively. • Table 9: Corrected V_{OD} (output voltage) range for LVDSEXT_25. • Table 25: Corrected SelectRAM+ memory available for XC2VPX70 device. • Table 33: Updated configuration default bitstream lengths.
06/20/05	4.3	*No changes in Module 2 for this revision.*
09/15/05	4.4	• Table 1: Deleted SONET OC-192 protocol. • Table 3: Deleted RocketIO X primitives for SONET OC-192, 10 Gbit Ethernet, and Xilinx 10G (Aurora) protocols. • Changed all instances of 10.3125 Gb/s to 6.25 Gb/s. • Table 7: Changed RocketIO X VCCAUXRX from 1.5V globally to 1.5V for 8B/10B encoding, 1.8V for all other encoding protocols.

Virtex-II Pro Switching Characteristics

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Note that Virtex-II Pro Performance Characteristics are subject to these guidelines, as well. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 15 correlates the current status of each Virtex-II Pro device with a corresponding speed file designation.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Table 15: **Virtex-II Pro Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC2VP2			-7, -6, -5
XC2VP4			-7, -6, -5
XC2VP7			-7, -6, -5
XC2VP20			-7, -6, -5
XC2VPX20		-6, -5	
XC2VP30			-7, -6, -5
XC2VP40			-7, -6, -5
XC2VP50			-7, -6, -5
XC2VP70			-7, -6, -5
XC2VPX70		-6, -5	
XC2VP100			-6, -5

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II Pro devices.

PowerPC Switching Characteristics

Table 16: **Processor Clocks Absolute AC Characteristics**

Description	Speed Grade						Units
	-7		-6		-5		
	Min	Max	Min	Max	Min	Max	
CPMC405CLOCK frequency	0	400(1)	0	350(1)	0	300	MHz
JTAGC405TCK frequency(2)	0	200	0	175	0	150	MHz
PLBCLK(3)	0	400	0	350	0	300	MHz
BRAMDSOCMCLK(3)	0	400	0	350	0	300	MHz
BRAMISOCMCLK(3)	0	400	0	350	0	300	MHz

Notes:

1. **IMPORTANT!** When CPMC405CLOCK runs at speeds greater than 350 MHz in -7 Commercial grade dual-processor devices, or greater than 300 MHz in -6 Industrial grade dual-processor devices, users must implement the technology presented in **XAPP755**, "PowerPC 405 Clock Macro for -7(C) and -6(I) Speed Grade Dual-Processor Devices." Refer to Table 1, Module 1 to identify dual-processor devices.
2. The theoretical maximum frequency of this clock is one-half the CPMC405CLOCK. However, the achievable maximum is dependent on the system, and will be much less.
3. The theoretical maximum frequency of these clocks is equal to the CPMC405CLOCK. However, the achievable maximum is dependent on the system. Please see ***PowerPC 405 Processor Block Reference Guide*** and **XAPP640** for more information.

Table 17: **Processor Block Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (CPMC405CLOCK)					
Device Control Register Bus control inputs	$T_{PCCK\_}DCR/T_{PCKC\_}DCR$	0.38/–0.18	0.44/–0.20	0.48/–0.23	ns, min
Device Control Register Bus data inputs	$T_{PDCK\_}DCR/T_{PCKD\_}DCR$	0.65/–0.01	0.75/–0.01	0.82/–0.02	ns, min
Clock and Power Management control inputs	$T_{PCCK\_}CPM/T_{PCKC\_}CPM$	0.16/ 0.03	0.19/ 0.03	0.20/ 0.03	ns, min
Reset control inputs	$T_{PCCK\_}RST/T_{PCKC\_}RST$	0.16/ 0.03	0.19/ 0.03	0.20/ 0.03	ns, min
Debug control inputs	$T_{PCCK\_}DBG/T_{PCKC\_}DBG$	0.27/ 0.30	0.31/ 0.35	0.34/ 0.38	ns, min
Trace control inputs	$T_{PCCK\_}TRC/T_{PCKC\_}TRC$	1.37/–0.41	1.57/–0.48	1.73/–0.52	ns, min
External Interrupt Controller control inputs	$T_{PCCK\_}EIC/T_{PCKC\_}EIC$	0.57/–0.22	0.66/–0.25	0.72/–0.27	ns, min
Clock to Out					
Device Control Register Bus control outputs	$T_{PCKCO\_}DCR$	1.32	1.52	1.67	ns, max
Device Control Register Bus address outputs	$T_{PCKAO\_}DCR$	1.72	1.98	2.17	ns, max
Device Control Register Bus data outputs	$T_{PCKDO\_}DCR$	1.76	2.02	2.22	ns, max
Clock and Power Management control outputs	$T_{PCKCO\_}CPM$	1.26	1.45	1.59	ns, max
Reset control outputs	$T_{PCKCO\_}RST$	1.32	1.51	1.66	ns, max
Debug control outputs	$T_{PCKCO\_}DBG$	1.94	2.22	2.44	ns, max
Trace control outputs	$T_{PCKCO\_}TRC$	1.35	1.56	1.71	ns, max
Clock					
CPMC405CLOCK minimum pulse width, high	T_{CPWH}	1.25	1.42	1.66	ns, min
CPMC405CLOCK minimum pulse width, low	T_{CPWL}	1.25	1.42	1.66	ns, min

Table 18: **Processor Block PLB Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (PLBCLK)					
Processor Local Bus(ICU/DCU) control inputs	$T_{PCCK\_}PLB/T_{PCKC\_}PLB$	0.98/ 0.18	1.12/ 0.21	1.23/ 0.23	ns, min
Processor Local Bus (ICU/DCU) data inputs	$T_{PDCK\_}PLB/T_{PCKD\_}PLB$	0.62/ 0.16	0.71/ 0.18	0.78/ 0.20	ns, min
Clock to Out					
Processor Local Bus(ICU/DCU) control outputs	$T_{PCKCO\_}PLB$	1.34	1.54	1.69	ns, max
Processor Local Bus(ICU/DCU) address bus outputs	$T_{PCKAO\_}PLB$	1.16	1.34	1.47	ns, max
Processor Local Bus(ICU/DCU) data bus outputs	$T_{PCKDO\_}PLB$	1.44	1.65	1.81	ns, max

Date	Version	Revision
12/05/03 (cont'd)	3.0 (cont'd)	• Non-speedsfile parameter values added or updated: • Table 3: I_{BATT}. • Table 4: For XC2VP100, I_{CCINTQ}, I_{CCOQ}, and I_{CCAUXQ}. • Table 5: For XC2VP100, $I_{CCINTMIN}$. • Table 17: T_{CPWL} and T_{CPWH}. • Table 25: Added explanatory footnote to T_{RXLAT} (MGT receiver latency) max value. • Table 57: Added Footnote (3) regarding use of CLKIN_DIVIDE_BY_2 attribute.
02/19/04	3.1	• Updated time and frequency parameters as per speedsfile **v1.85**. • Table 2, Recommended Operating Conditions: Revised Footnotes (4) and (6). • Table 4, Quiescent Supply Current: Added Footnote (1) and updated Typical parameters. • Table 10, LVPECL DC Specifications: Added parameter values for Maximum Differential Input Voltage (LVPECL). • Table 14, Register-to-Register Performance: Removed reference to a number of designs for which test data is no longer provided. • Table 16, Processor Clocks Absolute AC Characteristics: Added Footnote (1) referring to XAPP755. • Added Table 41, Clock Distribution Switching Characteristics. • Revised section Configuration Timing, page 39 through page 41, and JTAG Test Access Port Switching Characteristics, page 42, with improved timing diagrams, parameter tables, and organization. • Table 50, Master/Slave Serial Mode Timing Characteristics, and Table 51, SelectMAP Mode Write Timing Characteristics: Added parameter $F_{CC\_STARTUP}$. • Table 51, SelectMAP Mode Write Timing Characteristics: Broke out T_{SMDCC}/T_{SMCCD}, DATA[0:7] setup/hold time, by device, and added new parameter specifications for XC2VP70 and XC2VP100 devices. • Table 57, Operating Frequency Ranges: Added callouts for existing Footnote (3) to the four CLKIN parameters. Added new Footnote (4) to the four CLKIN parameters. Added new Footnote (5) to CLK2X, CLK2X180. Added new Footnote (6) to CLK2X, CLK2X180; CLK0, CLK180; and CLKIN (using DLL outputs).
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
04/22/04	3.2	• Table 2, Recommended Operating Conditions: Corrected VTTX/VTRX lower voltage limit from 1.8V to 1.6V. • Table 5, Power-On Current for Virtex-II Pro Devices: Added Footnote (2) stating that listed I_{CCOMIN} values apply to the entire device (all banks). • Table 40, Output Delay Measurement Methodology: Corrected V_{MEAS} for LVTTL from 1.4V to 1.65V. • Table 57, Operating Frequency Ranges: Corrected CLKOUT_FREQ_1X_LF_MAX and CLKIN_FREQ_DLL_LF_MAX for -7 devices from 210 MHz to 270 MHz. • Table 65, Package Skew: Removed XC2VP40FF1517.
06/30/04	4.0	Merged in DS110-3 (Module 3 of Virtex-II Pro X data sheet). This merge added numerous previously unpublished RocketIO X MGT parameters. Specifications in this revision are from speedsfile **v1.86**.

Table 4: **Virtex-II Pro Pin Definitions *(Continued)***

Pin Name	Direction	Description
GCLKx (S/P)	Input/Output	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks. These pins can be used to clock the RocketIO transceiver. See the **RocketIO Transceiver User Guide** for design guidelines and BREFCLK-specific pins, by device.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
V_{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins:(1)		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection. Pin is biased by V_{CCAUX} (must be 2.5V). These pins should not connect to 3.3V unless 100Ω series resistors are used. The mode pins are not to be toggled (changed) while in operation during and after configuration.
HSWAP_EN	Input	Enable I/O pull-ups during configuration.
TCK	Input	Boundary Scan Clock. This pin is 3.3V compatible.
TDI	Input	Boundary Scan Data Input. This pin is 3.3V compatible.
TDO	Output (open-drain)	Boundary Scan Data Output. Pin is open-drain and can be pulled up to 3.3V. It is recommended that the external pull-up be greater than 200Ω. There is no internal pull-up.
TMS	Input	Boundary Scan Mode Select. This pin is 3.3V compatible.
PWRDWN_B	Input *(unsupported)*	Active Low power-down pin (unsupported). *Driving this pin Low can adversely affect device operation and configuration.* PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up.
Other Pins:		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V_{BATT}	Input	Decryptor key memory backup supply. (Connect to V_{CCAUX} or GND if battery not used.)
RSVD	N/A	Reserved pin - do not connect.
V_{CCO}	Input	Power-supply pins for the output drivers (per bank).
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V_{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.
AVCCAUXRX#	Input	Analog power supply for receive circuitry of the RocketIO MGT (2.5V).
AVCCAUXTX#	Input	Analog power supply for transmit circuitry of the RocketIO MGT (2.5V).
BREFCLKN, BREFCLKP(2)	Input	Differential clock input that clocks the RocketIO X MGTs populating the same side of the chip (top or bottom). Can also drive DCMs for RocketIO X MGT use.

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
5	IO_L46N_5	W11			
5	IO_L46P_5	W10			
5	IO_L45N_5/VREF_5	AD9			
5	IO_L45P_5	AC9			
5	IO_L43N_5	AB9			
5	IO_L43P_5	AA9			
5	IO_L39N_5	Y9			
5	IO_L39P_5	W9			
5	IO_L37N_5	AF8			
5	IO_L37P_5	AE8			
5	IO_L09N_5/VREF_5	AB8			
5	IO_L09P_5	AA8			
5	IO_L07N_5/VREF_5	Y8			
5	IO_L07P_5	W8			
5	IO_L06N_5/VRP_5	AD7			
5	IO_L06P_5/VRN_5	AC7			
5	IO_L05_5/No_Pair	AB7			
5	IO_L03N_5/D4	AA7			
5	IO_L03P_5/D5	Y7			
5	IO_L02N_5/D6	AC6			
5	IO_L02P_5/D7	AB6			
5	IO_L01N_5/RDWR_B	AC5			
5	IO_L01P_5/CS_B	AB5			
6	IO_L01P_6/VRN_6	AE1			
6	IO_L01N_6/VRP_6	AD1			
6	IO_L02P_6	AD2			
6	IO_L02N_6	AC3			
6	IO_L03P_6	AC2			
6	IO_L03N_6/VREF_6	AC1			
6	IO_L05P_6	AB4			
6	IO_L05N_6	AA5			
6	IO_L06P_6	AB2			
6	IO_L06N_6	AB1			
6	IO_L23P_6	AA6	NC		

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
6	IO_L55P_6	T2			
6	IO_L55N_6	T1			
6	IO_L57P_6	R9			
6	IO_L57N_6/VREF_6	R8			
6	IO_L59P_6	R6			
6	IO_L59N_6	P6			
6	IO_L60P_6	R5			
6	IO_L60N_6	R4			
6	IO_L85P_6	R2			
6	IO_L85N_6	R1			
6	IO_L87P_6	P9			
6	IO_L87N_6/VREF_6	P8			
6	IO_L89P_6	P5			
6	IO_L89N_6	P4			
6	IO_L90P_6	P3			
6	IO_L90N_6	P2			
7	IO_L90P_7	N2			
7	IO_L90N_7	N3			
7	IO_L88P_7	N4			
7	IO_L88N_7/VREF_7	N5			
7	IO_L86P_7	N8			
7	IO_L86N_7	N9			
7	IO_L85P_7	M1			
7	IO_L85N_7	M2			
7	IO_L60P_7	M4			
7	IO_L60N_7	M5			
7	IO_L58P_7	N6			
7	IO_L58N_7/VREF_7	M6			
7	IO_L56P_7	M8			
7	IO_L56N_7	M9			
7	IO_L55P_7	L1			
7	IO_L55N_7	L2			
7	IO_L54P_7	L5			
7	IO_L54N_7	L6			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	VCCINT	U10			
N/A	VCCINT	U11			
N/A	VCCINT	U16			
N/A	VCCINT	U17			
N/A	VCCINT	U20			
N/A	VCCINT	V9			
N/A	VCCINT	V18			
N/A	VCCINT	Y10			
N/A	VCCINT	Y13			
N/A	VCCINT	Y14			
N/A	VCCINT	Y17			
N/A	VCCAUX	A2			
N/A	VCCAUX	A13			
N/A	VCCAUX	A14			
N/A	VCCAUX	A25			
N/A	VCCAUX	N1			
N/A	VCCAUX	N26			
N/A	VCCAUX	P1			
N/A	VCCAUX	P26			
N/A	VCCAUX	AF2			
N/A	VCCAUX	AF13			
N/A	VCCAUX	AF14			
N/A	VCCAUX	AF25			
N/A	GND	A1			
N/A	GND	A26			
N/A	GND	B2			
N/A	GND	B25			
N/A	GND	C3			
N/A	GND	C24			
N/A	GND	D4			
N/A	GND	D8			
N/A	GND	D19			
N/A	GND	D23			
N/A	GND	F10			
N/A	GND	F17			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
5	IO_L48N_5		AH20	NC		
5	IO_L48P_5		AH21	NC		
5	IO_L47N_5		AE19	NC		
5	IO_L47P_5		AE20	NC		
5	IO_L46N_5		AD18	NC		
5	IO_L46P_5		AC18	NC		
5	IO_L45N_5/VREF_5		AJ22			
5	IO_L45P_5		AH22			
5	IO_L44N_5		AE21			
5	IO_L44P_5		AE22			
5	IO_L43N_5		AD19			
5	IO_L43P_5		AC19			
5	IO_L39N_5		AG21			
5	IO_L39P_5		AF21			
5	IO_L38N_5		AF22			
5	IO_L38P_5		AF23			
5	IO_L37N_5		AD20			
5	IO_L37P_5		AC20			
5	IO_L09N_5/VREF_5		AK23			
5	IO_L09P_5		AJ23			
5	IO_L08N_5		AE23			
5	IO_L08P_5		AE24			
5	IO_L07N_5/VREF_5		AD21			
5	IO_L07P_5		AC21			
5	IO_L06N_5/VRP_5		AH23			
5	IO_L06P_5/VRN_5		AG23			
5	IO_L05_5/No_Pair		AD23			
5	IO_L03N_5/D4		AH24			
5	IO_L03P_5/D5		AG24			
5	IO_L02N_5/D6		AD22			
5	IO_L02P_5/D7		AC22			
5	IO_L01N_5/RDWR_B		AF24			
5	IO_L01P_5/CS_B		AG25			
6	IO_L01P_6/VRN_6		AK28			
6	IO_L01N_6/VRP_6		AJ28			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
6	IO_L86P_6		T23			
6	IO_L86N_6		T24			
6	IO_L87P_6		U28			
6	IO_L87N_6/VREF_6		U29			
6	IO_L88P_6		T27			
6	IO_L88N_6		T28			
6	IO_L89P_6		T25			
6	IO_L89N_6		T26			
6	IO_L90P_6		V30			
6	IO_L90N_6		U30			
7	IO_L90P_7		R28			
7	IO_L90N_7		R27			
7	IO_L89P_7		R26			
7	IO_L89N_7		R25			
7	IO_L88P_7		T29			
7	IO_L88N_7/VREF_7		R29			
7	IO_L87P_7		P27			
7	IO_L87N_7		P26			
7	IO_L86P_7		R24			
7	IO_L86N_7		R23			
7	IO_L85P_7		P29			
7	IO_L85N_7		P28			
7	IO_L60P_7		N28			
7	IO_L60N_7		N27			
7	IO_L59P_7		P24			
7	IO_L59N_7		P23			
7	IO_L58P_7		P30			
7	IO_L58N_7/VREF_7		N30			
7	IO_L57P_7		M28			
7	IO_L57N_7		M27			
7	IO_L56P_7		R22			
7	IO_L56N_7		P22			
7	IO_L55P_7		N29			
7	IO_L55N_7		M29			
7	IO_L54P_7		L27			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
4	VCCO_4		AA11			
4	VCCO_4		AA10			
5	VCCO_5		AB21			
5	VCCO_5		AB20			
5	VCCO_5		AB19			
5	VCCO_5		AB18			
5	VCCO_5		AA21			
5	VCCO_5		AA20			
5	VCCO_5		AA19			
5	VCCO_5		AA18			
5	VCCO_5		AA17			
5	VCCO_5		AA16			
6	VCCO_6		AB22			
6	VCCO_6		AA22			
6	VCCO_6		Y22			
6	VCCO_6		Y21			
6	VCCO_6		W22			
6	VCCO_6		W21			
6	VCCO_6		V22			
6	VCCO_6		V21			
6	VCCO_6		U21			
6	VCCO_6		T21			
7	VCCO_7		R21			
7	VCCO_7		P21			
7	VCCO_7		N22			
7	VCCO_7		N21			
7	VCCO_7		M22			
7	VCCO_7		M21			
7	VCCO_7		L22			
7	VCCO_7		L21			
7	VCCO_7		K22			
7	VCCO_7		J22			
N/A	CCLK		AC7			
N/A	PROG_B		G24			
N/A	DONE		AC8			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
4	IO_L27P_4/VREF_4	AL10	NC	NC		
4	IO_L37N_4	AE13				
4	IO_L37P_4	AF13				
4	IO_L38N_4	AG13				
4	IO_L38P_4	AH13				
4	IO_L39N_4	AJ11				
4	IO_L39P_4	AK11				
4	IO_L43N_4	AE14				
4	IO_L43P_4	AF14				
4	IO_L44N_4	AJ13				
4	IO_L44P_4	AK13				
4	IO_L45N_4	AL11				
4	IO_L45P_4/VREF_4	AM11				
4	IO_L46N_4	AE15				
4	IO_L46P_4	AF15				
4	IO_L47N_4	AG14				
4	IO_L47P_4	AH14				
4	IO_L48N_4	AL13				
4	IO_L48P_4	AL12				
4	IO_L49N_4	AD16				
4	IO_L49P_4	AE16				
4	IO_L50_4/No_Pair	AJ14				
4	IO_L53_4/No_Pair	AK14				
4	IO_L54N_4	AM14				
4	IO_L54P_4	AM13				
4	IO_L55N_4	AF16				
4	IO_L55P_4	AG16				
4	IO_L56N_4	AH15				
4	IO_L56P_4	AJ15				
4	IO_L57N_4	AL14				
4	IO_L57P_4/VREF_4	AL15				
4	IO_L67N_4	AD17				
4	IO_L67P_4	AE17				
4	IO_L68N_4	AH16				
4	IO_L68P_4	AJ16				
4	IO_L69N_4	AK16				
4	IO_L69P_4/VREF_4	AL16				
4	IO_L73N_4	AF17				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
4	VCCO_4	AD12		
4	VCCO_4	AL11		
4	VCCO_4	AG11		
3	VCCO_3	AB12		
3	VCCO_3	AA12		
3	VCCO_3	Y12		
3	VCCO_3	W12		
3	VCCO_3	V12		
3	VCCO_3	AC11		
3	VCCO_3	AF9		
3	VCCO_3	AM8		
3	VCCO_3	AH8		
3	VCCO_3	AD8		
3	VCCO_3	Y8		
3	VCCO_3	AM4		
3	VCCO_3	AH4		
3	VCCO_3	AD4		
3	VCCO_3	Y4		
3	VCCO_3	AK2		
2	VCCO_2	U12		
2	VCCO_2	T12		
2	VCCO_2	R12		
2	VCCO_2	P12		
2	VCCO_2	N12		
2	VCCO_2	M11		
2	VCCO_2	J9		
2	VCCO_2	R8		
2	VCCO_2	L8		
2	VCCO_2	G8		
2	VCCO_2	C8		
2	VCCO_2	R4		
2	VCCO_2	L4		
2	VCCO_2	G4		
2	VCCO_2	C4		
2	VCCO_2	E2		
1	VCCO_1	M17		
1	VCCO_1	M16		
1	VCCO_1	M15		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L53N_3		AE10		
3	IO_L53P_3		AE11		
3	IO_L52N_3		AE1		
3	IO_L52P_3		AE2		
3	IO_L51N_3/VREF_3		AE4		
3	IO_L51P_3		AE5		
3	IO_L50N_3		AF11		
3	IO_L50P_3		AE12		
3	IO_L49N_3		AE7		
3	IO_L49P_3		AE8		
3	IO_L48N_3		AF1		
3	IO_L48P_3		AF2		
3	IO_L47N_3		AG12		
3	IO_L47P_3		AF12		
3	IO_L46N_3		AF3		
3	IO_L46P_3		AF4		
3	IO_L45N_3/VREF_3		AF5		
3	IO_L45P_3		AF6		
3	IO_L44N_3		AF7		
3	IO_L44P_3		AF8		
3	IO_L43N_3		AF9		
3	IO_L43P_3		AF10		
3	IO_L42N_3		AG2		
3	IO_L42P_3		AG3		
3	IO_L41N_3		AG10		
3	IO_L41P_3		AG11		
3	IO_L40N_3		AG4		
3	IO_L40P_3		AG5		
3	IO_L39N_3/VREF_3		AG6		
3	IO_L39P_3		AG7		
3	IO_L38N_3		AG8		
3	IO_L38P_3		AH8		
3	IO_L37N_3		AH1		
3	IO_L37P_3		AH2		
3	IO_L36N_3		AH3		
3	IO_L36P_3		AJ3		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L03P_7		D37		
7	IO_L03N_7		E37		
7	IO_L02P_7		D36		
7	IO_L02N_7		E36		
7	IO_L01P_7/VRN_7		C37		
7	IO_L01N_7/VRP_7		C38		
0	VCCO_0		D25		
0	VCCO_0		G23		
0	VCCO_0		G28		
0	VCCO_0		G32		
0	VCCO_0		J25		
0	VCCO_0		J29		
0	VCCO_0		P22		
0	VCCO_0		P23		
0	VCCO_0		P24		
0	VCCO_0		P25		
0	VCCO_0		P26		
0	VCCO_0		R22		
0	VCCO_0		R23		
0	VCCO_0		R24		
0	VCCO_0		R25		
1	VCCO_1		R21		
1	VCCO_1		R20		
1	VCCO_1		R19		
1	VCCO_1		R18		
1	VCCO_1		P21		
1	VCCO_1		P20		
1	VCCO_1		P19		
1	VCCO_1		P18		
1	VCCO_1		P17		
1	VCCO_1		J18		
1	VCCO_1		J14		
1	VCCO_1		G20		
1	VCCO_1		G15		
1	VCCO_1		G11		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCAUX	A2	
N/A	VCCAUX	BA1	
N/A	VCCAUX	AY1	
N/A	VCCAUX	AL1	
N/A	VCCAUX	AB1	
N/A	VCCAUX	AA1	
N/A	VCCAUX	M1	
N/A	VCCAUX	C1	
N/A	VCCAUX	B1	
N/A	GND	AV42	
N/A	GND	AP42	
N/A	GND	AK42	
N/A	GND	AF42	
N/A	GND	AC42	
N/A	GND	Y42	
N/A	GND	U42	
N/A	GND	N42	
N/A	GND	J42	
N/A	GND	E42	
N/A	GND	BA41	
N/A	GND	AY41	
N/A	GND	C41	
N/A	GND	B41	
N/A	GND	BA40	
N/A	GND	B40	
N/A	GND	BB38	
N/A	GND	AV38	
N/A	GND	AP38	
N/A	GND	AK38	
N/A	GND	AF38	
N/A	GND	AC38	
N/A	GND	Y38	
N/A	GND	U38	
N/A	GND	N38	
N/A	GND	J38	
N/A	GND	E38	
N/A	GND	A38	