Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	352
Number of Logic Elements/Cells	3168
Total RAM Bits	221184
Number of I/O	140
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp2-7fgg256c

  - HyperTransport (LDT) I/O with current driver buffers
  - Built-in DDR input and output registers
- Proprietary high-performance SelectLink technology for communications between Xilinx devices
  - High-bandwidth data path
  - Double Data Rate (DDR) link
  - Web-based HDL generation methodology
- SRAM-Based In-System Configuration
  - Fast SelectMAP™ configuration
  - Triple Data Encryption Standard (DES) security option (bitstream encryption)
  - IEEE 1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Integrated VHDL and Verilog design flows
  - ChipScope™ Integrated Logic Analyzer
- 0.13 µm Nine-Layer Copper Process with 90 nm High-Speed Transistors
- 1.5V (V_{CCINT}) core power supply, dedicated 2.5V V_{CCAUX} auxiliary and V_{CCO} I/O power supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) Packages in Standard 1.00 mm Pitch.
- Wire-Bond BGA Devices Available in Pb-Free Packaging (**www.xilinx.com/pbfree)**
- Each Device 100% Factory Tested

General Description

The Virtex-II Pro and Virtex-II Pro X families contain platform FPGAs for designs that are based on IP cores and customized modules. The family incorporates multi-gigabit transceivers and PowerPC CPU blocks in Virtex-II Pro Series FPGA architecture. It empowers complete solutions for telecommunication, wireless, networking, video, and DSP applications.

The leading-edge 0.13 µm CMOS nine-layer copper process and Virtex-II Pro architecture are optimized for high performance designs in a wide range of densities. Combining a wide variety of flexible features and IP cores, the Virtex-II Pro family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gate arrays.

Architecture

Array Overview

Virtex-II Pro and Virtex-II Pro X devices are user-programmable gate arrays with various configurable elements and embedded blocks optimized for high-density and high-performance system designs. Virtex-II Pro devices implement the following functionality:

- Embedded high-speed serial transceivers enable data bit rate up to 3.125 Gb/s per channel (RocketIO) or 6.25 Gb/s (RocketIO X).
- Embedded IBM PowerPC 405 RISC processor blocks provide performance up to 400 MHz.
- SelectIO-Ultra blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.
- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM+ memory modules provide large 18 Kb storage elements of True Dual-Port RAM.
- Embedded multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, and coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and supports high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Features

This section briefly describes Virtex-II Pro / Virtex-II Pro X features. For more details, refer to Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description.

RocketIO / RocketIO X MGT Cores

The RocketIO and RocketIO X Multi-Gigabit Transceivers are flexible parallel-to-serial and serial-to-parallel embedded transceiver cores used for high-bandwidth interconnection between buses, backplanes, or other subsystems.

Multiple user instantiations in an FPGA are possible, providing up to 100 Gb/s (RocketIO) or 170 Gb/s (RocketIO X) of full-duplex raw data transfer. Each channel can be operated at a maximum data transfer rate of 3.125 Gb/s (RocketIO) or 6.25 Gb/s (RocketIO X).

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/13/02	2.0	New Virtex-II Pro family members. New timing parameters per speedsfile **v1.62**.
09/03/02	2.1	Updates to Table 1 and Table 3. Processor Block information added to Table 4.
09/27/02	2.2	In Table 1, correct max number of XC2VP30 I/Os to 644.
11/20/02	2.3	Add bullet items for 3.3V I/O features.
01/20/03	2.4	• In Table 3, add FG676 package option for XC2VP20, XC2VP30, and XC2VP40. • Remove FF1517 package option for XC2VP40.
03/24/03	2.4.1	• Correct number of single-ended I/O standards from 19 to 22. • Correct minimum RocketIO serial speed from 622 Mbps to 600 Mbps.
08/25/03	2.4.2	• Add footnote referring to XAPP659 to callout for 3.3V I/O standards on page 4.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Table 1: Corrected number of RocketIO transceiver blocks for XC2VP40. • Section Virtex-II Pro Platform FPGA Technology (All Devices): Updated number of differential standards supported from six to ten. • Section Input/Output Blocks (IOBs): Added text stating that differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards. • Figure 1: Added note stating that -7 devices are not available in Industrial grade.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/30/04	4.0	Merged in DS110-1 (Module 1 of Virtex-II Pro X data sheet). Added information on available Pb-free packages.
11/17/04	4.1	*No changes in Module 1 for this revision.*
03/01/05	4.2	Table 3: Corrected number of RocketIO transceivers for XC2VP7-FG456.
06/20/05	4.3	*No changes in Module 1 for this revision.*
09/15/05	4.4	• Changed all instances of 10.3125 Gb/s (RocketIO transceiver maximum bit rate) to 6.25 Gb/s. • Changed all instances of 412.5 Gb/s (RocketIO X transceiver maximum multi-channel raw data transfer rate) to 250 Gb/s.
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s. • Changed maximum performance for -7 Virtex-II Pro X MGT (Table 4) to N/A.
03/05/07	4.6	*No changes in Module 1 for this revision.*
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner.

Output Swing and Emphasis

The output swing and emphasis levels are fully programmable. Each is controlled via attributes at configuration, and can be modified via the PMA attribute programming bus.

The programmable output swing control can adjust the differential peak-to-peak output level between 200 mV and 1600 mV.

With emphasis, the differential voltage swing is boosted to create a stronger rising or falling waveform. This method compensates for high frequency loss in the transmission media that would otherwise limit the magnitude of this waveform. Lossy transmission lines cause the dissipation of electrical energy. This emphasis technique extends the distance that signals can be driven down lossy line media and increases the signal-to-noise ratio at the receiver.

Emphasis can be described from two perspectives, additive to the smaller voltage (V_{SM}) (pre-emphasis) or subtractive from the larger voltage (V_{LG}) (de-emphasis). The resulting benefits in compensating for channel loss are identical. It is simply a relative way of specifying the effect at the transmitter.

The equations for calculating pre-emphasis as a percentage and dB are as follows:

$$\text{Pre-Emphasis}_{\%} = ((V_{LG}-V_{SM}) / V_{SM}) \times 100$$
$$\text{Pre-Emphasis}_{dB} = 20 \log(V_{LG}/V_{SM})$$

The equations for calculating de-emphasis as a percentage and dB are as follows:

$$\text{De-Emphasis}_{\%} = (V_{LG} - V_{SM}) / V_{LG}) \times 100$$
$$\text{De-Emphasis}_{dB} = 20 \log(V_{SM}/V_{LG})$$

The pre-emphasis amount can be programmed in discrete steps between 0% and 500%. The de-emphasis amount can be programmed in discrete steps between 0% and 83%.

Serializer

The serializer multiplies the reference frequency provided on REFCLK by 10, 16, 20, 32, or 40, depending on the operation mode. The multiplication of the clock is achieved by using an embedded PLL.

Data is converted from parallel to serial format and transmitted on the TXP and TXN differential outputs. The electrical connection of TXP and TXN can be interchanged through configuration. This option can be controlled by an input (TXPOLARITY) at the FPGA transmitter interface.

Deserializer

Synchronous serial data reception is facilitated by a clock and data recovery (CDR) circuit. This circuit uses a fully monolithic Phase Lock Loop (PLL), which does not require any external components. The CDR circuit extracts both phase and frequency from the incoming data stream.

The derived clock, RXRECCLK, is generated and locked to as long as it remains within the specified component range. This clock is presented to the FPGA fabric at $^1/_{10}$, $^1/_{16}$, $^1/_{20}$, $^1/_{32}$, or $^1/_{40}$ the incoming data rate depending on the operating mode.

A sufficient number of transitions must be present in the data stream for CDR to work properly. The CDR circuit is guaranteed to work with 8B/10B and 64B/66B encoding. Further, CDR requires approximately 5,000 transitions upon power-up to guarantee locking to the incoming data rate. Once lock is achieved, up to 75 missing transitions can be tolerated before lock to the incoming data stream is lost.

Another feature of CDR is its ability to accept an external precision reference clock, REFCLK, which either acts to clock incoming data or to assist in synchronizing the derived RXRECCLK.

For further clarity, the TXUSRCLK is used to clock data from the FPGA fabric to the TX FIFO. The FIFO depth accounts for the slight phase difference between these two clocks. If the clocks are locked in frequency, then the FIFO acts much like a pass-through buffer.

The receiver can be configured to reverse the RXP and RXN inputs. This can be useful in the event that printed circuit board traces have been reversed.

Receiver Lock Control

The CDR circuits will lock to the reference clock automatically if the data is not present. For proper operation, the frequency of the reference clock must be within ±100 ppm of the nominal frequency.

During normal operation, the receiver PLL automatically locks to incoming data (when present) or to the local reference clock (when data is not present). This is the default configuration for all primitives. This function can be overridden via the PMARXLOCKSEL port

When receive PLL lock is forced to the local reference, phase information from the incoming data stream is ignored. Data continues to be sampled, but synchronous to the local reference rather than relative to edges in the data stream.

Receive Equalization

In addition to transmit emphasis, the RocketIO X MGT provides a programmable active receive equalization feature to further compensate the effects of channel attenuation at high frequencies.

By adjusting RXFER, the right amount of equalization can be added to reverse the signal degradation caused by a printed circuit board, a backplane, or a line/switch card. RXFER can be set through software configuration or the PMA Attribute Bus.

Receiver Termination

On-chip termination is provided at the receiver, eliminating the need for external termination. The receiver termination supply (V_{TRX}) is the center tap of differential termination to

The top half of the figure shows the transmission of words split across four transceivers (channels or lanes). PPPP, QQQQ, RRRR, SSSS, and TTTT represent words sent over the four channels.

The bottom-left portion of Figure 13 shows the initial situation in the FPGA's receivers at the other end of the four channels. Due to variations in transmission delay—especially if the channels are routed through repeaters—the FPGA fabric might not correctly assemble the bytes into complete words. The bottom-left illustration shows the incorrect assembly of data words PQPP, QRQQ, RSRR, and so forth.

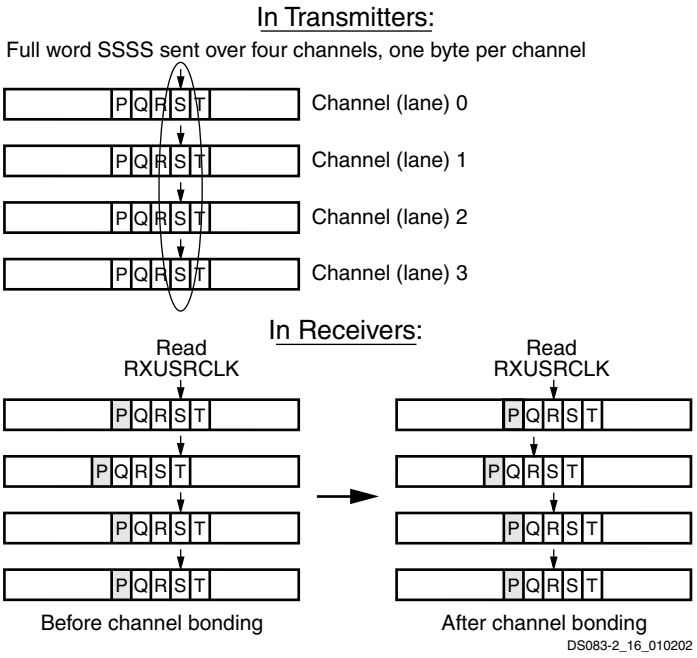


Figure 13: **Channel Bonding (Alignment)**

To support correction of this misalignment, the data stream includes special byte sequences that define corresponding points in the several channels. In the bottom half of Figure 13, the shaded "P" bytes represent these special characters. Each receiver recognizes the "P" channel bonding character, and remembers its location in the buffer. At some point, one transceiver designated as the master instructs all the transceivers to align to the channel bonding character "P" (or to some location relative to the channel bonding character).

After this operation, words transmitted to the FPGA fabric are properly aligned: RRRR, SSSS, TTTT, and so forth, as shown in the bottom-right portion of Figure 13. To ensure that the channels remain properly aligned following the channel bonding operation, the master transceiver must also control the clock correction operations described in the previous section for all channel-bonded transceivers.

Transmitter Buffer

The transmitter's buffer write pointer (TXUSRCLK) is frequency-locked to its read pointer (REFCLK). Therefore, clock correction and channel bonding are not required. The purpose of the transmitter's buffer is to accommodate a phase difference between TXUSRCLK and REFCLK. A simple FIFO suffices for this purpose. A FIFO depth of four will permit reliable operation with simple detection of overflow or underflow, which could occur if the clocks are not frequency-locked.

RocketIO Configuration

This section outlines functions that can be selected or controlled by configuration. Xilinx implementation software supports 16 transceiver primitives, as shown in Table 6.

Each of the primitives in Table 6 defines default values for the configuration attributes, allowing some number of them to be modified by the user. Refer to the ***RocketIO Transceiver User Guide*** for more details.

Table 6: **Supported RocketIO MGT Protocol Primitives**

GT_CUSTOM	Fully customizable by user
GT_FIBRE_CHAN_1	Fibre Channel, 1-byte data path
GT_FIBRE_CHAN_2	Fibre Channel, 2-byte data path
GT_FIBRE_CHAN_4	Fibre Channel, 4-byte data path
GT_ETHERNET_1	Gigabit Ethernet, 1-byte data path
GT_ETHERNET_2	Gigabit Ethernet, 2-byte data path
GT_ETHERNET_4	Gigabit Ethernet, 4-byte data path
GT_XAUI_1	10-gigabit Ethernet, 1-byte data path
GT_XAUI_2	10-gigabit Ethernet, 2-byte data path
GT_XAUI_4	10-gigabit Ethernet, 4-byte data path
GT_INFINIBAND_1	Infiniband, 1-byte data path
GT_INFINIBAND_2	Infiniband, 2-byte data path
GT_INFINIBAND_4	Infiniband, 4-byte data path
GT_AURORA_1(1)	1-byte data path
GT_AURORA_2(1)	2-byte data path
GT_AURORA_4(1)	4-byte data path

Notes:
1. For more information on the Aurora protocol, visit http://www.xilinx.com.

Other RocketIO Features and Notes

CRC

The RocketIO transceiver CRC logic supports the 32-bit invariant CRC calculation used by Infiniband, FibreChannel, and Gigabit Ethernet.

On the transmitter side, the CRC logic recognizes where the CRC bytes should be inserted and replaces four placeholder bytes at the tail of a data packet with the computed CRC. For Gigabit Ethernet and FibreChannel, transmitter

The Trace port provides instruction execution trace information to an external trace tool. The PPC405 core is capable of back trace and forward trace. Back trace is the tracing of instructions prior to a debug event while forward trace is the tracing of instructions after a debug event.

The processor JTAG port and the FPGA JTAG port can be accessed independently, or the two can be programmatically linked together and accessed via the dedicated FPGA JTAG pins.

For detailed information on the PPC405 JTAG interface, please refer to the "JTAG Interface" section of the **PowerPC 405 Processor Block Reference Guide**

CoreConnect™ Bus Architecture

The Processor Block is compatible with the CoreConnect™ bus architecture. Any CoreConnect compliant cores including Xilinx soft IP can integrate with the Processor Block through this high-performance bus architecture implemented on FPGA fabric.

The CoreConnect architecture provides three buses for interconnecting Processor Blocks, Xilinx soft IP, third party IP, and custom logic, as shown in Figure 15:

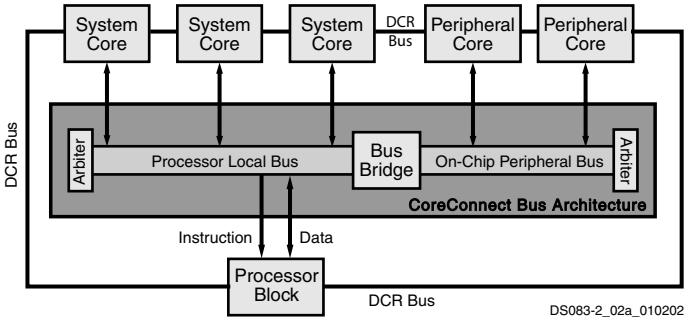


Figure 15: **CoreConnect Block Diagram**

- Processor Local Bus (PLB)
- On-Chip Peripheral Bus (OPB)
- Device Control Register (DCR) bus

High-performance peripherals connect to the high-bandwidth, low-latency PLB. Slower peripheral cores connect to the OPB, which reduces traffic on the PLB, resulting in greater overall system performance.

For more information, refer to:
http://www-3.ibm.com/chips/techlib/techlib.nfs/productfamilies/CoreConnect_Bus_Architecture/

Functional Description: Embedded PowerPC 405 Core

This section offers a brief overview of the various functional blocks shown in Figure 16.

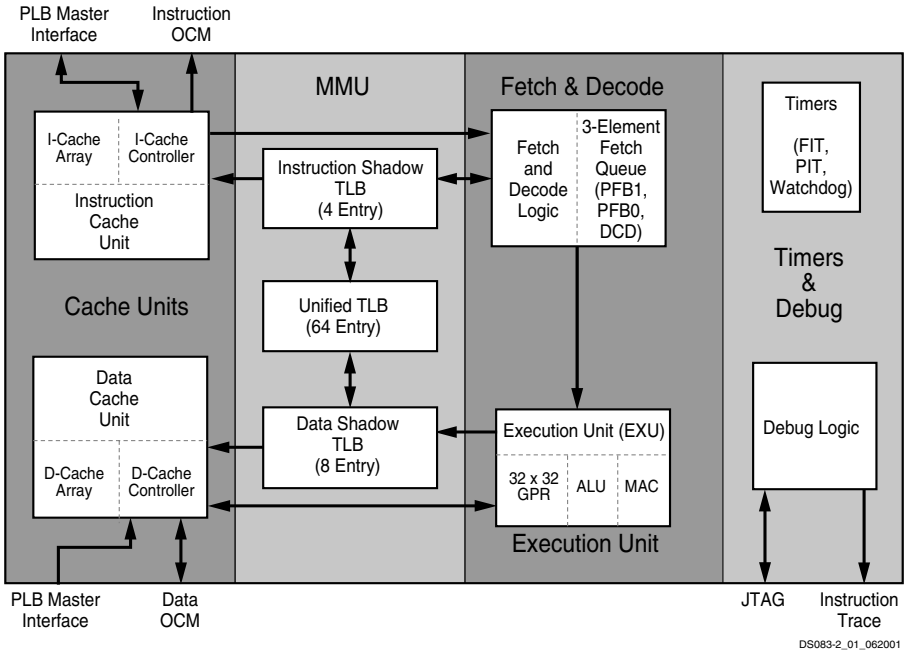


Figure 16: **Embedded PPC405 Core Block Diagram**

Embedded PPC405 Core

The embedded PPC405 core is a 32-bit Harvard architecture processor. Figure 16 illustrates its functional blocks:

- Cache units
- Memory Management unit
- Fetch Decode unit

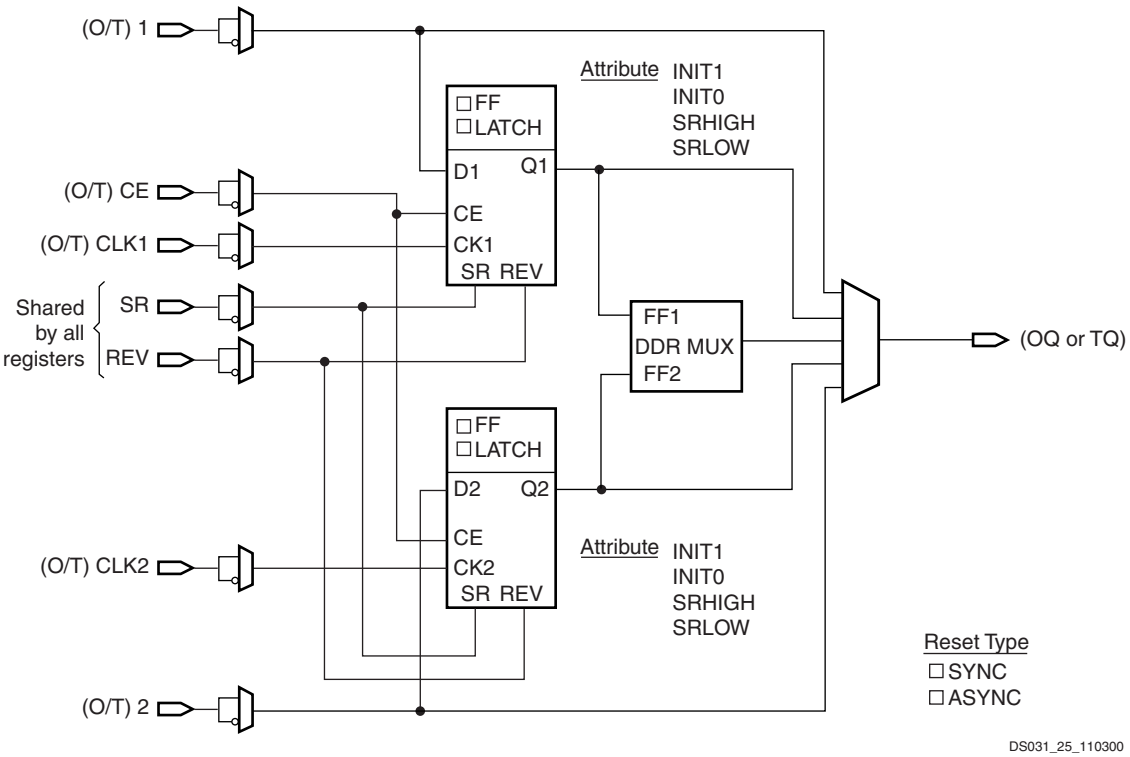


Figure 21: **Register / Latch Configuration in an IOB Block**

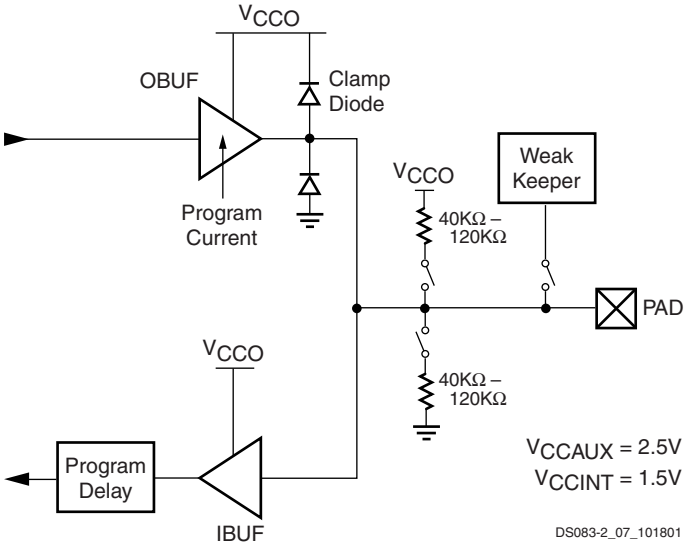


Figure 22: **LVTTL, LVCMOS, or PCI SelectIO-Ultra Standard**

Input/Output Individual Options

Each device pad has optional pull-up/pull-down resistors and weak-keeper circuit in the LVTTL, LVCMOS, and PCI SelectIO-Ultra configurations, as illustrated in Figure 22. Values of the optional pull-up and pull-down resistors fall within a range of 40 KΩ to 120 KΩ when V_{CCO} = 2.5V (from 2.38V to 2.63V only). The clamp diodes are always present, even when power is not.

The optional weak-keeper circuit is connected to each user I/O pad. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low. If the pin is connected to a multiple-source signal, the weak-keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter. An enabled pull-up or pull-down overrides the weak-keeper circuit.

LVCMOS25 sinks and sources current up to 24 mA. The current is programmable (see Table 11). Drive strength and slew rate controls for each output driver minimize bus transients. For LVDCI and LVDCI_DV2 standards, drive strength and slew rate controls are not available.

Table 12: **Summary of Voltage Supply Requirements for All Input and Output Standards**

I/O Standard	V_{CCO}		V_{REF}	Termination Type	
	Output	Input	Input	Output	Input
LVTTL(1)	3.3	3.3	N/R	N/R	N/R
LVCMOS33(1)			N/R	N/R	N/R
LVDCI_33(1)			N/R	Series	N/R
PCIX(2)			N/R	N/R	N/R
PCI33_3(2)			N/R	N/R	N/R
PCI66_3(2)			N/R	N/R	N/R
LVDS_25	2.5	Note (3)	N/R	N/R	N/R
LVDSEXT_25			N/R	N/R	N/R
LDT_25			N/R	N/R	N/R
ULVDS_25			N/R	N/R	N/R
BLVDS_25			N/R	N/R	N/R
LVPECL_25			N/R	N/R	N/R
SSTL2_I			1.25	N/R	N/R
SSTL2_II			1.25	N/R	N/R
LVCMOS25		2.5	N/R	N/R	N/R
LVDCI_25			N/R	Series	N/R
LVDCI_DV2_25			N/R	Series	N/R
LVDS_25_DCI			N/R	N/R	Split
LVDSEXT_25_DCI			N/R	N/R	Split
SSTL2_I_DCI			1.25	N/R	Split
SSTL2_II_DCI			1.25	Split	Split
LVDS_25_DT			N/R	N/R	N/R
LVDSEXT_25_DT			N/R	N/R	N/R
LDT_25_DT			N/R	N/R	N/R
ULVDS_25_DT			N/R	N/R	N/R

Table 12: **Summary of Voltage Supply Requirements for All Input and Output Standards *(Continued)***

I/O Standard	V_{CCO}		V_{REF}	Termination Type	
	Output	Input	Input	Output	Input
HSTL_III_18	1.8	Note (3)	1.1	N/R	N/R
HSTL_IV_18			1.1	N/R	N/R
HSTL_I_18			0.9	N/R	N/R
HSTL_II_18			0.9	N/R	N/R
SSTL18_I			0.9	N/R	N/R
SSTL18_II			0.9	N/R	N/R
LVCMOS18		1.8	N/R	N/R	N/R
LVDCI_18			N/R	Series	N/R
LVDCI_DV2_18			N/R	Series	N/R
HSTL_III_DCI_18			1.1	N/R	Single
HSTL_IV_DCI_18			1.1	Single	Single
HSTL_I_DCI_18			0.9	N/R	Split
HSTL_II_DCI_18			0.9	Split	Split
SSTL18_I_DCI			0.9	N/R	Split
SSTL18_II_DCI			0.9	Split	Split
HSTL_III	1.5	Note (3)	0.9	N/R	N/R
HSTL_IV			0.9	N/R	N/R
HSTL_I			0.75	N/R	N/R
HSTL_II			0.75	N/R	N/R
LVCMOS15		1.5	N/R	N/R	N/R
LVDCI_15			N/R	Series	N/R
LVDCI_DV2_15			N/R	Series	N/R
GTLP_DCI			1	Single	Single
HSTL_III_DCI			0.9	N/R	Single
HSTL_IV_DCI			0.9	Single	Single
HSTL_I_DCI			0.75	N/R	Split
HSTL_II_DCI			0.75	Split	Split
GTL_DCI	1.2	1.2	0.8	Single	Single
GTLP	N/R	Note (3)	1	N/R	N/R
GTL			0.8	N/R	N/R

Notes:
1. See application note **XAPP659** for more detailed information.
2. See application note **XAPP653** for more detailed information.
3. Pin voltage must not exceed V_{CCO}.
4. N/R = no requirement.

Sum of Products

Each Virtex-II Pro slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice, as shown in Figure 43.

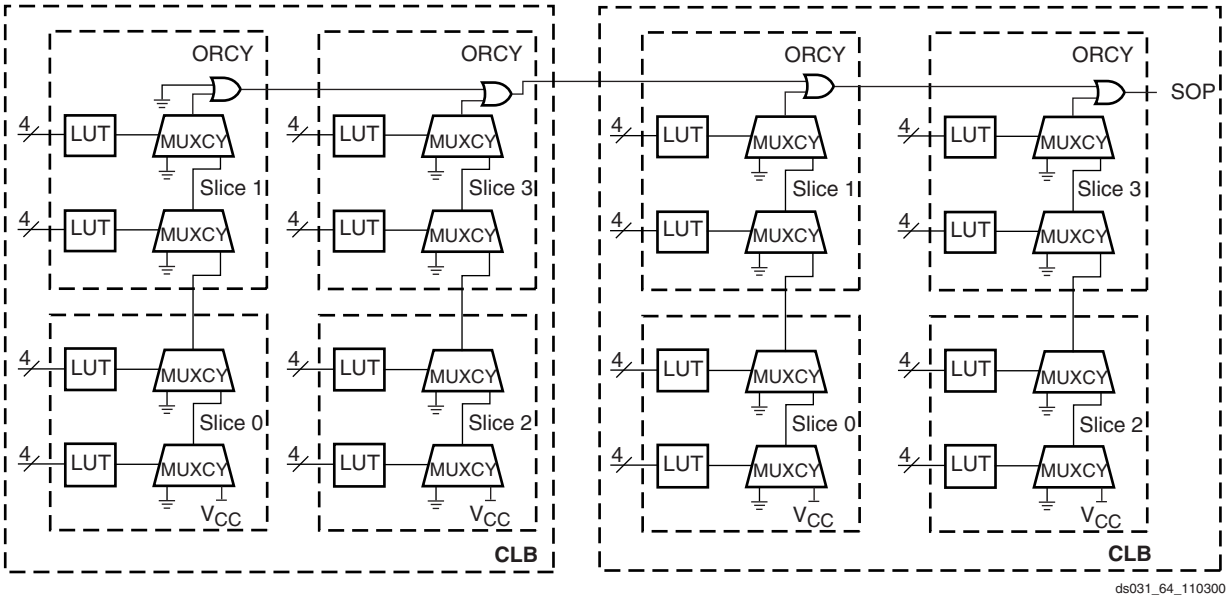


Figure 43: **Horizontal Cascade Chain**

LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 44 illustrates LUT and MUXCY resources configured as a 16-input AND gate.

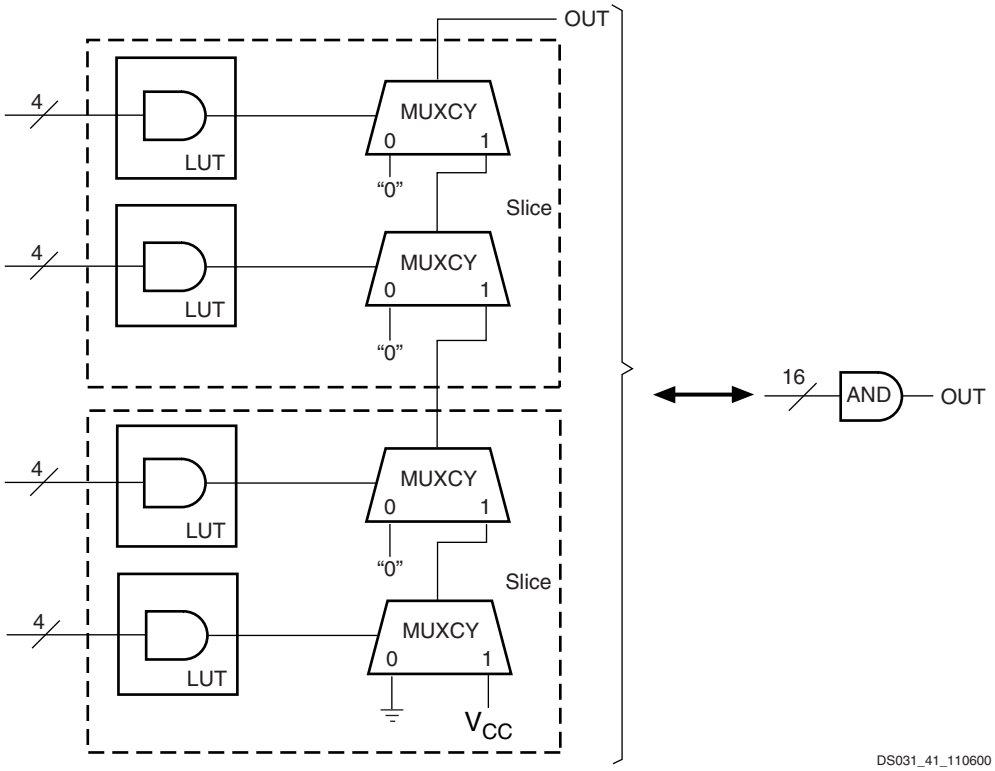


Figure 44: **Wide-Input AND Gate (16 Inputs)**

Table 32: **RocketIO RXUSRCLK2 Switching Characteristics *(Continued)***

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
RXBUFSTATUS status outputs	$T_{GCKST_}$RBSTA	0.45	0.45	0.50	ns, max
RXCHECKINGCRC status output	$T_{GCKST_}$RCCRC	0.36	0.40	0.44	ns, max
RXCRCERR status output	$T_{GCKST_}$RCRCE	0.36	0.40	0.44	ns, max
CHBONDDONE status output	$T_{GCKST_}$CHBD	0.50	0.50	0.55	ns, max
RXCHARISK status outputs	$T_{GCKST_}$RKCH	0.50	0.50	0.55	ns, max
RXRUNDISP status outputs	$T_{GCKST_}$RRDIS	0.50	0.50	0.55	ns, max
RXDATA data outputs	$T_{GCKDO_}$RDAT	0.50	0.50	0.55	ns, max
Clock					
RXUSRCLK2 minimum pulse width, High	$T_{GPWH_}$RX2	1.42	1.42	2.25	ns, min
RXUSRCLK2 minimum pulse width, Low	$T_{GPWL_}$RX2	1.42	1.42	2.25	ns, min

Table 33: **RocketIO X TXUSRCLK2 Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (TXUSRCLK2)					
TXBYPASS8B10B control inputs	$T_{GCCK_}$TBYP/$T_{GCKC_}$TBYP				ns, min
TXPOLARITY control input	$T_{GCCK_}$TPOL/$T_{GCKC_}$TPOL				ns, min
TXINHIBIT control inputs	$T_{GCCK_}$TINH/$T_{GCKC_}$TINH				ns, min
LOOPBACK control inputs	$T_{GCCK_}$LBK/$T_{GCKC_}$LBK				ns, min
TXRESET control input	$T_{GCCK_}$TRST/$T_{GCKC_}$TRST				ns, min
TXCHARISK control inputs	$T_{GCCK_}$TKCH/$T_{GCKC_}$TKCH				ns, min
TXCHARDISPMODE control inputs	$T_{GCCK_}$TCDM/$T_{GCKC_}$TCDM				ns, min
TXCHARDISPVAL control inputs	$T_{GCCK_}$TCDV/$T_{GCKC_}$TCDV				ns, min
TXDATAWIDTH control inputs	$T_{GCCK_}$TDATW/$T_{GCCK_}$TDATW				ns, min
TXENC64B66BUSE TXENC8B10BUSE control inputs	$T_{GCCK_}$TENC/$T_{GCCK_}$TENC				ns, min
TXINTDATAWIDTH control inputs	$T_{GCCK_}$TIDATW/$T_{GCCK_}$TIDATW				ns, min
TXGEARBOX64B66BUSE control inputs	$T_{GCCK_}$TXGEAR/$T_{GCCK_}$TXGEAR				ns, min
TXSCRAM64B66BUSE control inputs	$T_{GCCK_}$TXSCBL/$T_{GCCK_}$TXSCBL				ns, min
REFCLKSEL REFCLKBSEL control inputs	$T_{GCCK_}$RFCKSL/$T_{GCCK_}$RFCKSL				ns, min
TXDATA data inputs	$T_{GDCK_}$TDAT/$T_{GCKD_}$TDAT				ns, min
Clock to Out					
TXBUFERR status output	$T_{GCKST_}$TBERR				ns, max
TXKERR status outputs	$T_{GCKST_}$TKERR				ns, max
TXRUNDISP status outputs	$T_{GCKST_}$TRDIS				ns, max
Clock					
TXUSRCLK2 minimum pulse width, High	$T_{GPWH_}$TX2				ns, min
TXUSRCLK2 minimum pulse width, Low	$T_{GPWL_}$TX2				ns, min

JTAG Test Access Port Switching Characteristics

Characterization data for some of the most commonly requested timing parameters shown in Figure 11 is listed in Table 52.

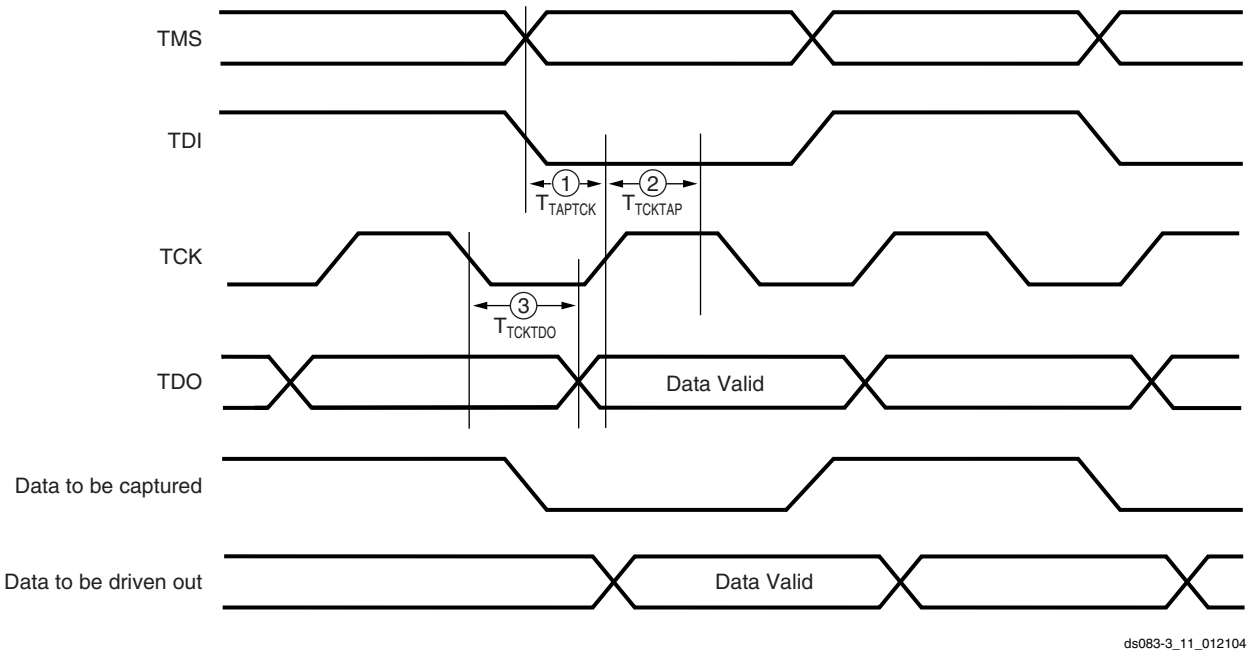


Figure 11: **Virtex-II Pro Boundary Scan Port Timing Waveforms**

Table 52: **Boundary-Scan Port Timing Specifications**

	Description	Figure References	Symbol	Value	Units
TCK	TMS and TDI setup time	1	T_{TAPTCK}	5.5	ns, min
	TMS and TDI hold times	2	T_{TCKTAP}	2.0	ns, min
	Falling edge to TDO output valid	3	T_{TCKTDO}	11.0	ns, max
	Maximum frequency		F_{TCK}	33.0	MHz, max

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	GND		U18			
N/A	GND		U17			
N/A	GND		U16			
N/A	GND		U15			
N/A	GND		U14			
N/A	GND		U13			
N/A	GND		U12			
N/A	GND		U6			
N/A	GND		T19			
N/A	GND		T18			
N/A	GND		T17			
N/A	GND		T16			
N/A	GND		T15			
N/A	GND		T14			
N/A	GND		T13			
N/A	GND		T12			
N/A	GND		R19			
N/A	GND		R18			
N/A	GND		R17			
N/A	GND		R16			
N/A	GND		R15			
N/A	GND		R14			
N/A	GND		R13			
N/A	GND		R12			
N/A	GND		P25			
N/A	GND		P19			
N/A	GND		P18			
N/A	GND		P17			
N/A	GND		P16			
N/A	GND		P15			
N/A	GND		P14			
N/A	GND		P13			
N/A	GND		P12			
N/A	GND		P6			
N/A	GND		N19			
N/A	GND		N18			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

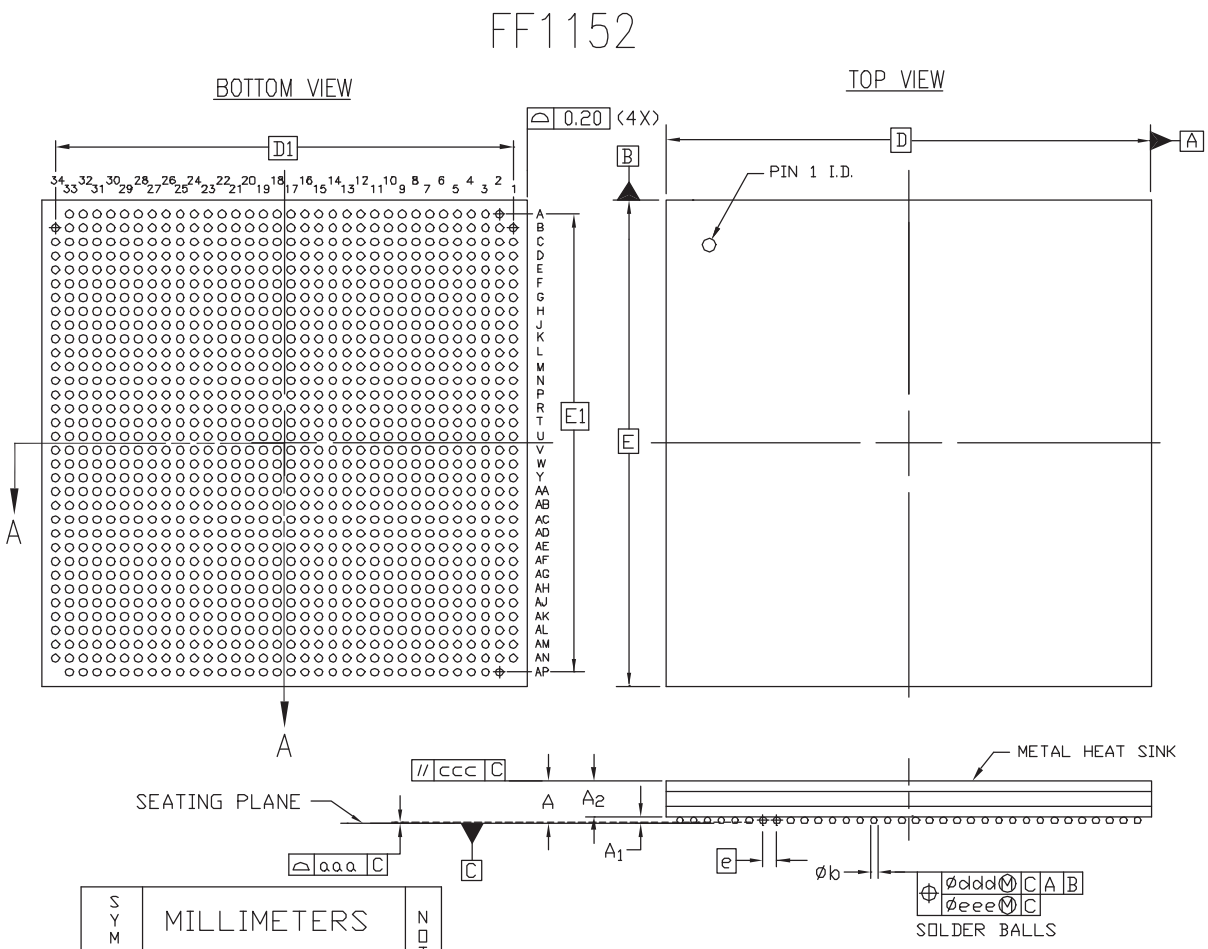
Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	VCCINT	Y13				
N/A	VCCINT	Y22				
N/A	VCCINT	AA13				
N/A	VCCINT	AA22				
N/A	VCCINT	AB13				
N/A	VCCINT	AB14				
N/A	VCCINT	AB15				
N/A	VCCINT	AB16				
N/A	VCCINT	AB17				
N/A	VCCINT	AB18				
N/A	VCCINT	AB19				
N/A	VCCINT	AB20				
N/A	VCCINT	AB21				
N/A	VCCINT	AB22				
N/A	VCCINT	AC12				
N/A	VCCINT	AC23				
N/A	VCCINT	AD11				
N/A	VCCINT	AD24				
N/A	VCCAUX	C3				
N/A	VCCAUX	C4				
N/A	VCCAUX	C17				
N/A	VCCAUX	C18				
N/A	VCCAUX	C31				
N/A	VCCAUX	C32				
N/A	VCCAUX	D3				
N/A	VCCAUX	D32				
N/A	VCCAUX	U1				
N/A	VCCAUX	V1				
N/A	VCCAUX	U34				
N/A	VCCAUX	V34				
N/A	VCCAUX	AL3				
N/A	VCCAUX	AL32				
N/A	VCCAUX	AM3				
N/A	VCCAUX	AM4				
N/A	VCCAUX	AM17				
N/A	VCCAUX	AM18				
N/A	VCCAUX	AM31				
N/A	VCCAUX	AM32				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	AG8				
N/A	GND	AG12				
N/A	GND	AG15				
N/A	GND	AG20				
N/A	GND	AG23				
N/A	GND	AG27				
N/A	GND	J34				
N/A	GND	AH7				
N/A	GND	AH28				
N/A	GND	AJ6				
N/A	GND	AJ29				
N/A	GND	AK5				
N/A	GND	AK12				
N/A	GND	AK23				
N/A	GND	AK30				
N/A	GND	AL4				
N/A	GND	AL31				
N/A	GND	AM1				
N/A	GND	AM2				
N/A	GND	AM10				
N/A	GND	AM16				
N/A	GND	AM19				
N/A	GND	AM25				
N/A	GND	AM33				
N/A	GND	AM34				
N/A	GND	AN1				
N/A	GND	AN34				

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	---	3.20	3.40	
A_1	0.40	0.50	0.60	
A_2	---	---	2.80	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	---	---	0.20	
ccc	---	---	0.35	
ddd	---	---	0.30	
eee	---	---	0.10	
M	34			2

NOTES:
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

Figure 6: **FF1152 Flip-Chip Fine-Pitch BGA Package Specifications**

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
7	IO_L32P_7	N24		
7	IO_L32N_7	N25		
7	IO_L31P_7	G33		
7	IO_L31N_7	G34		
7	IO_L30P_7	H31		
7	IO_L30N_7	G32		
7	IO_L29P_7	N27		
7	IO_L29N_7	M28		
7	IO_L28P_7	G28		
7	IO_L28N_7/VREF_7	G29		
7	IO_L27P_7	F33		
7	IO_L27N_7	F34		
7	IO_L26P_7	M26		
7	IO_L26N_7	M27		
7	IO_L25P_7	F31		
7	IO_L25N_7	F32		
7	IO_L24P_7	F30		
7	IO_L24N_7	G30		
7	IO_L23P_7	L25		
7	IO_L23N_7	M25		
7	IO_L22P_7	F27		
7	IO_L22N_7/VREF_7	F28		
7	IO_L21P_7	E29		
7	IO_L21N_7	F29		
7	IO_L20P_7	L28		
7	IO_L20N_7	K28		
7	IO_L19P_7	D33		
7	IO_L19N_7	D34		
7	IO_L18P_7	D32		
7	IO_L18N_7	E32		
7	IO_L17P_7	K26		
7	IO_L17N_7	L26		
7	IO_L16P_7	D31		
7	IO_L16N_7/VREF_7	E31		
7	IO_L15P_7	D29		
7	IO_L15N_7	D30		
7	IO_L14P_7	J28		
7	IO_L14N_7	J29		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L11N_2	L9		
2	IO_L11P_2	M10		
2	IO_L12N_2	H4		
2	IO_L12P_2	J5		
2	IO_L13N_2	J1		
2	IO_L13P_2	J2		
2	IO_L14N_2	M8		
2	IO_L14P_2	N9		
2	IO_L15N_2	K6		
2	IO_L15P_2	K7		
2	IO_L16N_2/VREF_2	K4		
2	IO_L16P_2	K5		
2	IO_L17N_2	P10		
2	IO_L17P_2	N10		
2	IO_L18N_2	K3		
2	IO_L18P_2	J3		
2	IO_L19N_2	K1		
2	IO_L19P_2	K2		
2	IO_L20N_2	M11		
2	IO_L20P_2	N11		
2	IO_L21N_2	L7		
2	IO_L21P_2	L8		
2	IO_L22N_2/VREF_2	L5		
2	IO_L22P_2	L6		
2	IO_L23N_2	P8		
2	IO_L23P_2	P9		
2	IO_L24N_2	L3		
2	IO_L24P_2	L4		
2	IO_L25N_2	L1		
2	IO_L25P_2	L2		
2	IO_L26N_2	P11		
2	IO_L26P_2	P12		
2	IO_L27N_2	M6		
2	IO_L27P_2	M7		
2	IO_L28N_2/VREF_2	M2		
2	IO_L28P_2	M3		
2	IO_L29N_2	R9		
2	IO_L29P_2	R10		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L30N_2	N6		
2	IO_L30P_2	N7		
2	IO_L31N_2	M4		
2	IO_L31P_2	N5		
2	IO_L32N_2	R11		
2	IO_L32P_2	R12		
2	IO_L33N_2	N1		
2	IO_L33P_2	N2		
2	IO_L34N_2/VREF_2	P6		
2	IO_L34P_2	P7		
2	IO_L35N_2	R13		
2	IO_L35P_2	T13		
2	IO_L36N_2	P4		
2	IO_L36P_2	P5		
2	IO_L37N_2	P3		
2	IO_L37P_2	N3		
2	IO_L38N_2	T10		
2	IO_L38P_2	T11		
2	IO_L39N_2	P1		
2	IO_L39P_2	P2		
2	IO_L40N_2/VREF_2	R7		
2	IO_L40P_2	R8		
2	IO_L41N_2	T12		
2	IO_L41P_2	U12		
2	IO_L42N_2	R5		
2	IO_L42P_2	R6		
2	IO_L43N_2	R3		
2	IO_L43P_2	R4		
2	IO_L44N_2	U8		
2	IO_L44P_2	T8		
2	IO_L45N_2	R1		
2	IO_L45P_2	R2		
2	IO_L46N_2/VREF_2	T6		
2	IO_L46P_2	T7		
2	IO_L47N_2	U9		
2	IO_L47P_2	U10		
2	IO_L48N_2	T2		
2	IO_L48P_2	T3		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L04P_6	AR33		
6	IO_L04N_6	AP33		
6	IO_L05P_6	AM32		
6	IO_L05N_6	AL31		
6	IO_L06P_6	AT34		
6	IO_L06N_6	AR34		
6	IO_L73P_6	AU35	NC	
6	IO_L73N_6	AT35	NC	
6	IO_L75P_6	AT38	NC	
6	IO_L75N_6/VREF_6	AT39	NC	
6	IO_L76P_6	AR37	NC	
6	IO_L76N_6	AR38	NC	
6	IO_L78P_6	AP38	NC	
6	IO_L78N_6	AP39	NC	
6	IO_L79P_6	AP36	NC	
6	IO_L79N_6	AP37	NC	
6	IO_L81P_6	AP35	NC	
6	IO_L81N_6/VREF_6	AN35	NC	
6	IO_L82P_6	AN38	NC	
6	IO_L82N_6	AN39	NC	
6	IO_L84P_6	AN36	NC	
6	IO_L84N_6	AN37	NC	
6	IO_L07P_6	AN33		
6	IO_L07N_6	AN34		
6	IO_L08P_6	AK31		
6	IO_L08N_6	AK32		
6	IO_L09P_6	AM37		
6	IO_L09N_6/VREF_6	AM38		
6	IO_L10P_6	AM36		
6	IO_L10N_6	AL35		
6	IO_L11P_6	AJ31		
6	IO_L11N_6	AH30		
6	IO_L12P_6	AM33		
6	IO_L12N_6	AM34		
6	IO_L13P_6	AL38		
6	IO_L13N_6	AL39		
6	IO_L14P_6	AH29		
6	IO_L14N_6	AG29		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
0	IO_L49P_0		G26		
0	IO_L50_0/No_Pair		D27		
0	IO_L53_0/No_Pair		D26		
0	IO_L54N_0		K25		
0	IO_L54P_0		L25		
0	IO_L55N_0		G25		
0	IO_L55P_0		H25		
0	IO_L56N_0		E26		
0	IO_L56P_0		E25		
0	IO_L57N_0		C25		
0	IO_L57P_0/VREF_0		C26		
0	IO_L58N_0		L24		
0	IO_L58P_0		M24		
0	IO_L59N_0		J24		
0	IO_L59P_0		K24		
0	IO_L60N_0		G24		
0	IO_L60P_0		H24		
0	IO_L64N_0		E24		
0	IO_L64P_0		F24		
0	IO_L65N_0		D24		
0	IO_L65P_0		C24		
0	IO_L66N_0		M22		
0	IO_L66P_0/VREF_0		M23		
0	IO_L67N_0		K23		
0	IO_L67P_0		L23		
0	IO_L68N_0		J23		
0	IO_L68P_0		H23		
0	IO_L69N_0		E23		
0	IO_L69P_0/VREF_0		F23		
0	IO_L73N_0		C23		
0	IO_L73P_0		D23		
0	IO_L74N_0/GCLK7P		K22		
0	IO_L74P_0/GCLK6S		J22		
0	IO_L75N_0/GCLK5P	BREFCLKN	F22		
0	IO_L75P_0/GCLK4S	BREFCLKP	G22		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L52P_6	AF40	
6	IO_L52N_6	AF41	
6	IO_L53P_6	AC36	
6	IO_L53N_6	AC37	
6	IO_L54P_6	AE41	
6	IO_L54N_6	AE42	
6	IO_L55P_6	AE40	
6	IO_L55N_6	AD40	
6	IO_L56P_6	AC31	
6	IO_L56N_6	AC32	
6	IO_L57P_6	AE38	
6	IO_L57N_6/VREF_6	AE39	
6	IO_L58P_6	AD41	
6	IO_L58N_6	AD42	
6	IO_L59P_6	AB35	
6	IO_L59N_6	AB36	
6	IO_L60P_6	AD37	
6	IO_L60N_6	AD38	
6	IO_L85P_6	AC40	
6	IO_L85N_6	AC41	
6	IO_L86P_6	AB33	
6	IO_L86N_6	AB34	
6	IO_L87P_6	AC39	
6	IO_L87N_6/VREF_6	AB39	
6	IO_L88P_6	AB40	
6	IO_L88N_6	AB41	
6	IO_L89P_6	AB31	
6	IO_L89N_6	AB32	
6	IO_L90P_6	AB37	
6	IO_L90N_6	AB38	
7	IO_L90P_7	AA40	
7	IO_L90N_7	AA41	
7	IO_L89P_7	AA35	
7	IO_L89N_7	AA36	
7	IO_L88P_7	Y39	
7	IO_L88N_7/VREF_7	AA39	