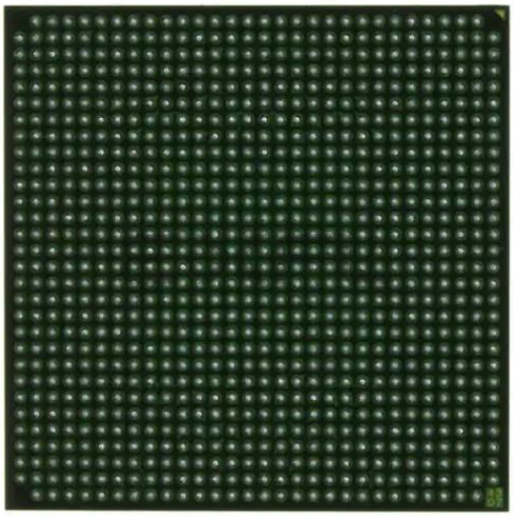


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2320
Number of Logic Elements/Cells	20880
Total RAM Bits	1622016
Number of I/O	556
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp20-5ff896i

Output Swing and Emphasis

The output swing and emphasis levels are fully programmable. Each is controlled via attributes at configuration, and can be modified via the PMA attribute programming bus.

The programmable output swing control can adjust the differential peak-to-peak output level between 200 mV and 1600 mV.

With emphasis, the differential voltage swing is boosted to create a stronger rising or falling waveform. This method compensates for high frequency loss in the transmission media that would otherwise limit the magnitude of this waveform. Lossy transmission lines cause the dissipation of electrical energy. This emphasis technique extends the distance that signals can be driven down lossy line media and increases the signal-to-noise ratio at the receiver.

Emphasis can be described from two perspectives, additive to the smaller voltage (V_{SM}) (pre-emphasis) or subtractive from the larger voltage (V_{LG}) (de-emphasis). The resulting benefits in compensating for channel loss are identical. It is simply a relative way of specifying the effect at the transmitter.

The equations for calculating pre-emphasis as a percentage and dB are as follows:

$$\text{Pre-Emphasis}_{\%} = ((V_{LG}-V_{SM}) / V_{SM}) \times 100$$
$$\text{Pre-Emphasis}_{dB} = 20 \log(V_{LG}/V_{SM})$$

The equations for calculating de-emphasis as a percentage and dB are as follows:

$$\text{De-Emphasis}_{\%} = (V_{LG} - V_{SM}) / V_{LG}) \times 100$$
$$\text{De-Emphasis}_{dB} = 20 \log(V_{SM}/V_{LG})$$

The pre-emphasis amount can be programmed in discrete steps between 0% and 500%. The de-emphasis amount can be programmed in discrete steps between 0% and 83%.

Serializer

The serializer multiplies the reference frequency provided on REFCLK by 10, 16, 20, 32, or 40, depending on the operation mode. The multiplication of the clock is achieved by using an embedded PLL.

Data is converted from parallel to serial format and transmitted on the TXP and TXN differential outputs. The electrical connection of TXP and TXN can be interchanged through configuration. This option can be controlled by an input (TXPOLARITY) at the FPGA transmitter interface.

Deserializer

Synchronous serial data reception is facilitated by a clock and data recovery (CDR) circuit. This circuit uses a fully monolithic Phase Lock Loop (PLL), which does not require any external components. The CDR circuit extracts both phase and frequency from the incoming data stream.

The derived clock, RXRECCLK, is generated and locked to as long as it remains within the specified component range. This clock is presented to the FPGA fabric at $^1/_{10}$, $^1/_{16}$, $^1/_{20}$, $^1/_{32}$, or $^1/_{40}$ the incoming data rate depending on the operating mode.

A sufficient number of transitions must be present in the data stream for CDR to work properly. The CDR circuit is guaranteed to work with 8B/10B and 64B/66B encoding. Further, CDR requires approximately 5,000 transitions upon power-up to guarantee locking to the incoming data rate. Once lock is achieved, up to 75 missing transitions can be tolerated before lock to the incoming data stream is lost.

Another feature of CDR is its ability to accept an external precision reference clock, REFCLK, which either acts to clock incoming data or to assist in synchronizing the derived RXRECCLK.

For further clarity, the TXUSRCLK is used to clock data from the FPGA fabric to the TX FIFO. The FIFO depth accounts for the slight phase difference between these two clocks. If the clocks are locked in frequency, then the FIFO acts much like a pass-through buffer.

The receiver can be configured to reverse the RXP and RXN inputs. This can be useful in the event that printed circuit board traces have been reversed.

Receiver Lock Control

The CDR circuits will lock to the reference clock automatically if the data is not present. For proper operation, the frequency of the reference clock must be within ±100 ppm of the nominal frequency.

During normal operation, the receiver PLL automatically locks to incoming data (when present) or to the local reference clock (when data is not present). This is the default configuration for all primitives. This function can be overridden via the PMARXLOCKSEL port

When receive PLL lock is forced to the local reference, phase information from the incoming data stream is ignored. Data continues to be sampled, but synchronous to the local reference rather than relative to edges in the data stream.

Receive Equalization

In addition to transmit emphasis, the RocketIO X MGT provides a programmable active receive equalization feature to further compensate the effects of channel attenuation at high frequencies.

By adjusting RXFER, the right amount of equalization can be added to reverse the signal degradation caused by a printed circuit board, a backplane, or a line/switch card. RXFER can be set through software configuration or the PMA Attribute Bus.

Receiver Termination

On-chip termination is provided at the receiver, eliminating the need for external termination. The receiver termination supply (V_{TRX}) is the center tap of differential termination to

Table 5: **Clock Ratios for Various Data Widths**

Fabric Data Width	Frequency Ratio of USRCLK:USRCLK2
1-byte	1:2 (1)
2-byte	1:1
4-byte	2:1 (1)

Notes:
1. Each edge of slower clock must align with falling edge of faster clock.

FPGA Transmit Interface

The FPGA can send either one, two, or four characters of data to the transmitter. Each character can be either 8 bits or 10 bits wide. If 8-bit data is applied, the additional inputs become control signals for the 8B/10B encoder. When the 8B/10B encoder is bypassed, the 10-bit character order is generated as follows:

TXCHARDISPMODE[0] (first bit transmitted)
TXCHARDISPVAL[0]
TXDATA[7:0] (last bit transmitted is TXDATA[0])

Disparity Control

The 8B/10B encoder is initialized with a negative running disparity. Unique control allows forcing the current running disparity state.

TXRUNDISP signals its current running disparity. This may be useful in those cases where there is a need to manipulate the initial running disparity value.

Bits TXCHARDISPMODE and TXCHARDISPVAL control the generation of running disparity before each byte.

For example, the transceiver can generate the sequence

```
K28.5+ K28.5+ K28.5- K28.5-
```

or

```
K28.5- K28.5- K28.5+ K28.5+
```

by specifying inverted running disparity for the second and fourth bytes.

Transmit FIFO

Proper operation of the circuit is only possible if the FPGA clock (TXUSRCLK) is frequency-locked to the reference clock (REFCLK). Phase variations up to one clock cycle are allowable. The FIFO has a depth of four. Overflow or underflow conditions are detected and signaled at the interface. Bypassing of this FIFO is programmable.

8B/10B Encoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

A bypassable 8B/10B encoder is included. The encoder uses the same 256 data characters and 12 control characters used by Gigabit Ethernet, Fibre Channel, and InfiniBand.

The encoder accepts 8 bits of data along with a K-character signal for a total of 9 bits per character applied, and generates a 10 bit character for transmission. If the K-character signal is High, the data is encoded into one of the twelve possible K-characters available in the 8B/10B code. If the K-character input is Low, the 8 bits are encoded as standard data. If the K-character input is High, and a user applies other than one of the twelve possible combinations, TXKERR indicates the error.

8B/10B Decoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

An optional 8B/10B decoder is included. A programmable option allows the decoder to be bypassed. When the 8B/10B decoder is bypassed, the 10-bit character order is, for example,

RXCHARISK[0] (first bit received)
RXRUNDISP[0]
RXDATA[7:0] (last bit received is RXDATA[0])

The decoder uses the same table that is used for Gigabit Ethernet, Fibre Channel, and InfiniBand. In addition to decoding all data and K-characters, the decoder has several extra features. The decoder separately detects both “disparity errors” and “out-of-band” errors. A disparity error is the reception of 10-bit character that exists within the 8B/10B table but has an incorrect disparity. An out-of-band error is the reception of a 10-bit character that does not exist within the 8B/10B table. It is possible to obtain an out-of-band error without having a disparity error. The proper disparity is always computed for both legal and illegal characters. The current running disparity is available at the RXRUNDISP signal.

The 8B/10B decoder performs a unique operation if out-of-band data is detected. If out-of-band data is detected, the decoder signals the error and passes the illegal 10-bits through and places them on the outputs. This can be used for debugging purposes if desired.

The decoder also signals the reception of one of the 12 valid K-characters. In addition, a programmable comma detect is included. The comma detect signal registers a comma on the receipt of any comma+, comma–, or both. Since the comma is defined as a 7-bit character, this includes several out-of-band characters. Another option allows the decoder to detect only the three defined commas (K28.1, K28.5, and K28.7) as comma+, comma–, or both. In total, there are six possible options, three for valid commas and three for "any comma."

Note that all bytes (1, 2, or 4) at the RX FPGA interface each have their own individual 8B/10B indicators (K-character, disparity error, out-of-band error, current running disparity, and comma detect).

Functional Description: FPGA

Input/Output Blocks (IOBs)

Virtex-II Pro I/O blocks (IOBs) are provided in groups of two or four on the perimeter of each device. Each IOB can be used as input and/or output for single-ended I/Os. Two IOBs can be used as a differential pair. A differential pair is always connected to the same switch matrix, as shown in Figure 18.

IOB blocks are designed for high-performance I/O, supporting 22 single-ended standards, as well as differential signaling with LVDS, LDT, bus LVDS, and LVPECL.

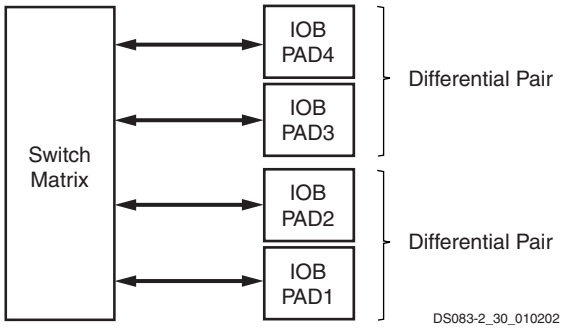


Figure 18: **Virtex-II Pro Input/Output Tile**

Note: Differential I/Os must use the same clock.

Supported I/O Standards

Virtex-II Pro IOB blocks feature SelectIO-Ultra inputs and outputs that support a wide variety of I/O signaling standards. In addition to the internal supply voltage (V_{CCINT} = 1.5V), output driver supply voltage (V_{CCO}) is dependent on the I/O standard (see Table 8 and Table 9). An auxiliary supply voltage (V_{CCAUX} = 2.5V) is required, regardless of the I/O standard used. For exact supply voltage absolute maximum ratings, see Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics.

All of the user IOBs have fixed-clamp diodes to V_{CCO} and to ground. The IOBs are not compatible or compliant with 5V I/O standards (not 5V-tolerant).

Table 10 lists supported I/O standards with Digitally Controlled Impedance. See Digitally Controlled Impedance (DCI), page 31.

Table 8: **Supported Single-Ended I/O Standards**

IOSTANDARD Attribute	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL(1)	3.3	3.3	N/R	N/R
LVCMOS33(1)	3.3	3.3	N/R	N/R
LVCMOS25	2.5	2.5	N/R	N/R
LVCMOS18	1.8	1.8	N/R	N/R
LVCMOS15	1.5	1.5	N/R	N/R
PCI33_3	Note (2)	Note (2)	N/R	N/R
PCI66_3	Note (2)	Note (2)	N/R	N/R
PCIX	Note (2)	Note (2)	N/R	N/R
GTL	Note (3)	Note (3)	0.8	1.2
GTLP	Note (3)	Note (3)	1.0	1.5
HSTL_I	1.5	N/R	0.75	0.75
HSTL_II	1.5	N/R	0.75	0.75
HSTL_III	1.5	N/R	0.9	1.5
HSTL_IV	1.5	N/R	0.9	1.5
HSTL_I_18	1.8	N/R	0.9	0.9
HSTL_II_18	1.8	N/R	0.9	0.9
HSTL_III _18	1.8	N/R	1.1	1.8
HSTL_IV_18	1.8	N/R	1.1	1.8
SSTL2_I	2.5	N/R	1.25	1.25
SSTL2_II	2.5	N/R	1.25	1.25
SSTL18_I (4)	1.8	N/R	0.9	0.9
SSTL18_II	1.8	N/R	0.9	0.9

Notes:
1. Refer to **XAPP659** for more details on interfacing to these 3.3V standards.
2. For PCI and PCI-X standards, refer to **XAPP653**.
3. V_{CCO} of GTL or GTLP should not be lower than the termination voltage or the voltage seen at the I/O pad. *Example:* If the pin High level is 1.5V, connect V_{CCO} to 1.5V.
4. SSTL18_I is not a JEDEC-supported standard.
5. N/R = no requirement.

Configurable Logic Blocks (CLBs)

The Virtex-II Pro configurable logic blocks (CLB) are organized in an array and are used to build combinatorial and synchronous logic designs. Each CLB element is tied to a switch matrix to access the general routing matrix, as shown in Figure 32. A CLB element comprises 4 similar slices, with fast local feedback within the CLB. The four slices are split in two columns of two slices with two independent carry logic chains and one common shift chain.

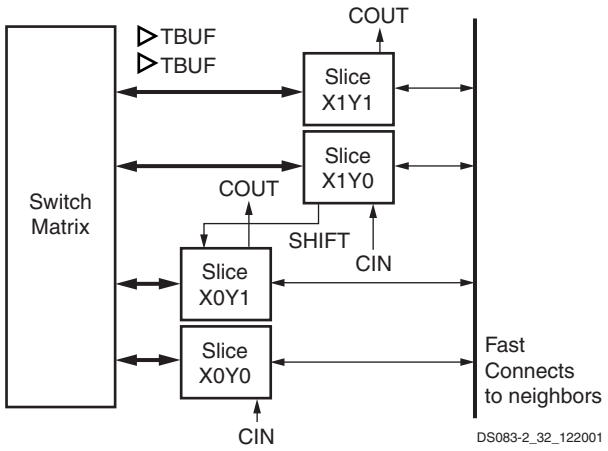


Figure 32: **Virtex-II Pro CLB Element**

Slice Description

Each slice includes two 4-input function generators, carry logic, arithmetic logic gates, wide function multiplexers and two storage elements. As shown in Figure 33, each 4-input function generator is programmable as a 4-input LUT, 16 bits of distributed SelectRAM+ memory, or a 16-bit variable-tap shift register element.

The output from the function generator in each slice drives both the slice output and the D input of the storage element. Figure 34 shows a more detailed view of a single slice.

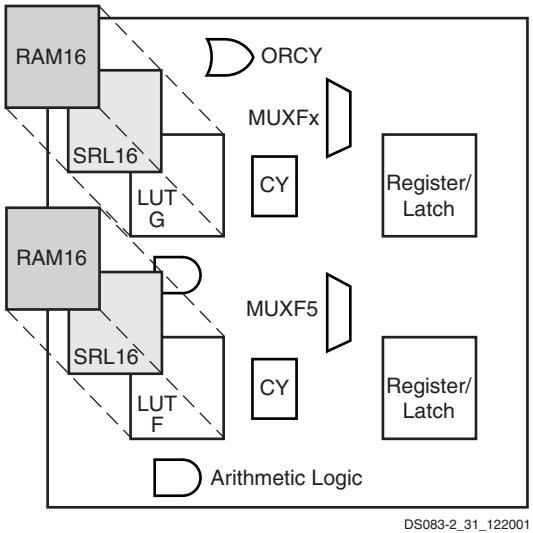


Figure 33: **Virtex-II Pro Slice Configuration**

Configurations

Look-Up Table

Virtex-II Pro function generators are implemented as 4-input look-up tables (LUTs). Four independent inputs are provided to each of the two function generators in a slice (F and G). These function generators are each capable of implementing any arbitrarily defined boolean function of four inputs. The propagation delay is therefore independent of the function implemented. Signals from the function generators can exit the slice (X or Y output), can input the XOR dedicated gate (see arithmetic logic), or input the carry-logic multiplexer (see fast look-ahead carry logic), or feed the D input of the storage element, or go to the MUXF5 (not shown in Figure 34).

In addition to the basic LUTs, the Virtex-II Pro slice contains logic (MUXF5 and MUXFX multiplexers) that combines function generators to provide any function of five, six, seven, or eight inputs. The MUXFX is either MUXF6, MUXF7, or MUXF8 according to the slice considered in the CLB. Selected functions up to nine inputs (MUXF5 multiplexer) can be implemented in one slice. The MUXFX can also be a MUXF6, MUXF7, or MUXF8 multiplexer to map any function of six, seven, or eight inputs and selected wide logic functions.

Register/Latch

The storage elements in a Virtex-II Pro slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D input can be directly driven by the X or Y output via the DX or DY input, or by the slice inputs bypassing the function generators via the BX or BY input. The clock enable signal (CE) is active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

In addition to clock (CK) and clock enable (CE) signals, each slice has set and reset signals (SR and BY slice inputs). SR forces the storage element into the state specified by the attribute SRHIGH or SRLOW. SRHIGH forces a logic 1 when SR is asserted. SRLOW forces a logic 0. When SR is used, an optional second input (BY) forces the storage element into the opposite state via the REV pin. The reset condition is predominant over the set condition. (See Figure 35.)

The initial state after configuration or global initial state is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1. For each slice, set and reset can be set to be synchronous or asynchronous. Virtex-II Pro devices also have the ability to set INIT0 and INIT1 independent of SRHIGH and SRLOW.

The control signals clock (CLK), clock enable (CE) and set/reset (SR) are common to both storage elements in one slice. All of the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Virtex-II Pro Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM

Table 53: **Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM**

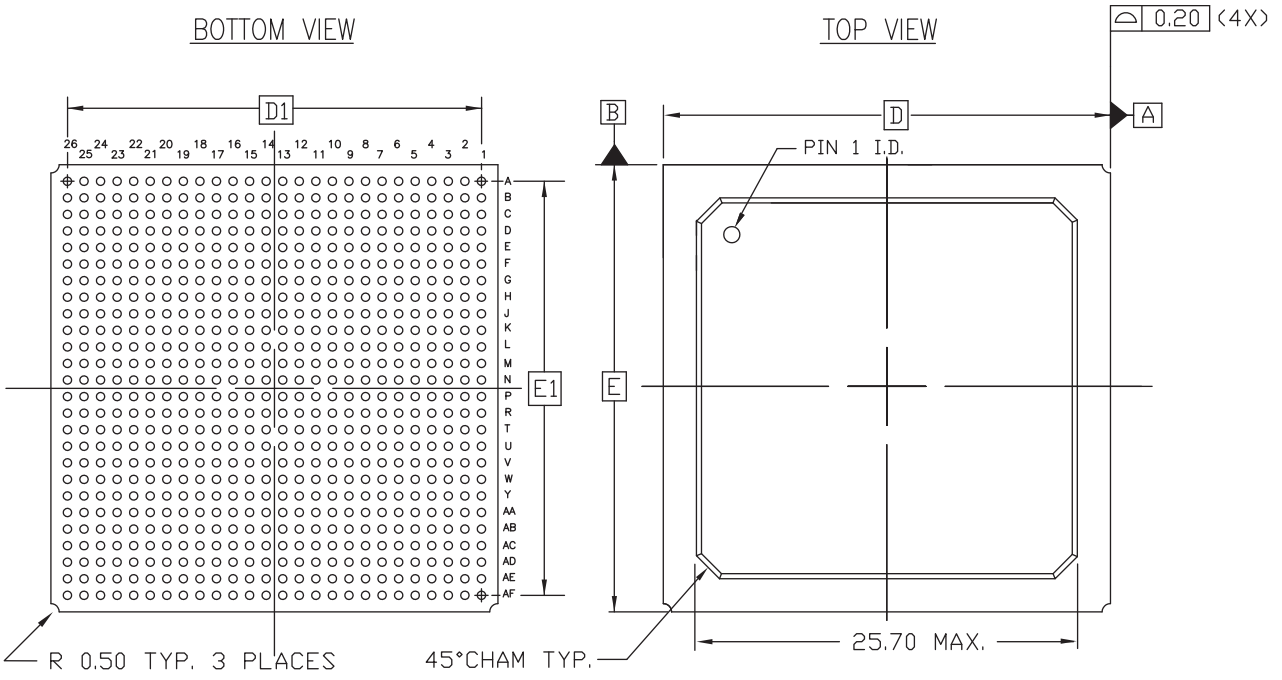
			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
LVCMOS25 Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 28.						
Global Clock and OFF with DCM	$T_{ICKOFDCM}$	XC2VP2	1.55	1.59	1.62	ns
		XC2VP4	1.58	1.61	1.65	ns
		XC2VP7	1.63	1.68	1.72	ns
		XC2VP20	1.68	1.74	1.79	ns
		XC2VPX20	1.68	1.74	1.79	ns
		XC2VP30	1.68	1.75	1.80	ns
		XC2VP40	1.71	1.86	1.92	ns
		XC2VP50	1.80	2.00	2.07	ns
		XC2VP70	1.87	2.07	2.24	ns
		XC2VPX70	1.87	2.07	2.24	ns
		XC2VP100	N/A	2.38	2.45	ns

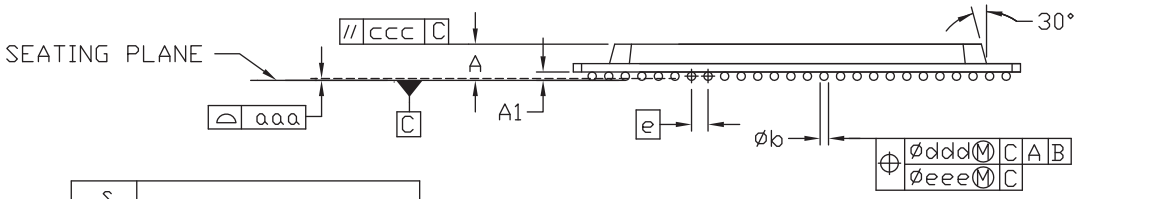
Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 6. For other I/O standards, see Table 40.
3. DCM output jitter is already included in the timing calculation.

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
2	IO_L56N_2	J21	NC		
2	IO_L56P_2	J22	NC		
2	IO_L58N_2/VREF_2	J18	NC		
2	IO_L58P_2	K18	NC		
2	IO_L60N_2	K19	NC		
2	IO_L60P_2	K20	NC		
2	IO_L85N_2	K21			
2	IO_L85P_2	K22			
2	IO_L86N_2	K17			
2	IO_L86P_2	L17			
2	IO_L88N_2/VREF_2	L18			
2	IO_L88P_2	L19			
2	IO_L90N_2	L20			
2	IO_L90P_2	L21			
3	IO_L90N_3	M21			
3	IO_L90P_3	M20			
3	IO_L89N_3	M19			
3	IO_L89P_3	M18			
3	IO_L87N_3/VREF_3	M17			
3	IO_L87P_3	N17			
3	IO_L85N_3	N22			
3	IO_L85P_3	N21			
3	IO_L60N_3	N20	NC		
3	IO_L60P_3	N19	NC		
3	IO_L59N_3	N18	NC		
3	IO_L59P_3	P18	NC		
3	IO_L57N_3/VREF_3	P22	NC		
3	IO_L57P_3	P21	NC		
3	IO_L55N_3	P20	NC		
3	IO_L55P_3	P19	NC		
3	IO_L54N_3	P17	NC		
3	IO_L54P_3	R18	NC		
3	IO_L53N_3	R22	NC		
3	IO_L53P_3	R21	NC		
3	IO_L51N_3/VREF_3	R20	NC		
3	IO_L51P_3	R19	NC		

FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)





FG676 - 63/37 (Sn/Pb) Solder Balls
FGG676 - Sn/Ag/Cu Solder Balls

SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.02	2.23	2.44
A_1	0.40	0.50	0.60
D/E	27.00 BSC		
D_1/E_1	25.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa	~	~	0.20
ccc	~	~	0.35
ddd	~	~	0.30
eee	~	~	0.10
M	26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

ds083_4_03_053111

Figure 3: **FG676/FGG676 Fine-Pitch BGA Package Specifications**

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	VCCINT	U16			
N/A	VCCINT	U18			
N/A	VCCINT	V10			
N/A	VCCINT	V17			
N/A	VCCINT	V18			
N/A	VCCINT	W19			
N/A	VCCAUX	B2			
N/A	VCCAUX	N1			
N/A	VCCAUX	P1			
N/A	VCCAUX	A13			
N/A	VCCAUX	A14			
N/A	VCCAUX	AE2			
N/A	VCCAUX	B25			
N/A	VCCAUX	N26			
N/A	VCCAUX	P26			
N/A	VCCAUX	AE25			
N/A	VCCAUX	AF13			
N/A	VCCAUX	AF14			
N/A	GND	C3			
N/A	GND	D4			
N/A	GND	E5			
N/A	GND	F6			
N/A	GND	G7			
N/A	GND	Y7			
N/A	GND	AA6			
N/A	GND	AB5			
N/A	GND	AC4			
N/A	GND	AD3			
N/A	GND	C24			
N/A	GND	D23			
N/A	GND	E22			
N/A	GND	F21			
N/A	GND	G20			
N/A	GND	K10			
N/A	GND	K12			
N/A	GND	K13			
N/A	GND	K14			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
0	IO_L43P_0	E22				
0	IO_L44N_0	E25				
0	IO_L44P_0	D25				
0	IO_L45N_0	H21				
0	IO_L45P_0/VREF_0	G21				
0	IO_L46N_0	D22				
0	IO_L46P_0	D23				
0	IO_L47N_0	D24				
0	IO_L47P_0	C24				
0	IO_L48N_0	K20				
0	IO_L48P_0	J20				
0	IO_L49N_0	F21				
0	IO_L49P_0	E21				
0	IO_L50_0/No_Pair	C21				
0	IO_L53_0/No_Pair	C22				
0	IO_L54N_0	L19				
0	IO_L54P_0	K19				
0	IO_L55N_0	G20				
0	IO_L55P_0	F20				
0	IO_L56N_0	D21				
0	IO_L56P_0	D20				
0	IO_L57N_0	J19				
0	IO_L57P_0/VREF_0	H19				
0	IO_L67N_0	G19				
0	IO_L67P_0	F19				
0	IO_L68N_0	E19				
0	IO_L68P_0	D19				
0	IO_L69N_0	L18				
0	IO_L69P_0/VREF_0	K18				
0	IO_L73N_0	G18				
0	IO_L73P_0	F18				
0	IO_L74N_0/GCLK7P	E18				
0	IO_L74P_0/GCLK6S	D18				
0	IO_L75N_0/GCLK5P	J18				
0	IO_L75P_0/GCLK4S	H18				
1	IO_L75N_1/GCLK3P	H17				
1	IO_L75P_1/GCLK2S	J17				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	AF34				
N/A	GND	B34				
N/A	GND	C1				
N/A	GND	C2				
N/A	GND	C10				
N/A	GND	C16				
N/A	GND	C19				
N/A	GND	C25				
N/A	GND	C33				
N/A	GND	C34				
N/A	GND	D4				
N/A	GND	D31				
N/A	GND	E5				
N/A	GND	E12				
N/A	GND	E23				
N/A	GND	E30				
N/A	GND	F6				
N/A	GND	F29				
N/A	GND	G7				
N/A	GND	G28				
N/A	GND	B1				
N/A	GND	H8				
N/A	GND	H12				
N/A	GND	H15				
N/A	GND	H20				
N/A	GND	J1				
N/A	GND	H27				
N/A	GND	AF1				
N/A	GND	K3				
N/A	GND	K32				
N/A	GND	M5				
N/A	GND	M8				
N/A	GND	M27				
N/A	GND	M30				
N/A	GND	P14				
N/A	GND	P15				
N/A	GND	P16				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L43N_0	B22		
0	IO_L43P_0	C22		
0	IO_L44N_0	K21		
0	IO_L44P_0	L21		
0	IO_L45N_0	G21		
0	IO_L45P_0/VREF_0	H21		
0	IO_L46N_0	E21		
0	IO_L46P_0	F21		
0	IO_L47N_0	K20		
0	IO_L47P_0	L20		
0	IO_L48N_0	C21		
0	IO_L48P_0	D21		
0	IO_L49N_0	A21		
0	IO_L49P_0	B21		
0	IO_L50_0/No_Pair	G20		
0	IO_L53_0/No_Pair	H19		
0	IO_L54N_0	E20		
0	IO_L54P_0	F20		
0	IO_L55N_0	C20		
0	IO_L55P_0	D19		
0	IO_L56N_0	K19		
0	IO_L56P_0	L19		
0	IO_L57N_0	A20		
0	IO_L57P_0/VREF_0	B20		
0	IO_L66N_0	F19	NC	
0	IO_L66P_0/VREF_0	G19	NC	
0	IO_L67N_0	B19		
0	IO_L67P_0	C19		
0	IO_L68N_0	H18		
0	IO_L68P_0	J18		
0	IO_L69N_0	F18		
0	IO_L69P_0/VREF_0	G18		
0	IO_L73N_0	D18		
0	IO_L73P_0	E18		
0	IO_L74N_0/GCLK7P	K18		
0	IO_L74P_0/GCLK6S	L18		
0	IO_L75N_0/GCLK5P	B18		
0	IO_L75P_0/GCLK4S	C18		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
2	IO_L59P_2	U11		
2	IO_L60N_2	R1		
2	IO_L60P_2	R2		
2	IO_L85N_2	T3		
2	IO_L85P_2	T4		
2	IO_L86N_2	U8		
2	IO_L86P_2	U9		
2	IO_L87N_2	U2		
2	IO_L87P_2	T2		
2	IO_L88N_2/VREF_2	U4		
2	IO_L88P_2	U5		
2	IO_L89N_2	U6		
2	IO_L89P_2	U7		
2	IO_L90N_2	V3		
2	IO_L90P_2	U3		
3	IO_L90N_3	V6		
3	IO_L90P_3	V7		
3	IO_L89N_3	V10		
3	IO_L89P_3	V11		
3	IO_L88N_3	V4		
3	IO_L88P_3	V5		
3	IO_L87N_3/VREF_3	V2		
3	IO_L87P_3	W2		
3	IO_L86N_3	V8		
3	IO_L86P_3	V9		
3	IO_L85N_3	W6		
3	IO_L85P_3	W7		
3	IO_L60N_3	W3		
3	IO_L60P_3	W4		
3	IO_L59N_3	W10		
3	IO_L59P_3	W11		
3	IO_L58N_3	Y5		
3	IO_L58P_3	Y6		
3	IO_L57N_3/VREF_3	Y3		
3	IO_L57P_3	AA3		
3	IO_L56N_3	W8		
3	IO_L56P_3	Y7		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	GND	AF30		
N/A	GND	AB30		
N/A	GND	W30		
N/A	GND	T30		
N/A	GND	N30		
N/A	GND	J30		
N/A	GND	E30		
N/A	GND	A30		
N/A	GND	AP26		
N/A	GND	AK26		
N/A	GND	AB26		
N/A	GND	W26		
N/A	GND	T26		
N/A	GND	N26		
N/A	GND	E26		
N/A	GND	A26		
N/A	GND	AE25		
N/A	GND	K25		
N/A	GND	AP22		
N/A	GND	AK22		
N/A	GND	AF22		
N/A	GND	J22		
N/A	GND	E22		
N/A	GND	A22		
N/A	GND	Y21		
N/A	GND	W21		
N/A	GND	V21		
N/A	GND	U21		
N/A	GND	T21		
N/A	GND	R21		
N/A	GND	AA20		
N/A	GND	Y20		
N/A	GND	W20		
N/A	GND	V20		
N/A	GND	U20		
N/A	GND	T20		
N/A	GND	R20		
N/A	GND	P20		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L11N_2	L9		
2	IO_L11P_2	M10		
2	IO_L12N_2	H4		
2	IO_L12P_2	J5		
2	IO_L13N_2	J1		
2	IO_L13P_2	J2		
2	IO_L14N_2	M8		
2	IO_L14P_2	N9		
2	IO_L15N_2	K6		
2	IO_L15P_2	K7		
2	IO_L16N_2/VREF_2	K4		
2	IO_L16P_2	K5		
2	IO_L17N_2	P10		
2	IO_L17P_2	N10		
2	IO_L18N_2	K3		
2	IO_L18P_2	J3		
2	IO_L19N_2	K1		
2	IO_L19P_2	K2		
2	IO_L20N_2	M11		
2	IO_L20P_2	N11		
2	IO_L21N_2	L7		
2	IO_L21P_2	L8		
2	IO_L22N_2/VREF_2	L5		
2	IO_L22P_2	L6		
2	IO_L23N_2	P8		
2	IO_L23P_2	P9		
2	IO_L24N_2	L3		
2	IO_L24P_2	L4		
2	IO_L25N_2	L1		
2	IO_L25P_2	L2		
2	IO_L26N_2	P11		
2	IO_L26P_2	P12		
2	IO_L27N_2	M6		
2	IO_L27P_2	M7		
2	IO_L28N_2/VREF_2	M2		
2	IO_L28P_2	M3		
2	IO_L29N_2	R9		
2	IO_L29P_2	R10		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
4	IO_L38P_4	AH16		
4	IO_L39N_4	AR14		
4	IO_L39P_4	AP14		
4	IO_L43N_4	AU14		
4	IO_L43P_4	AT14		
4	IO_L44N_4	AH17		
4	IO_L44P_4	AG17		
4	IO_L45N_4	AN15		
4	IO_L45P_4/VREF_4	AM15		
4	IO_L46N_4	AR15		
4	IO_L46P_4	AP15		
4	IO_L47N_4	AK16		
4	IO_L47P_4	AJ17		
4	IO_L48N_4	AU15		
4	IO_L48P_4	AT15		
4	IO_L49N_4	AM16		
4	IO_L49P_4	AL16		
4	IO_L50_4/No_Pair	AM17		
4	IO_L53_4/No_Pair	AL17		
4	IO_L54N_4	AP16		
4	IO_L54P_4	AN17		
4	IO_L55N_4	AR16		
4	IO_L55P_4	AR17		
4	IO_L56N_4	AH18		
4	IO_L56P_4	AG18		
4	IO_L57N_4	AU17		
4	IO_L57P_4/VREF_4	AT17		
4	IO_L58N_4	AM18		
4	IO_L58P_4	AL18		
4	IO_L59N_4	AK18		
4	IO_L59P_4	AJ18		
4	IO_L60N_4	AP18		
4	IO_L60P_4	AN18		
4	IO_L64N_4	AT18		
4	IO_L64P_4	AR18		
4	IO_L65N_4	AH19		
4	IO_L65P_4	AG19		
4	IO_L66N_4	AU18		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L86P_2		Y12		
2	IO_L87N_2		AA9		
2	IO_L87P_2		AA10		
2	IO_L88N_2/VREF_2		AA6		
2	IO_L88P_2		AA7		
2	IO_L89N_2		AA12		
2	IO_L89P_2		AB12		
2	IO_L90N_2		AA3		
2	IO_L90P_2		AA4		
3	IO_L90N_3		AB3		
3	IO_L90P_3		AB4		
3	IO_L89N_3		AB6		
3	IO_L89P_3		AB7		
3	IO_L88N_3		AB9		
3	IO_L88P_3		AB10		
3	IO_L87N_3/VREF_3		AC3		
3	IO_L87P_3		AC4		
3	IO_L86N_3		AC11		
3	IO_L86P_3		AC12		
3	IO_L85N_3		AC6		
3	IO_L85P_3		AC7		
3	IO_L60N_3		AC9		
3	IO_L60P_3		AC10		
3	IO_L59N_3		AD9		
3	IO_L59P_3		AD10		
3	IO_L58N_3		AD1		
3	IO_L58P_3		AD2		
3	IO_L57N_3/VREF_3		AD3		
3	IO_L57P_3		AD4		
3	IO_L56N_3		AD11		
3	IO_L56P_3		AD12		
3	IO_L55N_3		AD5		
3	IO_L55P_3		AD6		
3	IO_L54N_3		AD7		
3	IO_L54P_3		AD8		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L16N_6		AM42		
6	IO_L17P_6		AL33		
6	IO_L17N_6		AL34		
6	IO_L18P_6		AL35		
6	IO_L18N_6		AL36		
6	IO_L19P_6		AL38		
6	IO_L19N_6		AL39		
6	IO_L20P_6		AL31		
6	IO_L20N_6		AL32		
6	IO_L21P_6		AL40		
6	IO_L21N_6/VREF_6		AL41		
6	IO_L22P_6		AK35		
6	IO_L22N_6		AK36		
6	IO_L23P_6		AK33		
6	IO_L23N_6		AK34		
6	IO_L24P_6		AK37		
6	IO_L24N_6		AK38		
6	IO_L25P_6		AK39		
6	IO_L25N_6		AK40		
6	IO_L26P_6		AK31		
6	IO_L26N_6		AK32		
6	IO_L27P_6		AK41		
6	IO_L27N_6/VREF_6		AK42		
6	IO_L28P_6		AJ35		
6	IO_L28N_6		AJ36		
6	IO_L29P_6		AJ33		
6	IO_L29N_6		AJ34		
6	IO_L30P_6		AJ37		
6	IO_L30N_6		AJ38		
6	IO_L31P_6		AJ41		
6	IO_L31N_6		AJ42		
6	IO_L32P_6		AJ31		
6	IO_L32N_6		AJ32		
6	IO_L33P_6		AH33		
6	IO_L33N_6/VREF_6		AH34		
6	IO_L34P_6		AH37		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		E22		
N/A	GND		E21		
N/A	GND		E5		
N/A	GND		D39		
N/A	GND		D32		
N/A	GND		D28		
N/A	GND		D15		
N/A	GND		D11		
N/A	GND		D4		
N/A	GND		C42		
N/A	GND		C41		
N/A	GND		C40		
N/A	GND		C3		
N/A	GND		C2		
N/A	GND		C1		
N/A	GND		B42		
N/A	GND		B1		
N/A	GND		N14		
N/A	GND		N29		
N/A	GND		AK14		
N/A	GND		AK29		
N/A	GND		P13		
N/A	GND		P30		
N/A	GND		AJ13		
N/A	GND		AJ30		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L22N_2/VREF_2	L4	
2	IO_L22P_2	L5	
2	IO_L23N_2	T8	
2	IO_L23P_2	T9	
2	IO_L24N_2	L3	
2	IO_L24P_2	K3	
2	IO_L25N_2	L1	
2	IO_L25P_2	L2	
2	IO_L26N_2	U12	
2	IO_L26P_2	V12	
2	IO_L27N_2	M7	
2	IO_L27P_2	L6	
2	IO_L28N_2/VREF_2	M5	
2	IO_L28P_2	M6	
2	IO_L29N_2	U10	
2	IO_L29P_2	U11	
2	IO_L30N_2	M3	
2	IO_L30P_2	M4	
2	IO_L31N_2	N6	
2	IO_L31P_2	N7	
2	IO_L32N_2	U7	
2	IO_L32P_2	U8	
2	IO_L33N_2	N3	
2	IO_L33P_2	N4	
2	IO_L34N_2/VREF_2	N2	
2	IO_L34P_2	M2	
2	IO_L35N_2	V10	
2	IO_L35P_2	V11	
2	IO_L36N_2	P6	
2	IO_L36P_2	P7	
2	IO_L37N_2	P1	
2	IO_L37P_2	P2	
2	IO_L38N_2	V8	
2	IO_L38P_2	V9	
2	IO_L39N_2	R6	
2	IO_L39P_2	P5	
2	IO_L40N_2/VREF_2	R4	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L45N_7	T36	
7	IO_L44P_7	W32	
7	IO_L44N_7	W33	
7	IO_L43P_7	R41	
7	IO_L43N_7	R42	
7	IO_L42P_7	P40	
7	IO_L42N_7	R40	
7	IO_L41P_7	V36	
7	IO_L41N_7	V37	
7	IO_L40P_7	R38	
7	IO_L40N_7/VREF_7	R39	
7	IO_L39P_7	P38	
7	IO_L39N_7	R37	
7	IO_L38P_7	V34	
7	IO_L38N_7	V35	
7	IO_L37P_7	P41	
7	IO_L37N_7	P42	
7	IO_L36P_7	P36	
7	IO_L36N_7	P37	
7	IO_L35P_7	V32	
7	IO_L35N_7	V33	
7	IO_L34P_7	M41	
7	IO_L34N_7/VREF_7	N41	
7	IO_L33P_7	N39	
7	IO_L33N_7	N40	
7	IO_L32P_7	U35	
7	IO_L32N_7	U36	
7	IO_L31P_7	N36	
7	IO_L31N_7	N37	
7	IO_L30P_7	M39	
7	IO_L30N_7	M40	
7	IO_L29P_7	U32	
7	IO_L29N_7	U33	
7	IO_L28P_7	M37	
7	IO_L28N_7/VREF_7	M38	
7	IO_L27P_7	L37	
7	IO_L27N_7	M36	