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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2320
Number of Logic Elements/Cells	20880
Total RAM Bits	1622016
Number of I/O	564
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp20-5ffg1152i

Virtex-II Pro / Virtex-II Pro X Device/Package Combinations and Maximum I/Os

Offerings include ball grid array (BGA) packages with 1.0 mm pitch. In addition to traditional wire-bond interconnect (FG/FGG packages), flip-chip interconnect (FF packages) is used in some of the BGA offerings. Flip-chip interconnect construction supports more I/Os than are possible in wire-bond versions of similar packages, providing a high pin count and excellent power dissipation.

The device/package combination table (Table 3) details the maximum number of user I/Os and RocketIO / RocketIO X MGTs for each device and package using wire-bond or flip-chip technology.

The FF1148 and FF1696 packages have no RocketIO transceivers bonded out. Extra SelectIO-Ultra resources occupy available pins in these packages, resulting in a higher user I/O count. These packages are available for the XC2VP40, XC2VP50, and XC2VP100 devices only.

The I/Os per package count includes all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, and RSVD), VBATT, and the RocketIO / RocketIO X transceiver pins.

Table 3: Virtex-II Pro Device/Package Combinations and Maximum Number of Available I/Os

Package ⁽¹⁾	FG256/ FGG256	FG456/ FGG456	FG676	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Size (mm)	17 x 17	23 x 23	26 x 26	27 x 27	31 x 31	35 x 35	35 x 35	40 x 40	42.5 x 42.5	42.5 x 42.5
XC2VP2	140 / 4	156 / 4		204 / 4						
XC2VP4	140 / 4	248 / 4		348 / 4						
XC2VP7		248 / 8		396 / 8	396 / 8					
XC2VP20			404 / 8		556 / 8	564 / 8				
XC2VPX20					552 / 8 ⁽²⁾					
XC2VP30			416 / 8		556 / 8	644 / 8				
XC2VP40			416 / 8			692 / 12	804 / 0 ⁽³⁾			
XC2VP50						692 / 16	812 / 0 ⁽³⁾	852 / 16		
XC2VP70								964 / 16	996 / 20	
XC2VPX70									992 / 20 ⁽²⁾	
XC2VP100									1,040 / 20	1,164 / 0 ⁽³⁾

Notes:

- Wirebond packages FG256, FG456, and FG676 are also available in Pb-free versions FGG256, FGG456, and FGG676. See [Virtex-II Pro Ordering Examples](#) for details on how to order.
- Virtex-II Pro X device is equipped with RocketIO X transceiver cores.
- The RocketIO transceivers in devices in the FF1148 and FF1696 packages are not bonded out to the package pins.

Maximum Performance

Maximum performance of the RocketIO / RocketIO X transceiver and the PowerPC processor block varies, depending on package style and speed grade. See Table 4 for details. [Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics](#) contains the rest of the FPGA fabric performance parameters.

Table 4: Maximum RocketIO / RocketIO X Transceiver and Processor Block Performance

Device	Speed Grade			Units
	-7 ⁽¹⁾	-6	-5	
RocketIO X Transceiver FlipChip (FF)	N/A	6.25 ⁽³⁾	4.25 ⁽³⁾	Gb/s
RocketIO Transceiver FlipChip (FF)	3.125	3.125	2.0	Gb/s
RocketIO Transceiver Wirebond (FG)	2.5	2.5	2.0	Gb/s
PowerPC Processor Block	400 ⁽²⁾	350 ⁽²⁾	300	MHz

Notes:

- 7 speed grade devices are not available in Industrial grade.
- IMPORTANT!** When CPMC405CLOCK runs at speeds greater than 350 MHz in -7 Commercial grade dual-processor devices, or greater than 300 MHz in -6 Industrial grade dual-processor devices, users must implement the technology presented in [XAPP755](#), "PowerPC 405 Clock Macro for -7(C) and -6(I) Speed Grade Dual-Processor Devices." Refer to Table 1 to identify dual-processor devices.
- XC2VPX70 is only available at fixed 4.25 Gb/s baud rate.

Receiver Buffer

The receiver includes buffers (FIFOs) in the datapath. This section gives the reasons for including the buffers and outlines their operation.

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

The receiver uses an *elastic buffer*, where "elastic" refers to the ability to modify the read pointer for clock correction and channel bonding.

Comma Detection

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indication is given at the receiver interface. The realignment indicator is a distinct output.

The transceiver continuously monitors the data for the presence of the 10-bit character(s). Upon each occurrence of a 10-bit character, the data is checked for word alignment. If comma detect is disabled, the data is not aligned to any particular pattern. The programmable option allows a user to align data on comma+, comma-, both, or a unique user-defined and programmed sequence.

Clock Correction

RXRECCLK (the recovered clock) reflects the data rate of the incoming data. RXUSRCLK defines the rate at which the FPGA fabric consumes the data. Ideally, these rates are identical. However, since the clocks typically have different sources, one of the clocks will be faster than the other. The receiver buffer accommodates this difference between the clock rates. See [Figure 12](#).

Nominally, the buffer is always half full. This is shown in the top buffer, [Figure 12](#), where the shaded area represents buffered data not yet read. Received data is inserted via the write pointer under control of RXRECCLK. The FPGA fabric reads data via the read pointer under control of RXUSRCLK. The half full/half empty condition of the buffer gives a cushion for the differing clock rates. This operation continues indefinitely, regardless of whether or not "meaningful" data is being received. When there is no meaningful data to be received, the incoming data will consist of IDLE characters or other padding.

If RXUSRCLK is faster than RXRECCLK, the buffer becomes more empty over time. The clock correction logic

corrects for this by decrementing the read pointer to reread a repeatable byte sequence. This is shown in the middle buffer, [Figure 12](#), where the solid read pointer decrements to the value represented by the dashed pointer.

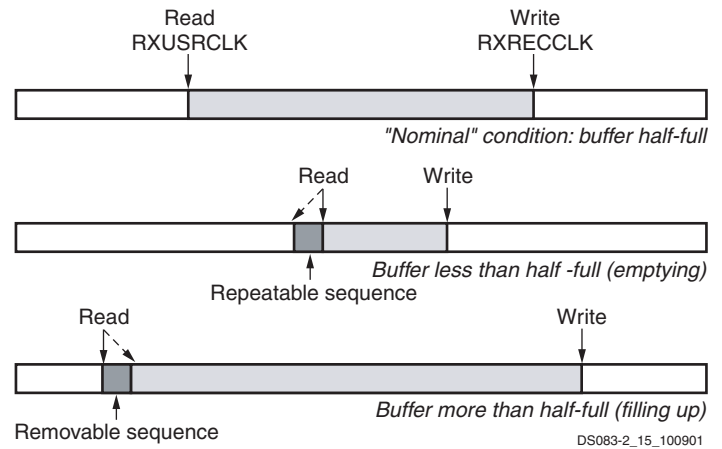


Figure 12: Clock Correction in Receiver

By decrementing the read pointer instead of incrementing it in the usual fashion, the buffer is partially refilled. The transceiver design will repeat a single repeatable byte sequence when necessary to refill a buffer. If the byte sequence length is greater than one, and if attribute CLK_COR_REPEAT_WAIT is 0, then the transceiver may repeat the same sequence multiple times until the buffer is refilled to the desired extent.

Similarly, if RXUSRCLK is slower than RXRECCLK, the buffer will fill up over time. The clock correction logic corrects for this by incrementing the read pointer to skip over a removable byte sequence that need not appear in the final FPGA fabric byte stream. This is shown in the bottom buffer, [Figure 12](#), where the solid read pointer increments to the value represented by the dashed pointer. This accelerates the emptying of the buffer, preventing its overflow. The transceiver design will skip a single byte sequence when necessary to partially empty a buffer. If attribute CLK_COR_REPEAT_WAIT is 0, the transceiver may also skip two consecutive removable byte sequences in one step to further empty the buffer when necessary.

These operations require the clock correction logic to recognize a byte sequence that can be freely repeated or omitted in the incoming data stream. This sequence is generally an IDLE sequence, or other sequence comprised of special values that occur in the gaps separating packets of meaningful data. These gaps are required to occur sufficiently often to facilitate the timely execution of clock correction.

Channel Bonding

Some gigabit I/O standards such as Infiniband specify the use of multiple transceivers in parallel for even higher data rates. Words of data are split into bytes, with each byte sent over a separate channel (transceiver). See [Figure 13](#).

Table 6: FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L06N_6	V1			
6	IO_L43P_6	U4	NC		
6	IO_L43N_6	U3	NC		
6	IO_L45P_6	U2	NC		
6	IO_L45N_6/VREF_6	U1	NC		
6	IO_L47P_6	U5	NC		
6	IO_L47N_6	T5	NC		
6	IO_L48P_6	T4	NC		
6	IO_L48N_6	T3	NC		
6	IO_L49P_6	T2	NC		
6	IO_L49N_6	T1	NC		
6	IO_L51P_6	R4	NC		
6	IO_L51N_6/VREF_6	R3	NC		
6	IO_L53P_6	R2	NC		
6	IO_L53N_6	R1	NC		
6	IO_L54P_6	R5	NC		
6	IO_L54N_6	P6	NC		
6	IO_L55P_6	P4	NC		
6	IO_L55N_6	P3	NC		
6	IO_L57P_6	P2	NC		
6	IO_L57N_6/VREF_6	P1	NC		
6	IO_L59P_6	P5	NC		
6	IO_L59N_6	N5	NC		
6	IO_L60P_6	N4	NC		
6	IO_L60N_6	N3	NC		
6	IO_L85P_6	N2			
6	IO_L85N_6	N1			
6	IO_L87P_6	N6			
6	IO_L87N_6/VREF_6	M6			
6	IO_L89P_6	M5			
6	IO_L89N_6	M4			
6	IO_L90P_6	M3			
6	IO_L90N_6	M2			
7	IO_L90P_7	L2			
7	IO_L90N_7	L3			
7	IO_L88P_7	L4			

Table 6: FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	VCCO_0	G9			
0	VCCO_0	G11			
0	VCCO_0	G10			
0	VCCO_0	F8			
0	VCCO_0	F7			
1	VCCO_1	G14			
1	VCCO_1	G13			
1	VCCO_1	G12			
1	VCCO_1	F16			
1	VCCO_1	F15			
2	VCCO_2	L16			
2	VCCO_2	K16			
2	VCCO_2	J16			
2	VCCO_2	H17			
2	VCCO_2	G17			
3	VCCO_3	T17			
3	VCCO_3	R17			
3	VCCO_3	P16			
3	VCCO_3	N16			
3	VCCO_3	M16			
4	VCCO_4	U16			
4	VCCO_4	U15			
4	VCCO_4	T14			
4	VCCO_4	T13			
4	VCCO_4	T12			
5	VCCO_5	U8			
5	VCCO_5	U7			
5	VCCO_5	T9			
5	VCCO_5	T11			
5	VCCO_5	T10			
6	VCCO_6	T6			
6	VCCO_6	R6			
6	VCCO_6	P7			
6	VCCO_6	N7			
6	VCCO_6	M7			
7	VCCO_7	L7			

Table 6: FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	GND	L11			
N/A	GND	L10			
N/A	GND	K9			
N/A	GND	K14			
N/A	GND	K13			
N/A	GND	K12			
N/A	GND	K11			
N/A	GND	K10			
N/A	GND	J9			
N/A	GND	J14			
N/A	GND	J13			
N/A	GND	J12			
N/A	GND	J11			
N/A	GND	J10			
N/A	GND	E5			
N/A	GND	E18			
N/A	GND	D4			
N/A	GND	D19			
N/A	GND	C3			
N/A	GND	C20			
N/A	GND	AB22			
N/A	GND	AB12			
N/A	GND	AB1			
N/A	GND	A22			
N/A	GND	A11			
N/A	GND	A1			

Notes:

1. See Table 4 for an explanation of the signals available on this pin.

Table 8: FF672 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L01P_6/VRN_6	AF24			
6	IO_L01N_6/VRP_6	AE24			
6	IO_L02P_6	AD23			
6	IO_L02N_6	AC24			
6	IO_L03P_6	AE26			
6	IO_L03N_6/VREF_6	AF25			
6	IO_L04P_6	AD25			
6	IO_L04N_6	AD26			
6	IO_L05P_6	AC25			
6	IO_L05N_6	AC26			
6	IO_L06P_6	AB23			
6	IO_L06N_6	AB24			
6	IO_L39P_6	AB25	NC	NC	NC
6	IO_L39N_6/VREF_6	AB26	NC	NC	NC
6	IO_L41P_6	AA22	NC	NC	NC
6	IO_L41N_6	AA23	NC	NC	NC
6	IO_L42P_6	AA24	NC	NC	NC
6	IO_L42N_6	AA25	NC	NC	NC
6	IO_L43P_6	Y21	NC		
6	IO_L43N_6	Y22	NC		
6	IO_L44P_6	Y23	NC		
6	IO_L44N_6	Y24	NC		
6	IO_L45P_6	AA26	NC		
6	IO_L45N_6/VREF_6	Y26	NC		
6	IO_L46P_6	W21	NC		
6	IO_L46N_6	W22	NC		
6	IO_L47P_6	W23	NC		
6	IO_L47N_6	W24	NC		
6	IO_L48P_6	W25	NC		
6	IO_L48N_6	W26	NC		
6	IO_L49P_6	V20	NC		
6	IO_L49N_6	V21	NC		
6	IO_L50P_6	V22	NC		
6	IO_L50N_6	V23	NC		
6	IO_L51P_6	V24	NC		
6	IO_L51N_6/VREF_6	V25	NC		
6	IO_L52P_6	U21	NC		

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
3	IO_L39P_3		AE2	NC		
3	IO_L38N_3		AA7	NC		
3	IO_L38P_3		AA8	NC		
3	IO_L37N_3		AD3	NC		
3	IO_L37P_3		AD4	NC		
3	IO_L36N_3		AF1	NC		
3	IO_L36P_3		AF2	NC		
3	IO_L35N_3		AC5	NC		
3	IO_L35P_3		AC6	NC		
3	IO_L34N_3		AF3	NC		
3	IO_L34P_3		AF4	NC		
3	IO_L33N_3/VREF_3		AE3	NC		
3	IO_L33P_3		AE4	NC		
3	IO_L32N_3		AB7	NC		
3	IO_L32P_3		AB8	NC		
3	IO_L31N_3		AE5	NC		
3	IO_L31P_3		AF6	NC		
3	IO_L06N_3		AG1			
3	IO_L06P_3		AG2			
3	IO_L05N_3		AD5			
3	IO_L05P_3		AD6			
3	IO_L04N_3		AG3			
3	IO_L04P_3		AH4			
3	IO_L03N_3/VREF_3		AH1			
3	IO_L03P_3		AH2			
3	IO_L02N_3		AG5			
3	IO_L02P_3		AH5			
3	IO_L01N_3/VRP_3		AJ3			
3	IO_L01P_3/VRN_3		AK3			
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾		AG6			
4	IO_L01P_4/INIT_B		AF7			
4	IO_L02N_4/D0/DIN ⁽¹⁾		AC9			
4	IO_L02P_4/D1		AD9			
4	IO_L03N_4/D2		AG7			
4	IO_L03P_4/D3		AH7			

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
4	IO_L05_4/No_Pair		AD8			
4	IO_L06N_4/VRP_4		AG8			
4	IO_L06P_4/VRN_4		AH8			
4	IO_L07N_4		AC10			
4	IO_L07P_4/VREF_4		AD10			
4	IO_L08N_4		AE7			
4	IO_L08P_4		AE8			
4	IO_L09N_4		AJ8			
4	IO_L09P_4/VREF_4		AK8			
4	IO_L37N_4		AC11			
4	IO_L37P_4		AD11			
4	IO_L38N_4		AF8			
4	IO_L38P_4		AF9			
4	IO_L39N_4		AF10			
4	IO_L39P_4		AG10			
4	IO_L43N_4		AC12			
4	IO_L43P_4		AD12			
4	IO_L44N_4		AE9			
4	IO_L44P_4		AE10			
4	IO_L45N_4		AH9			
4	IO_L45P_4/VREF_4		AJ9			
4	IO_L46N_4		AC13	NC		
4	IO_L46P_4		AD13	NC		
4	IO_L47N_4		AE11	NC		
4	IO_L47P_4		AE12	NC		
4	IO_L48N_4		AH10	NC		
4	IO_L48P_4		AH11	NC		
4	IO_L49N_4		AB14	NC		
4	IO_L49P_4		AC14	NC		
4	IO_L50_4/No_Pair		AF11	NC		
4	IO_L53_4/No_Pair		AG11	NC		
4	IO_L54N_4		AJ10	NC		
4	IO_L54P_4		AK10	NC		
4	IO_L56N_4		AF12	NC		
4	IO_L56P_4		AF13	NC		
4	IO_L57N_4		AG13	NC		

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
6	IO_L86P_6		T23			
6	IO_L86N_6		T24			
6	IO_L87P_6		U28			
6	IO_L87N_6/VREF_6		U29			
6	IO_L88P_6		T27			
6	IO_L88N_6		T28			
6	IO_L89P_6		T25			
6	IO_L89N_6		T26			
6	IO_L90P_6		V30			
6	IO_L90N_6		U30			
7	IO_L90P_7		R28			
7	IO_L90N_7		R27			
7	IO_L89P_7		R26			
7	IO_L89N_7		R25			
7	IO_L88P_7		T29			
7	IO_L88N_7/VREF_7		R29			
7	IO_L87P_7		P27			
7	IO_L87N_7		P26			
7	IO_L86P_7		R24			
7	IO_L86N_7		R23			
7	IO_L85P_7		P29			
7	IO_L85N_7		P28			
7	IO_L60P_7		N28			
7	IO_L60N_7		N27			
7	IO_L59P_7		P24			
7	IO_L59N_7		P23			
7	IO_L58P_7		P30			
7	IO_L58N_7/VREF_7		N30			
7	IO_L57P_7		M28			
7	IO_L57N_7		M27			
7	IO_L56P_7		R22			
7	IO_L56N_7		P22			
7	IO_L55P_7		N29			
7	IO_L55N_7		M29			
7	IO_L54P_7		L27			

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
1	IO_L74N_1/GCLK1P	D17				
1	IO_L74P_1/GCLK0S	E17				
1	IO_L73N_1	F17				
1	IO_L73P_1	G17				
1	IO_L69N_1/VREF_1	K17				
1	IO_L69P_1	L17				
1	IO_L68N_1	D16				
1	IO_L68P_1	E16				
1	IO_L67N_1	F16				
1	IO_L67P_1	G16				
1	IO_L57N_1/VREF_1	H16				
1	IO_L57P_1	J16				
1	IO_L56N_1	D15				
1	IO_L56P_1	D14				
1	IO_L55N_1	F15				
1	IO_L55P_1	G15				
1	IO_L54N_1	K16				
1	IO_L54P_1	L16				
1	IO_L53_1/No_Pair	C13				
1	IO_L50_1/No_Pair	C14				
1	IO_L49N_1	E14				
1	IO_L49P_1	F14				
1	IO_L48N_1	J15				
1	IO_L48P_1	K15				
1	IO_L47N_1	C11				
1	IO_L47P_1	D11				
1	IO_L46N_1	D12				
1	IO_L46P_1	D13				
1	IO_L45N_1/VREF_1	G14				
1	IO_L45P_1	H14				
1	IO_L44N_1	D10				
1	IO_L44P_1	E10				
1	IO_L43N_1	E13				
1	IO_L43P_1	F13				
1	IO_L39N_1	J14				
1	IO_L39P_1	K14				
1	IO_L38N_1	C9				
1	IO_L38P_1	D9				

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
4	IO_L27P_4/VREF_4	AL10	NC	NC		
4	IO_L37N_4	AE13				
4	IO_L37P_4	AF13				
4	IO_L38N_4	AG13				
4	IO_L38P_4	AH13				
4	IO_L39N_4	AJ11				
4	IO_L39P_4	AK11				
4	IO_L43N_4	AE14				
4	IO_L43P_4	AF14				
4	IO_L44N_4	AJ13				
4	IO_L44P_4	AK13				
4	IO_L45N_4	AL11				
4	IO_L45P_4/VREF_4	AM11				
4	IO_L46N_4	AE15				
4	IO_L46P_4	AF15				
4	IO_L47N_4	AG14				
4	IO_L47P_4	AH14				
4	IO_L48N_4	AL13				
4	IO_L48P_4	AL12				
4	IO_L49N_4	AD16				
4	IO_L49P_4	AE16				
4	IO_L50_4/No_Pair	AJ14				
4	IO_L53_4/No_Pair	AK14				
4	IO_L54N_4	AM14				
4	IO_L54P_4	AM13				
4	IO_L55N_4	AF16				
4	IO_L55P_4	AG16				
4	IO_L56N_4	AH15				
4	IO_L56P_4	AJ15				
4	IO_L57N_4	AL14				
4	IO_L57P_4/VREF_4	AL15				
4	IO_L67N_4	AD17				
4	IO_L67P_4	AE17				
4	IO_L68N_4	AH16				
4	IO_L68P_4	AJ16				
4	IO_L69N_4	AK16				
4	IO_L69P_4/VREF_4	AL16				
4	IO_L73N_4	AF17				

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
6	IO_L01P_6/VRN_6	AJ30				
6	IO_L01N_6/VRP_6	AJ31				
6	IO_L02P_6	AJ27				
6	IO_L02N_6	AJ28				
6	IO_L03P_6	AK31				
6	IO_L03N_6/VREF_6	AK32				
6	IO_L04P_6	AH29				
6	IO_L04N_6	AH30				
6	IO_L05P_6	AH27				
6	IO_L05N_6	AG28				
6	IO_L06P_6	AL33				
6	IO_L06N_6	AL34				
6	IO_L15P_6	AG29	NC			
6	IO_L15N_6/VREF_6	AG30	NC			
6	IO_L16P_6	AK33	NC			
6	IO_L16N_6	AK34	NC			
6	IO_L17P_6	AF27	NC			
6	IO_L17N_6	AF28	NC			
6	IO_L18P_6	AJ33	NC			
6	IO_L18N_6	AJ34	NC			
6	IO_L19P_6	AH31	NC			
6	IO_L19N_6	AH32	NC			
6	IO_L20P_6	AD25	NC			
6	IO_L20N_6	AD26	NC			
6	IO_L21P_6	AG31	NC			
6	IO_L21N_6/VREF_6	AG32	NC			
6	IO_L22P_6	AF29	NC			
6	IO_L22N_6	AF30	NC			
6	IO_L23P_6	AE27	NC			
6	IO_L23N_6	AE28	NC			
6	IO_L24P_6	AH33	NC			
6	IO_L24N_6	AH34	NC			
6	IO_L31P_6	AF31				
6	IO_L31N_6	AF32				
6	IO_L32P_6	AC25				
6	IO_L32N_6	AC26				
6	IO_L33P_6	AG33				
6	IO_L33N_6/VREF_6	AG34				

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
7	IO_L43N_7	M31				
7	IO_L42P_7	L32				
7	IO_L42N_7	L31				
7	IO_L41P_7	N28				
7	IO_L41N_7	N27				
7	IO_L40P_7	M33				
7	IO_L40N_7/VREF_7	L33				
7	IO_L39P_7	M29				
7	IO_L39N_7	M28				
7	IO_L38P_7	N26				
7	IO_L38N_7	N25				
7	IO_L37P_7	L34				
7	IO_L37N_7	K34				
7	IO_L36P_7	L30				
7	IO_L36N_7	L29				
7	IO_L35P_7	L28				
7	IO_L35N_7	L27				
7	IO_L34P_7	K33				
7	IO_L34N_7/VREF_7	J33				
7	IO_L33P_7	K31				
7	IO_L33N_7	K30				
7	IO_L32P_7	M26				
7	IO_L32N_7	M25				
7	IO_L31P_7	H34				
7	IO_L31N_7	H33				
7	IO_L24P_7	H32	NC			
7	IO_L24N_7	H31	NC			
7	IO_L23P_7	K28	NC			
7	IO_L23N_7	K27	NC			
7	IO_L22P_7	J32	NC			
7	IO_L22N_7/VREF_7	J31	NC			
7	IO_L21P_7	J30	NC			
7	IO_L21N_7	J29	NC			
7	IO_L20P_7	G34	NC			
7	IO_L20N_7	G33	NC			
7	IO_L19P_7	H30	NC			
7	IO_L19N_7	H29	NC			
7	IO_L18P_7	L26	NC			

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
6	IO_L44N_6	AA28		
6	IO_L45P_6	AC31		
6	IO_L45N_6/VREF_6	AC32		
6	IO_L46P_6	AC29		
6	IO_L46N_6	AC30		
6	IO_L47P_6	AA24		
6	IO_L47N_6	AA25		
6	IO_L48P_6	AB32		
6	IO_L48N_6	AB33		
6	IO_L49P_6	AB28		
6	IO_L49N_6	AB29		
6	IO_L50P_6	AA26		
6	IO_L50N_6	Y26		
6	IO_L51P_6	AA33		
6	IO_L51N_6/VREF_6	AA34		
6	IO_L52P_6	AB31		
6	IO_L52N_6	AA31		
6	IO_L53P_6	Y24		
6	IO_L53N_6	Y25		
6	IO_L54P_6	AA29		
6	IO_L54N_6	AA30		
6	IO_L55P_6	Y33		
6	IO_L55N_6	Y34		
6	IO_L56P_6	Y28		
6	IO_L56N_6	W27		
6	IO_L57P_6	AA32		
6	IO_L57N_6/VREF_6	Y32		
6	IO_L58P_6	Y29		
6	IO_L58N_6	Y30		
6	IO_L59P_6	W24		
6	IO_L59N_6	W25		
6	IO_L60P_6	W31		
6	IO_L60N_6	W32		
6	IO_L85P_6	W28		
6	IO_L85N_6	W29		
6	IO_L86P_6	V26		
6	IO_L86N_6	V27		
6	IO_L87P_6	W33		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L49N_2	U5		
2	IO_L49P_2	U6		
2	IO_L50N_2	U13		
2	IO_L50P_2	V13		
2	IO_L51N_2	U4		
2	IO_L51P_2	T4		
2	IO_L52N_2/VREF_2	U1		
2	IO_L52P_2	U2		
2	IO_L53N_2	V9		
2	IO_L53P_2	V10		
2	IO_L54N_2	V7		
2	IO_L54P_2	V8		
2	IO_L55N_2	V5		
2	IO_L55P_2	V6		
2	IO_L56N_2	V11		
2	IO_L56P_2	V12		
2	IO_L57N_2	V3		
2	IO_L57P_2	V4		
2	IO_L58N_2/VREF_2	V1		
2	IO_L58P_2	V2		
2	IO_L59N_2	W10		
2	IO_L59P_2	W11		
2	IO_L60N_2	W7		
2	IO_L60P_2	W8		
2	IO_L85N_2	W5		
2	IO_L85P_2	W6		
2	IO_L86N_2	W12		
2	IO_L86P_2	W13		
2	IO_L87N_2	W3		
2	IO_L87P_2	W4		
2	IO_L88N_2/VREF_2	Y7		
2	IO_L88P_2	Y8		
2	IO_L89N_2	W9		
2	IO_L89P_2	Y9		
2	IO_L90N_2	Y3		
2	IO_L90P_2	Y4		
3	IO_L90N_3	AA7		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

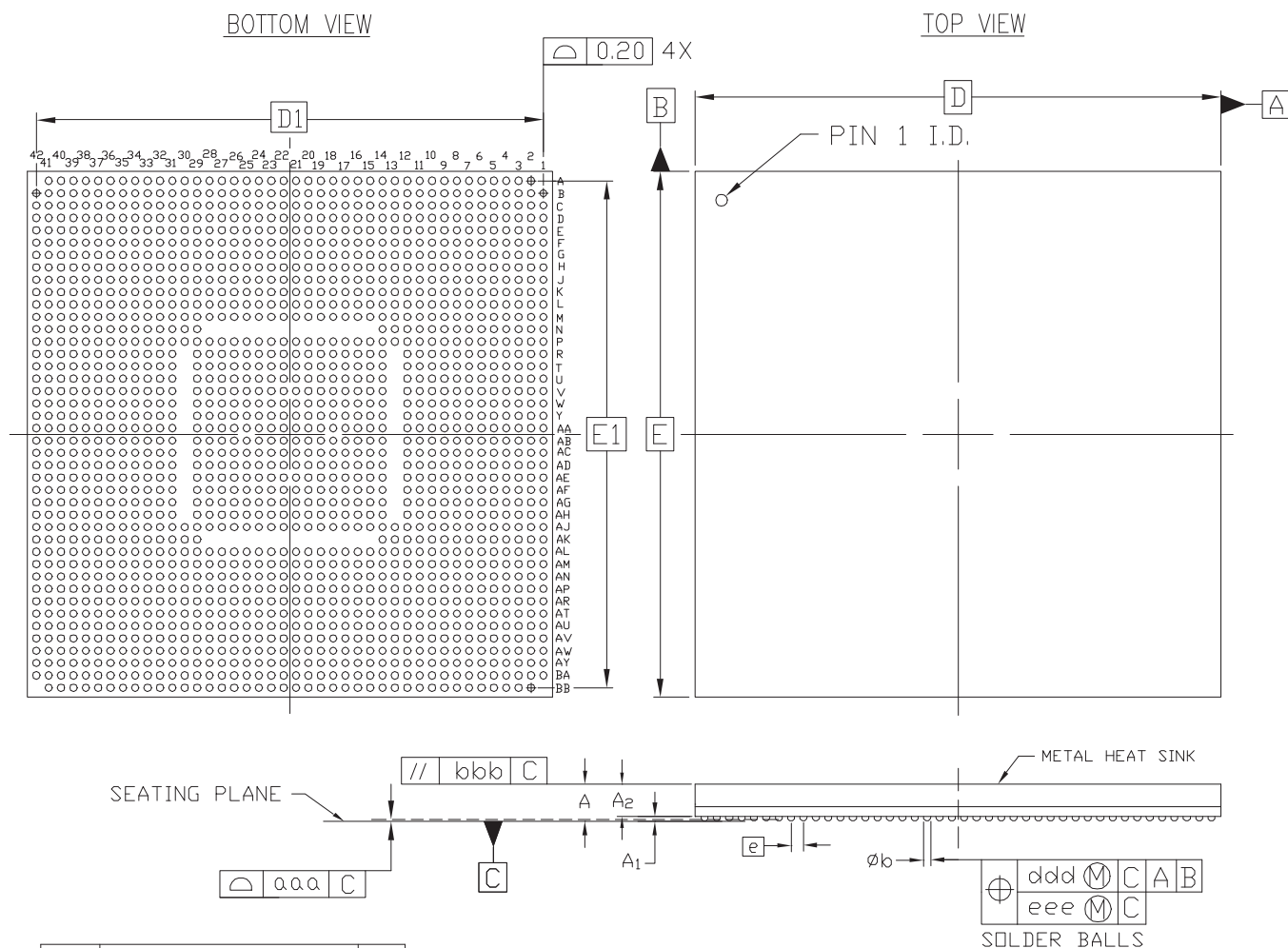
Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L26P_2		N12		
2	IO_L27N_2		P9		
2	IO_L27P_2		P10		
2	IO_L28N_2/VREF_2		P7		
2	IO_L28P_2		P8		
2	IO_L29N_2		P11		
2	IO_L29P_2		P12		
2	IO_L30N_2		P5		
2	IO_L30P_2		P6		
2	IO_L31N_2		P1		
2	IO_L31P_2		P2		
2	IO_L32N_2		R9		
2	IO_L32P_2		R10		
2	IO_L33N_2		R5		
2	IO_L33P_2		R6		
2	IO_L34N_2/VREF_2		P3		
2	IO_L34P_2		R3		
2	IO_L35N_2		R1		
2	IO_L35P_2		R2		
2	IO_L36N_2		R11		
2	IO_L36P_2		R12		
2	IO_L37N_2		T6		
2	IO_L37P_2		T7		
2	IO_L38N_2		T8		
2	IO_L38P_2		R8		
2	IO_L39N_2		T4		
2	IO_L39P_2		T5		
2	IO_L40N_2/VREF_2		T2		
2	IO_L40P_2		T3		
2	IO_L41N_2		T10		
2	IO_L41P_2		T11		
2	IO_L42N_2		U7		
2	IO_L42P_2		U8		
2	IO_L43N_2		U5		
2	IO_L43P_2		U6		
2	IO_L44N_2		U9		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AA5		
N/A	GND		Y41		
N/A	GND		Y26		
N/A	GND		Y25		
N/A	GND		Y24		
N/A	GND		Y23		
N/A	GND		Y22		
N/A	GND		Y21		
N/A	GND		Y20		
N/A	GND		Y19		
N/A	GND		Y18		
N/A	GND		Y17		
N/A	GND		Y2		
N/A	GND		W26		
N/A	GND		W25		
N/A	GND		W24		
N/A	GND		W23		
N/A	GND		W22		
N/A	GND		W21		
N/A	GND		W20		
N/A	GND		W19		
N/A	GND		W18		
N/A	GND		W17		
N/A	GND		V37		
N/A	GND		V34		
N/A	GND		V26		
N/A	GND		V25		
N/A	GND		V24		
N/A	GND		V23		
N/A	GND		V22		
N/A	GND		V21		
N/A	GND		V20		
N/A	GND		V19		
N/A	GND		V18		
N/A	GND		V17		
N/A	GND		V9		

FF1704 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)

FF1704



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.45	2
A ₁	0.40	0.50	0.60	
A ₂			2.85	
D/E	42.50 BASIC			
D ₁ /E ₁	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M		42		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAV-1 (DEPOPULATED)

Figure 9: FF1704 Flip-Chip Fine-Pitch BGA Package Specifications

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L45N_7	T36	
7	IO_L44P_7	W32	
7	IO_L44N_7	W33	
7	IO_L43P_7	R41	
7	IO_L43N_7	R42	
7	IO_L42P_7	P40	
7	IO_L42N_7	R40	
7	IO_L41P_7	V36	
7	IO_L41N_7	V37	
7	IO_L40P_7	R38	
7	IO_L40N_7/VREF_7	R39	
7	IO_L39P_7	P38	
7	IO_L39N_7	R37	
7	IO_L38P_7	V34	
7	IO_L38N_7	V35	
7	IO_L37P_7	P41	
7	IO_L37N_7	P42	
7	IO_L36P_7	P36	
7	IO_L36N_7	P37	
7	IO_L35P_7	V32	
7	IO_L35N_7	V33	
7	IO_L34P_7	M41	
7	IO_L34N_7/VREF_7	N41	
7	IO_L33P_7	N39	
7	IO_L33N_7	N40	
7	IO_L32P_7	U35	
7	IO_L32N_7	U36	
7	IO_L31P_7	N36	
7	IO_L31N_7	N37	
7	IO_L30P_7	M39	
7	IO_L30N_7	M40	
7	IO_L29P_7	U32	
7	IO_L29N_7	U33	
7	IO_L28P_7	M37	
7	IO_L28N_7/VREF_7	M38	
7	IO_L27P_7	L37	
7	IO_L27N_7	M36	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	M2	AM33	
N/A	TCK	K10	
N/A	TDI	M32	
N/A	TDO	M11	
N/A	TMS	L10	
N/A	PWRDWN_B	AP10	
N/A	HSWAP_EN	K33	
N/A	RSVD	J10	
N/A	VBATT	M12	
N/A	DXP	M31	
N/A	DXN	L33	
N/A	VCCINT	AK30	
N/A	VCCINT	N30	
N/A	VCCINT	AJ29	
N/A	VCCINT	P29	
N/A	VCCINT	AJ28	
N/A	VCCINT	AH28	
N/A	VCCINT	R28	
N/A	VCCINT	P28	
N/A	VCCINT	AJ27	
N/A	VCCINT	AH27	
N/A	VCCINT	AG27	
N/A	VCCINT	AF27	
N/A	VCCINT	AE27	
N/A	VCCINT	AD27	
N/A	VCCINT	AC27	
N/A	VCCINT	AB27	
N/A	VCCINT	AA27	
N/A	VCCINT	Y27	
N/A	VCCINT	W27	
N/A	VCCINT	V27	
N/A	VCCINT	U27	
N/A	VCCINT	T27	
N/A	VCCINT	R27	
N/A	VCCINT	P27	
N/A	VCCINT	AH26	