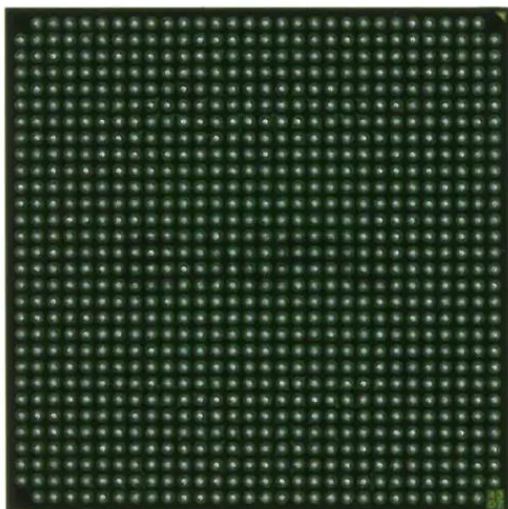




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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2320
Number of Logic Elements/Cells	20880
Total RAM Bits	1622016
Number of I/O	556
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp20-5ffg896i



Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview

DS083 (v5.0) June 21, 2011

Product Specification

Summary of Virtex-II Pro™ / Virtex-II Pro X Features

- High-Performance Platform FPGA Solution, Including
 - Up to twenty RocketIO™ or RocketIO X embedded Multi-Gigabit Transceivers (MGTS)
 - Up to two IBM PowerPC™ RISC processor blocks
- Based on Virtex-II™ Platform FPGA Technology
 - Flexible logic resources
 - SRAM-based in-system configuration
 - Active Interconnect technology
- SelectRAM™+ memory hierarchy
- Dedicated 18-bit x 18-bit multiplier blocks
- High-performance clock management circuitry
- SelectIO™-Ultra technology
- XCITE Digitally Controlled Impedance (DCI) I/O

Virtex-II Pro / Virtex-II Pro X family members and resources are shown in [Table 1](#).

Table 1: Virtex-II Pro / Virtex-II Pro X FPGA Family Members

Device ⁽¹⁾	RocketIO Transceiver Blocks	PowerPC Processor Blocks	Logic Cells ⁽²⁾	CLB (1 = 4 slices = max 128 bits)		18 X 18 Bit Multiplier Blocks	Block SelectRAM+		DCMs	Maximum User I/O Pads
				Slices	Max Distr RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)		
XC2VP2	4	0	3,168	1,408	44	12	12	216	4	204
XC2VP4	4	1	6,768	3,008	94	28	28	504	4	348
XC2VP7	8	1	11,088	4,928	154	44	44	792	4	396
XC2VP20	8	2	20,880	9,280	290	88	88	1,584	8	564
XC2VPX20	8 ⁽⁴⁾	1	22,032	9,792	306	88	88	1,584	8	552
XC2VP30	8	2	30,816	13,696	428	136	136	2,448	8	644
XC2VP40	0 ⁽³⁾ , 8, or 12	2	43,632	19,392	606	192	192	3,456	8	804
XC2VP50	0 ⁽³⁾ or 16	2	53,136	23,616	738	232	232	4,176	8	852
XC2VP70	16 or 20	2	74,448	33,088	1,034	328	328	5,904	8	996
XC2VPX70	20 ⁽⁴⁾	2	74,448	33,088	1,034	308	308	5,544	8	992
XC2VP100	0 ⁽³⁾ or 20	2	99,216	44,096	1,378	444	444	7,992	12	1,164

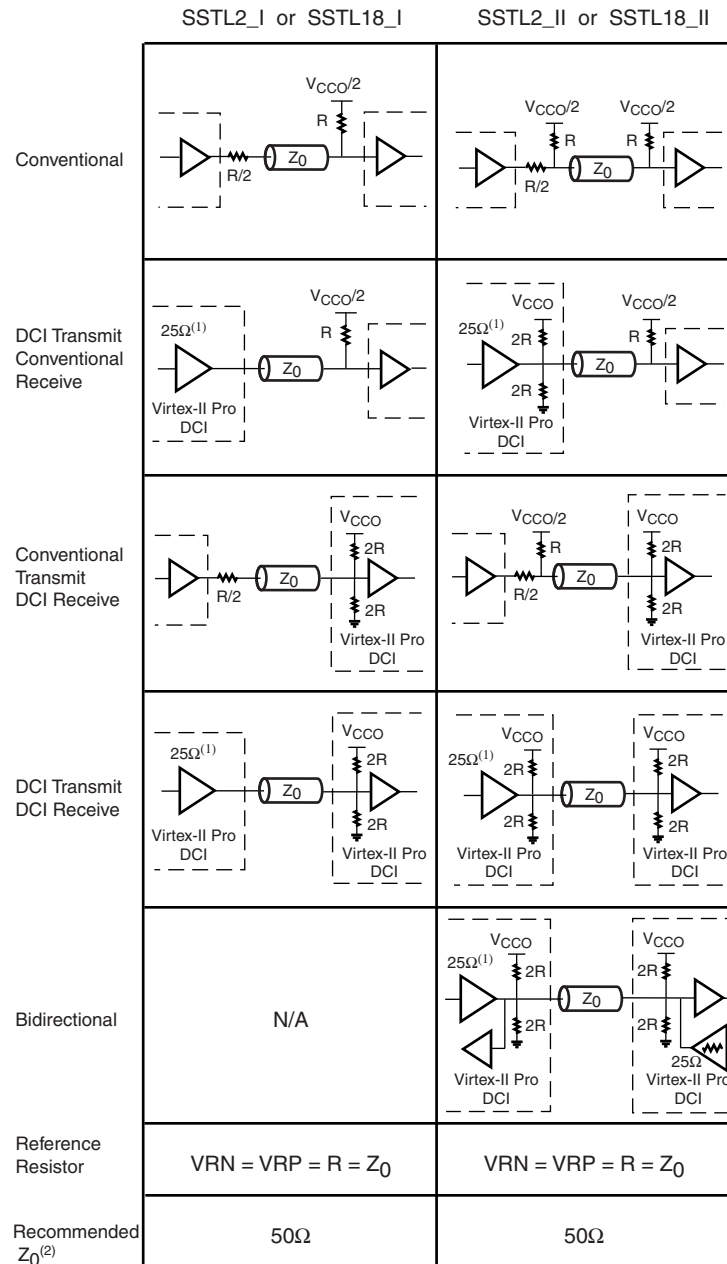
Notes:

- 7 speed grade devices are not available in Industrial grade.
- Logic Cell ≈ (1) 4-input LUT + (1)FF + Carry Logic
- These devices can be ordered in a configuration without RocketIO transceivers. See [Table 3](#) for package configurations.
- Virtex-II Pro X devices equipped with RocketIO X transceiver cores.

RocketIO X Transceiver Features (XC2VPX20 and XC2VPX70 Only)

- Variable-Speed Full-Duplex Transceiver (XC2VPX20) Allowing 2.488 Gb/s to 6.25 Gb/s Baud Transfer Rates.
 - Includes specific baud rates used by various standards, as listed in [Table 4, Module 2](#).
- Fixed-Speed Full-Duplex Transceiver (XC2VPX70) Operating at 4.25 Gb/s Baud Transfer Rate.
- Eight or Twenty Transceiver Modules on an FPGA, Depending upon Device
- Monolithic Clock Synthesis and Clock Recovery
 - Eliminates the need for external components
- Automatic Lock-to-Reference Function
- Programmable Serial Output Differential Swing
 - 200 mV to 1600 mV, peak-peak
 - Allows compatibility with other serial system voltage levels
- Programmable Pre-emphasis Levels 0 to 500%
- Telecom/Datacom Support Modes
 - "x8" and "x10" clocking/data paths
 - 64B/66B clocking support

Figure 29 provides examples illustrating the use of the SSTL2_I_DCI, SSTL2_II_DCI, SSTL18_I_DCI, and SSTL18_II_DCI I/O standards. For a complete list, see the [Virtex-II Pro Platform FPGA User Guide](#).



DS083-2_65b_011603

Notes:

1. The SSTL-compatible 25Ω series resistor is accounted for in the DCI buffer, and it is not DCI controlled.
2. Z_0 is the recommended PCB trace impedance.

Figure 29: SSTL DCI Usage Examples

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in **Figure 39**. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous; however, the storage element or flip-flop is available to implement a synchronous read. Any of the 16 bits can be read out asynchronously by varying the address. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

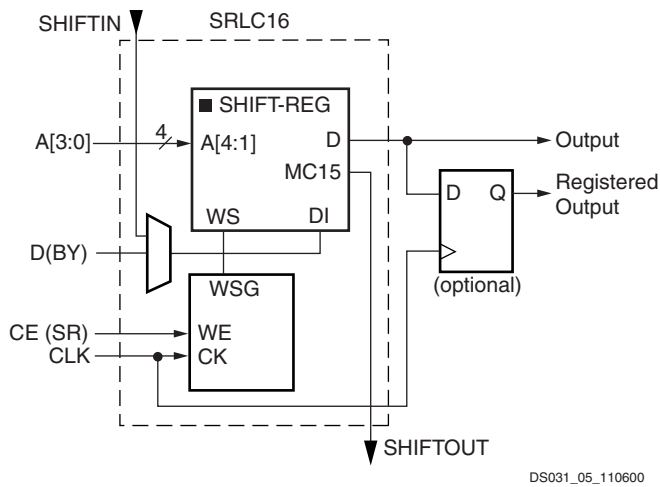


Figure 39: Shift Register Configurations

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See **Figure 40**.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

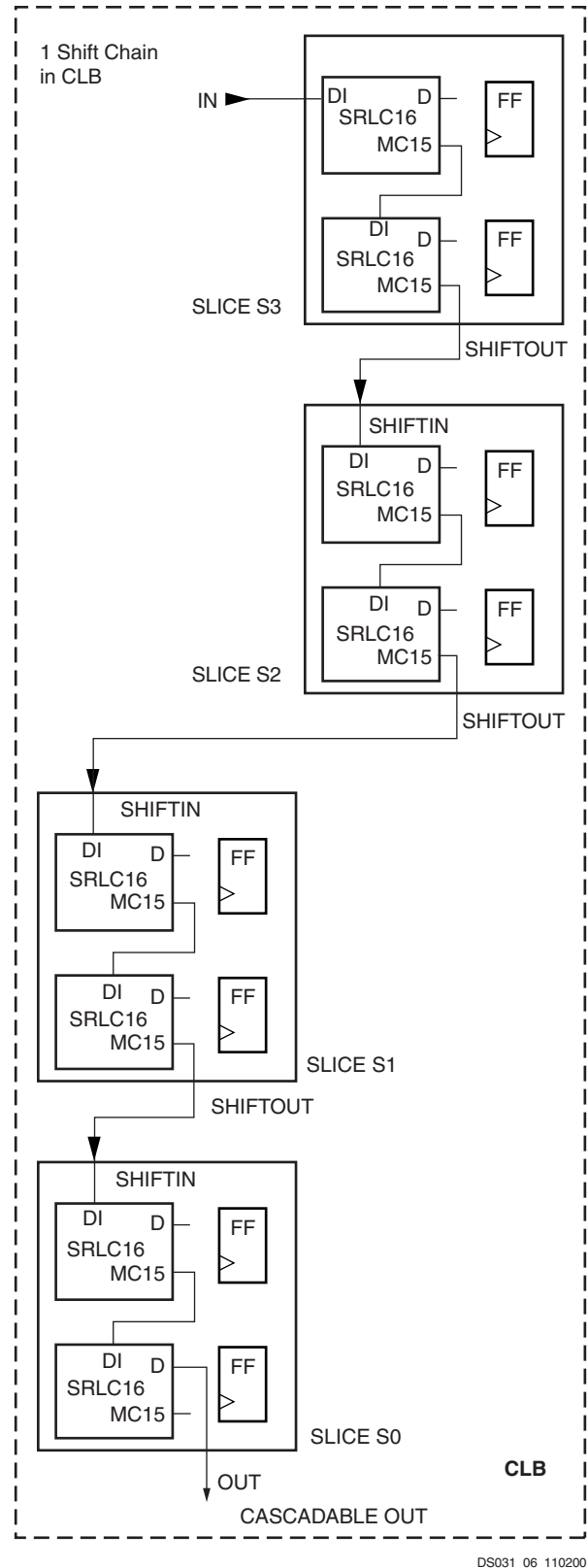


Figure 40: Cascadable Shift Register

IOB Output Switching Characteristics Standard Adjustments

Table 38 gives all standard-specific adjustments for output delays terminating at pads, based on standard capacitive load, C_{REF} . Output delays terminating at a pad are specified for LVCMOS25 with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 38: IOB Output Switching Characteristics Standard Adjustments

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
LVTTTL (Low-Voltage Transistor-Transistor Logic), Slow, 2 mA	LVTTTL_S2	$T_{OLVTTTL_S2}$	5.42	6.24	6.86	ns
LVTTTL, Slow, 4 mA	LVTTTL_S4	$T_{OLVTTTL_S4}$	3.09	3.55	3.91	ns
LVTTTL, Slow, 6 mA	LVTTTL_S6	$T_{OLVTTTL_S6}$	2.26	2.60	2.86	ns
LVTTTL, Slow, 8 mA	LVTTTL_S8	$T_{OLVTTTL_S8}$	1.47	1.69	1.86	ns
LVTTTL, Slow, 12 mA	LVTTTL_S12	$T_{OLVTTTL_S12}$	1.02	1.18	1.29	ns
LVTTTL, Slow, 16 mA	LVTTTL_S16	$T_{OLVTTTL_S16}$	0.46	0.53	0.58	ns
LVTTTL, Slow, 24 mA	LVTTTL_S24	$T_{OLVTTTL_S24}$	0.37	0.42	0.47	ns
LVTTTL, Fast, 2 mA	LVTTTL_F2	$T_{OLVTTTL_F2}$	4.42	5.09	5.59	ns
LVTTTL, Fast, 4 mA	LVTTTL_F4	$T_{OLVTTTL_F4}$	1.95	2.24	2.46	ns
LVTTTL, Fast, 6 mA	LVTTTL_F6	$T_{OLVTTTL_F6}$	1.10	1.26	1.39	ns
LVTTTL, Fast, 8 mA	LVTTTL_F8	$T_{OLVTTTL_F8}$	0.40	0.46	0.51	ns
LVTTTL, Fast, 12 mA	LVTTTL_F12	$T_{OLVTTTL_F12}$	0.24	0.27	0.30	ns
LVTTTL, Fast, 16 mA	LVTTTL_F16	$T_{OLVTTTL_F16}$	0.05	0.06	0.07	ns
LVTTTL, Fast, 24 mA	LVTTTL_F24	$T_{OLVTTTL_F24}$	-0.01	-0.01	-0.01	ns
LVC MOS (Low-Voltage CMOS), 3.3V, Slow, 2 mA	LVC MOS33_S2	$T_{OLVCMOS33_S2}$	5.42	6.23	6.86	ns
LVC MOS, 3.3V, Slow, 4 mA	LVC MOS33_S4	$T_{OLVCMOS33_S4}$	3.14	3.61	3.97	ns
LVC MOS, 3.3V, Slow, 6 mA	LVC MOS33_S6	$T_{OLVCMOS33_S6}$	2.26	2.60	2.86	ns
LVC MOS, 3.3V, Slow, 8 mA	LVC MOS33_S8	$T_{OLVCMOS33_S8}$	1.47	1.69	1.86	ns
LVC MOS, 3.3V, Slow, 12 mA	LVC MOS33_S12	$T_{OLVCMOS33_S12}$	1.03	1.18	1.30	ns
LVC MOS, 3.3V, Slow, 16 mA	LVC MOS33_S16	$T_{OLVCMOS33_S16}$	0.45	0.52	0.57	ns
LVC MOS, 3.3V, Slow, 24 mA	LVC MOS33_S24	$T_{OLVCMOS33_S24}$	0.39	0.44	0.49	ns
LVC MOS, 3.3V, Fast, 2 mA	LVC MOS33_F2	$T_{OLVCMOS33_F2}$	4.46	5.13	5.64	ns
LVC MOS, 3.3V, Fast, 4 mA	LVC MOS33_F4	$T_{OLVCMOS33_F4}$	1.96	2.25	2.48	ns
LVC MOS, 3.3V, Fast, 6 mA	LVC MOS33_F6	$T_{OLVCMOS33_F6}$	1.11	1.28	1.40	ns
LVC MOS, 3.3V, Fast, 8 mA	LVC MOS33_F8	$T_{OLVCMOS33_F8}$	0.41	0.47	0.52	ns
LVC MOS, 3.3V, Fast, 12 mA	LVC MOS33_F12	$T_{OLVCMOS33_F12}$	0.23	0.26	0.28	ns
LVC MOS, 3.3V, Fast, 16 mA	LVC MOS33_F16	$T_{OLVCMOS33_F16}$	0.02	0.02	0.03	ns
LVC MOS, 3.3V, Fast, 24 mA	LVC MOS33_F24	$T_{OLVCMOS33_F24}$	-0.07	-0.08	-0.09	ns
LVC MOS, 2.5V, Slow, 2 mA	LVC MOS25_S2	$T_{OLVCMOS25_S2}$	4.12	4.74	5.21	ns
LVC MOS, 2.5V, Slow, 4 mA	LVC MOS25_S4	$T_{OLVCMOS25_S4}$	2.43	2.80	3.07	ns
LVC MOS, 2.5V, Slow, 6 mA	LVC MOS25_S6	$T_{OLVCMOS25_S6}$	1.76	2.02	2.22	ns
LVC MOS, 2.5V, Slow, 8 mA	LVC MOS25_S8	$T_{OLVCMOS25_S8}$	1.04	1.19	1.31	ns
LVC MOS, 2.5V, Slow, 12 mA	LVC MOS25_S12	$T_{OLVCMOS25_S12}$	0.76	0.87	0.96	ns
LVC MOS, 2.5V, Slow, 16 mA	LVC MOS25_S16	$T_{OLVCMOS25_S16}$	0.41	0.47	0.52	ns
LVC MOS, 2.5V, Slow, 24 mA	LVC MOS25_S24	$T_{OLVCMOS25_S24}$	0.23	0.26	0.28	ns
LVC MOS, 2.5V, Fast, 2 mA	LVC MOS25_F2	$T_{OLVCMOS25_F2}$	3.29	3.78	4.16	ns
LVC MOS, 2.5V, Fast, 4 mA	LVC MOS25_F4	$T_{OLVCMOS25_F4}$	1.31	1.50	1.65	ns

Date	Version	Revision
12/05/03 (cont'd)	3.0 (cont'd)	- Non-speedsfile parameter values added or updated: Table 3: I_{BATT}. Table 4: For XC2VP100, I_{CCINTQ}, I_{CCOQ}, and I_{CCAUXQ}. Table 5: For XC2VP100, $I_{CCINTMIN}$. Table 17: T_{CPWL} and T_{CPWH}. Table 25: Added explanatory footnote to T_{RXLAT} (MGT receiver latency) max value. Table 57: Added Footnote (3) regarding use of CLKIN_DIVIDE_BY_2 attribute.
02/19/04	3.1	- Updated time and frequency parameters as per speedsfile v1.85. Table 2, Recommended Operating Conditions: Revised Footnotes (4) and (6). Table 4, Quiescent Supply Current: Added Footnote (1) and updated Typical parameters. Table 10, LVPECL DC Specifications: Added parameter values for Maximum Differential Input Voltage (LVPECL). Table 14, Register-to-Register Performance: Removed reference to a number of designs for which test data is no longer provided. Table 16, Processor Clocks Absolute AC Characteristics: Added Footnote (1) referring to XAPP755. - Added Table 41, Clock Distribution Switching Characteristics. - Revised section Configuration Timing, page 39 through page 41, and JTAG Test Access Port Switching Characteristics, page 42, with improved timing diagrams, parameter tables, and organization. Table 50, Master/Slave Serial Mode Timing Characteristics, and Table 51, SelectMAP Mode Write Timing Characteristics: Added parameter $F_{CC_STARTUP}$. Table 51, SelectMAP Mode Write Timing Characteristics: Broke out T_{SMDCC}/T_{SMCCD}, DATA[0:7] setup/hold time, by device, and added new parameter specifications for XC2VP70 and XC2VP100 devices. Table 57, Operating Frequency Ranges: Added callouts for existing Footnote (3) to the four CLKIN parameters. Added new Footnote (4) to the four CLKIN parameters. Added new Footnote (5) to CLK2X, CLK2X180. Added new Footnote (6) to CLK2X, CLK2X180; CLK0, CLK180; and CLKIN (using DLL outputs).
03/09/04	3.1.1	Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
04/22/04	3.2	Table 2, Recommended Operating Conditions: Corrected VTTX/VTRX lower voltage limit from 1.8V to 1.6V. Table 5, Power-On Current for Virtex-II Pro Devices: Added Footnote (2) stating that listed I_{CCOMIN} values apply to the entire device (all banks). Table 40, Output Delay Measurement Methodology: Corrected V_{MEAS} for LVTTTL from 1.4V to 1.65V. Table 57, Operating Frequency Ranges: Corrected CLKOUT_FREQ_1X_LF_MAX and CLKIN_FREQ_DLL_LF_MAX for -7 devices from 210 MHz to 270 MHz. Table 65, Package Skew: Removed XC2VP40FF1517.
06/30/04	4.0	Merged in DS110-3 (Module 3 of Virtex-II Pro X data sheet). This merge added numerous previously unpublished RocketIO X MGT parameters. Specifications in this revision are from speedsfile v1.86 .



Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information

DS083 (v5.0) June 21, 2011

Product Specification

This document provides Virtex™-II Pro Device/Package Combinations, Maximum I/Os, and Virtex-II Pro Pin Definitions, followed by pinout tables, for these packages:

- FG256/FGG256 Fine-Pitch BGA Package
- FG456/FGG456 Fine-Pitch BGA Package
- FG676/FGG676 Fine-Pitch BGA Package
- FF672 Flip-Chip Fine-Pitch BGA Package
- FF896 Flip-Chip Fine-Pitch BGA Package

- FF1152 Flip-Chip Fine-Pitch BGA Package
- FF1148 Flip-Chip Fine-Pitch BGA Package
- FF1517 Flip-Chip Fine-Pitch BGA Package
- FF1704 Flip-Chip Fine-Pitch BGA Package
- FF1696 Flip-Chip Fine-Pitch BGA Package

For device pinout diagrams and layout guidelines, refer to the [Virtex-II Pro Platform FPGA User Guide](#). ASCII package pinout files are also available for download from the Xilinx website (www.xilinx.com).

Virtex-II Pro Device/Package Combinations and Maximum I/Os⁽¹⁾

Wire-bond and flip-chip packages are available. [Table 1](#) and [Table 2](#) show the maximum number of user I/Os possible in wire-bond and flip-chip packages, respectively.

- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FGG denotes Pb-free wire-bond fine-pitch BGA (1.00 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch)

Table 1: Wire-Bond Packages Information

Package ⁽¹⁾	FG256/ FGG256	FG456/ FGG456	FG676/ FGG676
Pitch (mm)	1.00	1.00	1.00
Size (mm)	17 x 17	23 x 23	26 x 26
Maximum I/Os	140	248	412

Notes:

1. Wire-bond packages include FGGnnn Pb-free versions. See [Virtex-II Pro Ordering Examples \(Module 1\)](#).

Table 2: Flip-Chip Packages Information

Package	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Size (mm)	27 x 27	31 x 31	35 x 35	35 x 35	40 x 40	42.5 x 42.5	42.5 x 42.5
Maximum I/Os	396	556	644	812	964	1040	1200

[Table 3](#) shows the number of available I/Os, the number of RocketIO™ (or RocketIO X) multi-gigabit transceiver (MGT) pins, and the number of differential I/O pairs for each Virtex-II Pro device/package combination. The number of I/Os per package includes all user I/Os *except* the fifteen control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, and RSVD), the nine (per transceiver) RocketIO MGT pins (TXP, TXN, RXP, RXN, AVCCAUTX, AVCCAUXRX, VTTX, VTRX, and GNDA), and for Virtex-II Pro X devices only, the two BREFCLKN/BREFCLKP differential clock input pairs (four pins). The Virtex-II Pro X devices are highlighted in bold type.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

Table 6: FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
2	IO_L56N_2	J21	NC		
2	IO_L56P_2	J22	NC		
2	IO_L58N_2/VREF_2	J18	NC		
2	IO_L58P_2	K18	NC		
2	IO_L60N_2	K19	NC		
2	IO_L60P_2	K20	NC		
2	IO_L85N_2	K21			
2	IO_L85P_2	K22			
2	IO_L86N_2	K17			
2	IO_L86P_2	L17			
2	IO_L88N_2/VREF_2	L18			
2	IO_L88P_2	L19			
2	IO_L90N_2	L20			
2	IO_L90P_2	L21			
3	IO_L90N_3	M21			
3	IO_L90P_3	M20			
3	IO_L89N_3	M19			
3	IO_L89P_3	M18			
3	IO_L87N_3/VREF_3	M17			
3	IO_L87P_3	N17			
3	IO_L85N_3	N22			
3	IO_L85P_3	N21			
3	IO_L60N_3	N20	NC		
3	IO_L60P_3	N19	NC		
3	IO_L59N_3	N18	NC		
3	IO_L59P_3	P18	NC		
3	IO_L57N_3/VREF_3	P22	NC		
3	IO_L57P_3	P21	NC		
3	IO_L55N_3	P20	NC		
3	IO_L55P_3	P19	NC		
3	IO_L54N_3	P17	NC		
3	IO_L54P_3	R18	NC		
3	IO_L53N_3	R22	NC		
3	IO_L53P_3	R21	NC		
3	IO_L51N_3/VREF_3	R20	NC		
3	IO_L51P_3	R19	NC		

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
6	IO_L02P_6		AH26			
6	IO_L02N_6		AG26			
6	IO_L03P_6		AH29			
6	IO_L03N_6/VREF_6		AH30			
6	IO_L04P_6		AH27			
6	IO_L04N_6		AG28			
6	IO_L05P_6		AD25			
6	IO_L05N_6		AD26			
6	IO_L06P_6		AG29			
6	IO_L06N_6		AG30			
6	IO_L31P_6		AF25	NC		
6	IO_L31N_6		AE26	NC		
6	IO_L32P_6		AB23	NC		
6	IO_L32N_6		AB24	NC		
6	IO_L33P_6		AE27	NC		
6	IO_L33N_6/VREF_6		AE28	NC		
6	IO_L34P_6		AF27	NC		
6	IO_L34N_6		AF28	NC		
6	IO_L35P_6		AC25	NC		
6	IO_L35N_6		AC26	NC		
6	IO_L36P_6		AF29	NC		
6	IO_L36N_6		AF30	NC		
6	IO_L37P_6		AD27	NC		
6	IO_L37N_6		AD28	NC		
6	IO_L38P_6		AA23	NC		
6	IO_L38N_6		AA24	NC		
6	IO_L39P_6		AE29	NC		
6	IO_L39N_6/VREF_6		AE30	NC		
6	IO_L40P_6		AB25	NC		
6	IO_L40N_6		AB26	NC		
6	IO_L41P_6		Y23	NC		
6	IO_L41N_6		Y24	NC		
6	IO_L42P_6		AD29	NC		
6	IO_L42N_6		AD30	NC		
6	IO_L43P_6		AC27			
6	IO_L43N_6		AC28			

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L38N_2	N10				
2	IO_L38P_2	N9				
2	IO_L39N_2	M7				
2	IO_L39P_2	M6				
2	IO_L40N_2/VREF_2	L2				
2	IO_L40P_2	M2				
2	IO_L41N_2	N8				
2	IO_L41P_2	N7				
2	IO_L42N_2	L4				
2	IO_L42P_2	L3				
2	IO_L43N_2	M4				
2	IO_L43P_2	M3				
2	IO_L44N_2	P10				
2	IO_L44P_2	P9				
2	IO_L45N_2	N6				
2	IO_L45P_2	N5				
2	IO_L46N_2/VREF_2	M1				
2	IO_L46P_2	N1				
2	IO_L47N_2	P8				
2	IO_L47P_2	P7				
2	IO_L48N_2	N4				
2	IO_L48P_2	N3				
2	IO_L49N_2	N2				
2	IO_L49P_2	P2				
2	IO_L50N_2	R10				
2	IO_L50P_2	R9				
2	IO_L51N_2	P6				
2	IO_L51P_2	P5				
2	IO_L52N_2/VREF_2	P4				
2	IO_L52P_2	P3				
2	IO_L53N_2	T11				
2	IO_L53P_2	U11				
2	IO_L54N_2	R7				
2	IO_L54P_2	R6				
2	IO_L55N_2	P1				
2	IO_L55P_2	R1				
2	IO_L56N_2	T10				
2	IO_L56P_2	T9				

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	P17				
N/A	GND	P18				
N/A	GND	P19				
N/A	GND	P20				
N/A	GND	P21				
N/A	GND	R8				
N/A	GND	R14				
N/A	GND	R15				
N/A	GND	R16				
N/A	GND	R17				
N/A	GND	R18				
N/A	GND	R19				
N/A	GND	R20				
N/A	GND	R21				
N/A	GND	R27				
N/A	GND	T1				
N/A	GND	T14				
N/A	GND	T15				
N/A	GND	T16				
N/A	GND	T17				
N/A	GND	T18				
N/A	GND	T19				
N/A	GND	T20				
N/A	GND	T21				
N/A	GND	T34				
N/A	GND	U14				
N/A	GND	U15				
N/A	GND	U16				
N/A	GND	U17				
N/A	GND	U18				
N/A	GND	U19				
N/A	GND	U20				
N/A	GND	U21				
N/A	GND	V14				
N/A	GND	V15				
N/A	GND	V16				
N/A	GND	V17				
N/A	GND	V18				

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
6	IO_L87N_6/VREF_6	V33		
6	IO_L88P_6	V30		
6	IO_L88N_6	V31		
6	IO_L89P_6	V24		
6	IO_L89N_6	V25		
6	IO_L90P_6	V28		
6	IO_L90N_6	V29		
7	IO_L90P_7	U32		
7	IO_L90N_7	V32		
7	IO_L89P_7	U28		
7	IO_L89N_7	U29		
7	IO_L88P_7	U30		
7	IO_L88N_7/VREF_7	U31		
7	IO_L87P_7	T33		
7	IO_L87N_7	U33		
7	IO_L86P_7	U26		
7	IO_L86N_7	U27		
7	IO_L85P_7	T31		
7	IO_L85N_7	T32		
7	IO_L60P_7	R33		
7	IO_L60N_7	R34		
7	IO_L59P_7	U24		
7	IO_L59N_7	U25		
7	IO_L58P_7	R29		
7	IO_L58N_7/VREF_7	R30		
7	IO_L57P_7	P33		
7	IO_L57N_7	P34		
7	IO_L56P_7	T28		
7	IO_L56N_7	T29		
7	IO_L55P_7	P32		
7	IO_L55N_7	R32		
7	IO_L54P_7	P29		
7	IO_L54N_7	P30		
7	IO_L53P_7	T24		
7	IO_L53N_7	T25		
7	IO_L52P_7	N32		
7	IO_L52N_7/VREF_7	N33		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L43N_7	R37		
7	IO_L42P_7	R34		
7	IO_L42N_7	R35		
7	IO_L41P_7	U28		
7	IO_L41N_7	T28		
7	IO_L40P_7	R32		
7	IO_L40N_7/VREF_7	R33		
7	IO_L39P_7	P38		
7	IO_L39N_7	P39		
7	IO_L38P_7	T29		
7	IO_L38N_7	T30		
7	IO_L37P_7	N37		
7	IO_L37N_7	P37		
7	IO_L36P_7	P35		
7	IO_L36N_7	P36		
7	IO_L35P_7	T27		
7	IO_L35N_7	R27		
7	IO_L34P_7	P33		
7	IO_L34N_7/VREF_7	P34		
7	IO_L33P_7	N38		
7	IO_L33N_7	N39		
7	IO_L32P_7	R28		
7	IO_L32N_7	R29		
7	IO_L31P_7	N35		
7	IO_L31N_7	M36		
7	IO_L30P_7	N33		
7	IO_L30N_7	N34		
7	IO_L29P_7	R30		
7	IO_L29N_7	R31		
7	IO_L28P_7	M37		
7	IO_L28N_7/VREF_7	M38		
7	IO_L27P_7	M33		
7	IO_L27N_7	M34		
7	IO_L26P_7	P28		
7	IO_L26N_7	P29		
7	IO_L25P_7	L38		
7	IO_L25N_7	L39		
7	IO_L24P_7	L36		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L24N_7	L37		
7	IO_L23P_7	P31		
7	IO_L23N_7	P32		
7	IO_L22P_7	L34		
7	IO_L22N_7/VREF_7	L35		
7	IO_L21P_7	L32		
7	IO_L21N_7	L33		
7	IO_L20P_7	N29		
7	IO_L20N_7	M29		
7	IO_L19P_7	K38		
7	IO_L19N_7	K39		
7	IO_L18P_7	J37		
7	IO_L18N_7	K37		
7	IO_L17P_7	N30		
7	IO_L17N_7	P30		
7	IO_L16P_7	K35		
7	IO_L16N_7/VREF_7	K36		
7	IO_L15P_7	K34		
7	IO_L15N_7	K33		
7	IO_L14P_7	N31		
7	IO_L14N_7	M32		
7	IO_L13P_7	J38		
7	IO_L13N_7	J39		
7	IO_L12P_7	J35		
7	IO_L12N_7	H36		
7	IO_L11P_7	M30		
7	IO_L11N_7	L31		
7	IO_L10P_7	J33		
7	IO_L10N_7/VREF_7	J34		
7	IO_L09P_7	H37		
7	IO_L09N_7	H38		
7	IO_L08P_7	K31		
7	IO_L08N_7	K32		
7	IO_L07P_7	H33		
7	IO_L07N_7	H34		
7	IO_L84P_7	G38	NC	
7	IO_L84N_7	G39	NC	
7	IO_L82P_7	G36	NC	

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L08P_2		K5		
2	IO_L09N_2		K8		
2	IO_L09P_2		K7		
2	IO_L10N_2/VREF_2		K2		
2	IO_L10P_2		K1		
2	IO_L11N_2		L8		
2	IO_L11P_2		L9		
2	IO_L12N_2		L6		
2	IO_L12P_2		L7		
2	IO_L13N_2		K3		
2	IO_L13P_2		L3		
2	IO_L14N_2		L5		
2	IO_L14P_2		L4		
2	IO_L15N_2		L1		
2	IO_L15P_2		L2		
2	IO_L16N_2/VREF_2		M7		
2	IO_L16P_2		M8		
2	IO_L17N_2		M11		
2	IO_L17P_2		M12		
2	IO_L18N_2		M9		
2	IO_L18P_2		M10		
2	IO_L19N_2		M2		
2	IO_L19P_2		M3		
2	IO_L20N_2		M4		
2	IO_L20P_2		M5		
2	IO_L21N_2		N7		
2	IO_L21P_2		N8		
2	IO_L22N_2/VREF_2		N5		
2	IO_L22P_2		N6		
2	IO_L23N_2		N9		
2	IO_L23P_2		N10		
2	IO_L24N_2		N3		
2	IO_L24P_2		N4		
2	IO_L25N_2		N1		
2	IO_L25P_2		N2		
2	IO_L26N_2		N11		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L26P_2		N12		
2	IO_L27N_2		P9		
2	IO_L27P_2		P10		
2	IO_L28N_2/VREF_2		P7		
2	IO_L28P_2		P8		
2	IO_L29N_2		P11		
2	IO_L29P_2		P12		
2	IO_L30N_2		P5		
2	IO_L30P_2		P6		
2	IO_L31N_2		P1		
2	IO_L31P_2		P2		
2	IO_L32N_2		R9		
2	IO_L32P_2		R10		
2	IO_L33N_2		R5		
2	IO_L33P_2		R6		
2	IO_L34N_2/VREF_2		P3		
2	IO_L34P_2		R3		
2	IO_L35N_2		R1		
2	IO_L35P_2		R2		
2	IO_L36N_2		R11		
2	IO_L36P_2		R12		
2	IO_L37N_2		T6		
2	IO_L37P_2		T7		
2	IO_L38N_2		T8		
2	IO_L38P_2		R8		
2	IO_L39N_2		T4		
2	IO_L39P_2		T5		
2	IO_L40N_2/VREF_2		T2		
2	IO_L40P_2		T3		
2	IO_L41N_2		T10		
2	IO_L41P_2		T11		
2	IO_L42N_2		U7		
2	IO_L42P_2		U8		
2	IO_L43N_2		U5		
2	IO_L43P_2		U6		
2	IO_L44N_2		U9		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L03P_7		D37		
7	IO_L03N_7		E37		
7	IO_L02P_7		D36		
7	IO_L02N_7		E36		
7	IO_L01P_7/VRN_7		C37		
7	IO_L01N_7/VRP_7		C38		
0	VCCO_0		D25		
0	VCCO_0		G23		
0	VCCO_0		G28		
0	VCCO_0		G32		
0	VCCO_0		J25		
0	VCCO_0		J29		
0	VCCO_0		P22		
0	VCCO_0		P23		
0	VCCO_0		P24		
0	VCCO_0		P25		
0	VCCO_0		P26		
0	VCCO_0		R22		
0	VCCO_0		R23		
0	VCCO_0		R24		
0	VCCO_0		R25		
1	VCCO_1		R21		
1	VCCO_1		R20		
1	VCCO_1		R19		
1	VCCO_1		R18		
1	VCCO_1		P21		
1	VCCO_1		P20		
1	VCCO_1		P19		
1	VCCO_1		P18		
1	VCCO_1		P17		
1	VCCO_1		J18		
1	VCCO_1		J14		
1	VCCO_1		G20		
1	VCCO_1		G15		
1	VCCO_1		G11		

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
0	IO_L11N_0	M25	NC
0	IO_L11P_0	M26	NC
0	IO_L12N_0	F26	NC
0	IO_L12P_0	G26	NC
0	IO_L18N_0	B26	NC
0	IO_L18P_0/VREF_0	C26	NC
0	IO_L46N_0	G24	
0	IO_L46P_0	G25	
0	IO_L47N_0	K26	
0	IO_L47P_0	L26	
0	IO_L48N_0	E25	
0	IO_L48P_0	F25	
0	IO_L49N_0	C24	
0	IO_L49P_0	C25	
0	IO_L50_0/No_Pair	L24	
0	IO_L53_0/No_Pair	L25	
0	IO_L54N_0	A25	
0	IO_L54P_0	B25	
0	IO_L55N_0	H23	
0	IO_L55P_0	H24	
0	IO_L56N_0	J25	
0	IO_L56P_0	K25	
0	IO_L57N_0	E24	
0	IO_L57P_0/VREF_0	F24	
0	IO_L58N_0	D23	
0	IO_L58P_0	D24	
0	IO_L59N_0	J24	
0	IO_L59P_0	K24	
0	IO_L60N_0	A24	
0	IO_L60P_0	B24	
0	IO_L64N_0	F23	
0	IO_L64P_0	G23	
0	IO_L65N_0	M22	
0	IO_L65P_0	M23	
0	IO_L66N_0	B23	
0	IO_L66P_0/VREF_0	C23	
0	IO_L67N_0	H22	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L69P_2	F6	
2	IO_L70N_2/VREF_2	G5	
2	IO_L70P_2	F5	
2	IO_L71N_2	P10	
2	IO_L71P_2	P11	
2	IO_L72N_2	G3	
2	IO_L72P_2	G4	
2	IO_L07N_2	G1	
2	IO_L07P_2	G2	
2	IO_L08N_2	N8	
2	IO_L08P_2	P9	
2	IO_L09N_2	H6	
2	IO_L09P_2	H7	
2	IO_L10N_2/VREF_2	H4	
2	IO_L10P_2	H5	
2	IO_L11N_2	R12	
2	IO_L11P_2	T12	
2	IO_L12N_2	H2	
2	IO_L12P_2	H3	
2	IO_L13N_2	J6	
2	IO_L13P_2	J7	
2	IO_L14N_2	R10	
2	IO_L14P_2	R11	
2	IO_L15N_2	J3	
2	IO_L15P_2	J4	
2	IO_L16N_2/VREF_2	J2	
2	IO_L16P_2	H1	
2	IO_L17N_2	R8	
2	IO_L17P_2	R9	
2	IO_L18N_2	K5	
2	IO_L18P_2	K6	
2	IO_L19N_2	K1	
2	IO_L19P_2	K2	
2	IO_L20N_2	T10	
2	IO_L20P_2	T11	
2	IO_L21N_2	L7	
2	IO_L21P_2	K7	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L08N_7	N35	
7	IO_L07P_7	G41	
7	IO_L07N_7	G42	
7	IO_L72P_7	G39	
7	IO_L72N_7	G40	
7	IO_L71P_7	P32	
7	IO_L71N_7	P33	
7	IO_L70P_7	F38	
7	IO_L70N_7/VREF_7	G38	
7	IO_L69P_7	F37	
7	IO_L69N_7	G37	
7	IO_L68P_7	N32	
7	IO_L68N_7	N33	
7	IO_L67P_7	G35	
7	IO_L67N_7	G36	
7	IO_L66P_7	F41	
7	IO_L66N_7	F42	
7	IO_L65P_7	P31	
7	IO_L65N_7	N31	
7	IO_L64P_7	E41	
7	IO_L64N_7/VREF_7	F40	
7	IO_L63P_7	E36	
7	IO_L63N_7	F36	
7	IO_L62P_7	M34	
7	IO_L62N_7	M35	
7	IO_L61P_7	E35	
7	IO_L61N_7	F35	
7	IO_L84P_7	D40	
7	IO_L84N_7	E40	
7	IO_L83P_7	L34	
7	IO_L83N_7	L35	
7	IO_L82P_7	D39	
7	IO_L82N_7/VREF_7	E39	
7	IO_L81P_7	D38	
7	IO_L81N_7	E37	
7	IO_L80P_7	K34	
7	IO_L80N_7	J35	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AC25	
N/A	GND	AB25	
N/A	GND	AA25	
N/A	GND	Y25	
N/A	GND	W25	
N/A	GND	V25	
N/A	GND	U25	
N/A	GND	AL24	
N/A	GND	AF24	
N/A	GND	AE24	
N/A	GND	AD24	
N/A	GND	AC24	
N/A	GND	AB24	
N/A	GND	AA24	
N/A	GND	Y24	
N/A	GND	W24	
N/A	GND	V24	
N/A	GND	U24	
N/A	GND	M24	
N/A	GND	BB23	
N/A	GND	AV23	
N/A	GND	AP23	
N/A	GND	AF23	
N/A	GND	AE23	
N/A	GND	AD23	
N/A	GND	AC23	
N/A	GND	AB23	
N/A	GND	AA23	
N/A	GND	Y23	
N/A	GND	W23	
N/A	GND	V23	
N/A	GND	U23	
N/A	GND	J23	
N/A	GND	E23	
N/A	GND	A23	
N/A	GND	AF22	
N/A	GND	AE22	