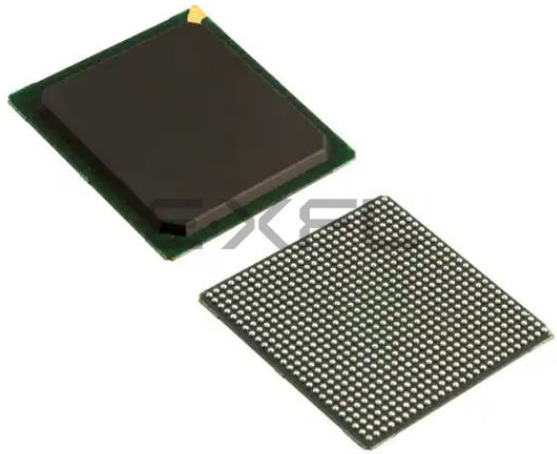

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2320 |
| Number of Logic Elements/Cells | 20880 |
| Total RAM Bits | 1622016 |
| Number of I/O | 404 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 676-BGA |
| Supplier Device Package | 676-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2vp20-5fgg676i |

## Notice of Disclaimer



## Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)

### Disparity Control

The 8B/10B encoder is initialized with a negative running disparity. Unique control allows forcing the current running disparity state.

TXRUNDISP signals its current running disparity. This may be useful in those cases where there is a need to manipulate the initial running disparity value.

Bits TXCHARDISPMODE and TXCHARDISPVAL control the generation of running disparity before each byte.

For example, the transceiver can generate the sequence

```
K28.5+ K28.5+ K28.5- K28.5-
```

or

```
K28.5- K28.5- K28.5+ K28.5+
```

by specifying inverted running disparity for the second and fourth bytes.

### Transmit FIFO

Proper operation of the circuit is only possible if the FPGA clock (TXUSRCLK) is frequency-locked to the reference clock (REFCLK). Phase variations up to one clock cycle are allowable. The FIFO has a depth of four. Overflow or underflow conditions are detected and signaled at the interface. Bypassing of this FIFO is programmable.

### 8B/10B Encoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

A bypassable 8B/10B encoder is included. The encoder uses the same 256 data characters and 12 control characters used by Gigabit Ethernet, Fibre Channel, and InfiniBand.

The encoder accepts 8 bits of data along with a K-character signal for a total of 9 bits per character applied, and generates a 10 bit character for transmission. If the K-character signal is High, the data is encoded into one of the twelve possible K-characters available in the 8B/10B code. If the K-character input is Low, the 8 bits are encoded as standard data. If the K-character input is High, and a user applies other than one of the twelve possible combinations, TXKERR indicates the error.

### 8B/10B Decoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

An optional 8B/10B decoder is included. A programmable option allows the decoder to be bypassed. When the 8B/10B decoder is bypassed, the 10-bit character order is, for example,

RXCHARISK[0] (first bit received)
RXRUNDISP[0]
RXDATA[7:0] (last bit received is RXDATA[0])

The decoder uses the same table that is used for Gigabit Ethernet, Fibre Channel, and InfiniBand. In addition to decoding all data and K-characters, the decoder has several extra features. The decoder separately detects both “disparity errors” and “out-of-band” errors. A disparity error is the reception of 10-bit character that exists within the 8B/10B table but has an incorrect disparity. An out-of-band error is the reception of a 10-bit character that does not exist within the 8B/10B table. It is possible to obtain an out-of-band error without having a disparity error. The proper disparity is always computed for both legal and illegal characters. The current running disparity is available at the RXRUNDISP signal.

The 8B/10B decoder performs a unique operation if out-of-band data is detected. If out-of-band data is detected, the decoder signals the error and passes the illegal 10-bits through and places them on the outputs. This can be used for debugging purposes if desired.

The decoder also signals the reception of one of the 12 valid K-characters. In addition, a programmable comma detect is included. The comma detect signal registers a comma on the receipt of any comma+, comma–, or both. Since the comma is defined as a 7-bit character, this includes several out-of-band characters. Another option allows the decoder to detect only the three defined commas (K28.1, K28.5, and K28.7) as comma+, comma–, or both. In total, there are six possible options, three for valid commas and three for "any comma."

Note that all bytes (1, 2, 4, or 8) at the RX FPGA interface each have their own individual 8B/10B indicators (K-character, disparity error, out-of-band error, current running disparity, and comma detect).

### Receiver Buffer

The receiver includes buffers (FIFOs) in the datapath. This section gives the reasons for including the buffers and outlines their operation.

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

The receiver uses an *elastic buffer*, where "elastic" refers to the ability to modify the read pointer for clock correction and channel bonding.

#### Comma Detection

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indi-

*Table 27:* **RocketIO Transmitter Switching Characteristics**

| Description | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Serial data rate, full-speed clock | $F_{GTX}$ | Flipchip packages | 1.0 | | 3.125(1) | Gb/s |
| | | Wirebond packages | 1.0 | | 2.5(1) | Gb/s |
| Serial data rate, half-speed clock(3) (2X oversampling) | | Flipchip packages | 0.600 | | 1.0 | Gb/s |
| | | Wirebond packages | 0.600 | | 1.0 | Gb/s |
| Serial data output deterministic jitter | $T_{DJ}$ | 2.126 Gb/s – 3.125 Gb/s | | | 0.17 | UI(2) |
| | | 1.0626 Gb/s – 2.125 Gb/s | | | 0.08 | UI |
| | | 1.0 Gb/s – 1.0625 Gb/s | | | 0.05 | UI |
| | | 600 Mb/s – 999 Mb/s | | | 0.08(4) | UI |
| Serial data output random jitter | $T_{RJ}$ | 2.126 Gb/s – 3.125 Gb/s | | | 0.18 | UI |
| | | 1.0626 Gb/s – 2.125 Gb/s | | | 0.19 | UI |
| | | 1.0 Gb/s – 1.0625 Gb/s | | | 0.18 | UI |
| | | 600 Mb/s – 999 Mb/s | | | 0.18(4) | UI |
| TX rise time | $T_{RTX}$ | 20% – 80% | | 120 | | ps |
| TX fall time | $T_{FTX}$ | | | 120 | | ps |
| Transmit latency(5) | $T_{TXLAT}$ | Including CRC | | 14 | 17 | TXUSR CLK cycles |
| | | Excluding CRC | | 8 | 11 | |
| TXUSRCLK duty cycle | $T_{TXDC}$ | | 45 | 50 | 55 | % |
| TXUSRCLK2 duty cycle | $T_{TX2DC}$ | | 45 | 50 | 55 | % |

**Notes:**
1. Serial data rate in the -5 speed grade is limited to 2.0 Gb/s in both wirebond and flipchip packages.
2. UI = Unit Interval
3. For serial rates under 1 Gb/s, the 3X (or greater) oversampling techniques described in **XAPP572** are required to meet the transmit jitter and receive jitter tolerance specifications defined in this data sheet.
4. The oversampling techniques described in **XAPP572** are required to meet these specifications for serial rates less than 1 Gb/s.
5. Transmit latency delay TXDATA to TXP/TXN. Refer to ***RocketIO Transceiver User Guide*** for more information on calculating latency.

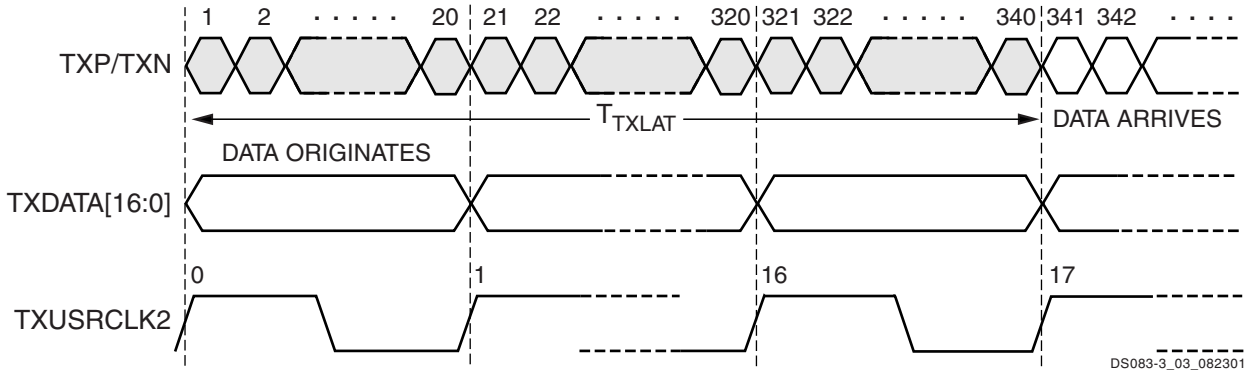



*Figure 5:* **RocketIO Transmit Latency (Maximum, Including CRC)**

# Virtex-II Pro Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

## Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM

*Table 55:* **Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM**

| | | | Speed Grade | | | |
|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Device** | **-7** | **-6** | **-5** | **Units** |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)<br>For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25. | | | | | | |
| No Delay<br>Global Clock and IFF(2) with DCM | $T_{PSDCM}/T_{PHDCM}$ | XC2VP2 | 1.54/–0.58 | 1.54/–0.57 | 1.54/–0.56 | ns |
| | | XC2VP4 | 1.59/–0.59 | 1.59/–0.58 | 1.59/–0.57 | ns |
| | | XC2VP7 | 1.66/–0.61 | 1.66/–0.59 | 1.66/–0.57 | ns |
| | | XC2VP20 | 1.68/–0.53 | 1.68/–0.53 | 1.68/–0.50 | ns |
| | | XC2VPX20 | 1.68/–0.53 | 1.68/–0.53 | 1.68/–0.50 | ns |
| | | XC2VP30 | 1.81/–0.74 | 1.81/–0.74 | 1.81/–0.71 | ns |
| | | XC2VP40 | 1.85/–0.65 | 1.85/–0.64 | 1.85/–0.60 | ns |
| | | XC2VP50 | 1.85/–0.57 | 1.85/–0.54 | 1.85/–0.50 | ns |
| | | XC2VP70 | 1.86/–0.45 | 1.86/–0.39 | 1.86/–0.30 | ns |
| | | XC2VPX70 | 1.86/–0.45 | 1.86/–0.39 | 1.86/–0.30 | ns |
| | | XC2VP100 | N/A | 1.86/–0.35 | 1.87/–0.28 | ns |

**Notes:**

1. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case duty-cycle distortion using CLK0 and CLK180, $T_{DCD\_CLK180}$.
3. IFF = Input Flip-Flop or Latch

## Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM

*Table 56:* **Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM**

| | | | Speed Grade | | | |
|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Device** | **-7** | **-6** | **-5** | **Units** |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.<br>For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25. | | | | | | |
| Full Delay<br>Global Clock and IFF without DCM | $T_{PSFD}/T_{PHFD}$ | XC2VP2 | 1.80/–0.44 | 1.85/–0.41 | 1.96/–0.43 | ns |
| | | XC2VP4 | 1.82/–0.53 | 1.83/–0.31 | 1.90/–0.29 | ns |
| | | XC2VP7 | 1.80/–0.34 | 1.81/–0.24 | 1.88/–0.19 | ns |
| | | XC2VP20 | 1.76/–0.24 | 1.83/–0.17 | 1.92/–0.15 | ns |
| | | XC2VPX20 | 1.76/–0.24 | 1.83/–0.17 | 1.92/–0.15 | ns |
| | | XC2VP30 | 1.75/–0.22 | 1.92/–0.26 | 1.99/–0.23 | ns |
| | | XC2VP40 | 2.25/–0.54 | 2.40/–0.56 | 2.49/–0.54 | ns |
| | | XC2VP50 | 2.93/–1.02 | 2.98/–0.93 | 3.00/–0.83 | ns |
| | | XC2VP70 | 2.79/–0.72 | 2.79/–0.55 | 2.78/–0.41 | ns |
| | | XC2VPX70 | 2.79/–0.72 | 2.79/–0.55 | 2.78/–0.41 | ns |
| | | XC2VP100 | N/A | 5.58/–2.35 | 5.60/–2.35 | ns |

**Notes:**
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

*Table 8:* **FF672 — XC2VP2, XC2VP4, and XC2VP7**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP2 | XC2VP4 | XC2VP7 |
| | | | | | |
| 3 | IO_L90N_3 | P2 | | | |
| 3 | IO_L90P_3 | P3 | | | |
| 3 | IO_L89N_3 | P4 | | | |
| 3 | IO_L89P_3 | P5 | | | |
| 3 | IO_L88N_3 | P6 | | | |
| 3 | IO_L88P_3 | P7 | | | |
| 3 | IO_L87N_3/VREF_3 | R1 | | | |
| 3 | IO_L87P_3 | R2 | | | |
| 3 | IO_L86N_3 | R3 | | | |
| 3 | IO_L86P_3 | R4 | | | |
| 3 | IO_L85N_3 | R5 | | | |
| 3 | IO_L85P_3 | R6 | | | |
| 3 | IO_L60N_3 | P8 | NC | | |
| 3 | IO_L60P_3 | R8 | NC | | |
| 3 | IO_L59N_3 | T1 | NC | | |
| 3 | IO_L59P_3 | T2 | NC | | |
| 3 | IO_L58N_3 | T3 | NC | | |
| 3 | IO_L58P_3 | T4 | NC | | |
| 3 | IO_L57N_3/VREF_3 | T5 | NC | | |
| 3 | IO_L57P_3 | T6 | NC | | |
| 3 | IO_L56N_3 | R7 | NC | | |
| 3 | IO_L56P_3 | T7 | NC | | |
| 3 | IO_L55N_3 | T8 | NC | | |
| 3 | IO_L55P_3 | U7 | NC | | |
| 3 | IO_L54N_3 | U1 | NC | | |
| 3 | IO_L54P_3 | V1 | NC | | |
| 3 | IO_L53N_3 | U3 | NC | | |
| 3 | IO_L53P_3 | U4 | NC | | |
| 3 | IO_L52N_3 | U5 | NC | | |
| 3 | IO_L52P_3 | U6 | NC | | |
| 3 | IO_L51N_3/VREF_3 | V2 | NC | | |
| 3 | IO_L51P_3 | V3 | NC | | |
| 3 | IO_L50N_3 | V4 | NC | | |
| 3 | IO_L50P_3 | V5 | NC | | |
| 3 | IO_L49N_3 | V6 | NC | | |
| 3 | IO_L49P_3 | V7 | NC | | |

*Table 8:* **FF672 — XC2VP2, XC2VP4, and XC2VP7**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP2 | XC2VP4 | XC2VP7 |
| 6 | IO_L01P_6/VRN_6 | AF24 | | | |
| 6 | IO_L01N_6/VRP_6 | AE24 | | | |
| 6 | IO_L02P_6 | AD23 | | | |
| 6 | IO_L02N_6 | AC24 | | | |
| 6 | IO_L03P_6 | AE26 | | | |
| 6 | IO_L03N_6/VREF_6 | AF25 | | | |
| 6 | IO_L04P_6 | AD25 | | | |
| 6 | IO_L04N_6 | AD26 | | | |
| 6 | IO_L05P_6 | AC25 | | | |
| 6 | IO_L05N_6 | AC26 | | | |
| 6 | IO_L06P_6 | AB23 | | | |
| 6 | IO_L06N_6 | AB24 | | | |
| 6 | IO_L39P_6 | AB25 | NC | NC | NC |
| 6 | IO_L39N_6/VREF_6 | AB26 | NC | NC | NC |
| 6 | IO_L41P_6 | AA22 | NC | NC | NC |
| 6 | IO_L41N_6 | AA23 | NC | NC | NC |
| 6 | IO_L42P_6 | AA24 | NC | NC | NC |
| 6 | IO_L42N_6 | AA25 | NC | NC | NC |
| 6 | IO_L43P_6 | Y21 | NC | | |
| 6 | IO_L43N_6 | Y22 | NC | | |
| 6 | IO_L44P_6 | Y23 | NC | | |
| 6 | IO_L44N_6 | Y24 | NC | | |
| 6 | IO_L45P_6 | AA26 | NC | | |
| 6 | IO_L45N_6/VREF_6 | Y26 | NC | | |
| 6 | IO_L46P_6 | W21 | NC | | |
| 6 | IO_L46N_6 | W22 | NC | | |
| 6 | IO_L47P_6 | W23 | NC | | |
| 6 | IO_L47N_6 | W24 | NC | | |
| 6 | IO_L48P_6 | W25 | NC | | |
| 6 | IO_L48N_6 | W26 | NC | | |
| 6 | IO_L49P_6 | V20 | NC | | |
| 6 | IO_L49N_6 | V21 | NC | | |
| 6 | IO_L50P_6 | V22 | NC | | |
| 6 | IO_L50N_6 | V23 | NC | | |
| 6 | IO_L51P_6 | V24 | NC | | |
| 6 | IO_L51N_6/VREF_6 | V25 | NC | | |
| 6 | IO_L52P_6 | U21 | NC | | |

*Table 10:* **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | | | |
|---|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 |
| 4 | IO_L27P_4/VREF_4 | AL10 | NC | NC | | |
| 4 | IO_L37N_4 | AE13 | | | | |
| 4 | IO_L37P_4 | AF13 | | | | |
| 4 | IO_L38N_4 | AG13 | | | | |
| 4 | IO_L38P_4 | AH13 | | | | |
| 4 | IO_L39N_4 | AJ11 | | | | |
| 4 | IO_L39P_4 | AK11 | | | | |
| 4 | IO_L43N_4 | AE14 | | | | |
| 4 | IO_L43P_4 | AF14 | | | | |
| 4 | IO_L44N_4 | AJ13 | | | | |
| 4 | IO_L44P_4 | AK13 | | | | |
| 4 | IO_L45N_4 | AL11 | | | | |
| 4 | IO_L45P_4/VREF_4 | AM11 | | | | |
| 4 | IO_L46N_4 | AE15 | | | | |
| 4 | IO_L46P_4 | AF15 | | | | |
| 4 | IO_L47N_4 | AG14 | | | | |
| 4 | IO_L47P_4 | AH14 | | | | |
| 4 | IO_L48N_4 | AL13 | | | | |
| 4 | IO_L48P_4 | AL12 | | | | |
| 4 | IO_L49N_4 | AD16 | | | | |
| 4 | IO_L49P_4 | AE16 | | | | |
| 4 | IO_L50_4/No_Pair | AJ14 | | | | |
| 4 | IO_L53_4/No_Pair | AK14 | | | | |
| 4 | IO_L54N_4 | AM14 | | | | |
| 4 | IO_L54P_4 | AM13 | | | | |
| 4 | IO_L55N_4 | AF16 | | | | |
| 4 | IO_L55P_4 | AG16 | | | | |
| 4 | IO_L56N_4 | AH15 | | | | |
| 4 | IO_L56P_4 | AJ15 | | | | |
| 4 | IO_L57N_4 | AL14 | | | | |
| 4 | IO_L57P_4/VREF_4 | AL15 | | | | |
| 4 | IO_L67N_4 | AD17 | | | | |
| 4 | IO_L67P_4 | AE17 | | | | |
| 4 | IO_L68N_4 | AH16 | | | | |
| 4 | IO_L68P_4 | AJ16 | | | | |
| 4 | IO_L69N_4 | AK16 | | | | |
| 4 | IO_L69P_4/VREF_4 | AL16 | | | | |
| 4 | IO_L73N_4 | AF17 | | | | |

*Table 10:* **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | | | |
|---|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 |
| N/A | VCCINT | Y13 | | | | |
| N/A | VCCINT | Y22 | | | | |
| N/A | VCCINT | AA13 | | | | |
| N/A | VCCINT | AA22 | | | | |
| N/A | VCCINT | AB13 | | | | |
| N/A | VCCINT | AB14 | | | | |
| N/A | VCCINT | AB15 | | | | |
| N/A | VCCINT | AB16 | | | | |
| N/A | VCCINT | AB17 | | | | |
| N/A | VCCINT | AB18 | | | | |
| N/A | VCCINT | AB19 | | | | |
| N/A | VCCINT | AB20 | | | | |
| N/A | VCCINT | AB21 | | | | |
| N/A | VCCINT | AB22 | | | | |
| N/A | VCCINT | AC12 | | | | |
| N/A | VCCINT | AC23 | | | | |
| N/A | VCCINT | AD11 | | | | |
| N/A | VCCINT | AD24 | | | | |
| N/A | VCCAUX | C3 | | | | |
| N/A | VCCAUX | C4 | | | | |
| N/A | VCCAUX | C17 | | | | |
| N/A | VCCAUX | C18 | | | | |
| N/A | VCCAUX | C31 | | | | |
| N/A | VCCAUX | C32 | | | | |
| N/A | VCCAUX | D3 | | | | |
| N/A | VCCAUX | D32 | | | | |
| N/A | VCCAUX | U1 | | | | |
| N/A | VCCAUX | V1 | | | | |
| N/A | VCCAUX | U34 | | | | |
| N/A | VCCAUX | V34 | | | | |
| N/A | VCCAUX | AL3 | | | | |
| N/A | VCCAUX | AL32 | | | | |
| N/A | VCCAUX | AM3 | | | | |
| N/A | VCCAUX | AM4 | | | | |
| N/A | VCCAUX | AM17 | | | | |
| N/A | VCCAUX | AM18 | | | | |
| N/A | VCCAUX | AM31 | | | | |
| N/A | VCCAUX | AM32 | | | | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| N/A | VCCINT | M12 | | |
| N/A | VCCINT | AD11 | | |
| N/A | VCCINT | L11 | | |
| N/A | VCCAUX | AN34 | | |
| N/A | VCCAUX | AG34 | | |
| N/A | VCCAUX | U34 | | |
| N/A | VCCAUX | H34 | | |
| N/A | VCCAUX | B34 | | |
| N/A | VCCAUX | AP33 | | |
| N/A | VCCAUX | A33 | | |
| N/A | VCCAUX | AP27 | | |
| N/A | VCCAUX | A27 | | |
| N/A | VCCAUX | AP17 | | |
| N/A | VCCAUX | A17 | | |
| N/A | VCCAUX | AP8 | | |
| N/A | VCCAUX | A8 | | |
| N/A | VCCAUX | AP2 | | |
| N/A | VCCAUX | A2 | | |
| N/A | VCCAUX | AN1 | | |
| N/A | VCCAUX | AG1 | | |
| N/A | VCCAUX | U1 | | |
| N/A | VCCAUX | H1 | | |
| N/A | VCCAUX | B1 | | |
| N/A | GND | AK34 | | |
| N/A | GND | AF34 | | |
| N/A | GND | AB34 | | |
| N/A | GND | W34 | | |
| N/A | GND | V34 | | |
| N/A | GND | T34 | | |
| N/A | GND | N34 | | |
| N/A | GND | J34 | | |
| N/A | GND | E34 | | |
| N/A | GND | AN33 | | |
| N/A | GND | B33 | | |
| N/A | GND | AM32 | | |
| N/A | GND | C32 | | |
| N/A | GND | AP30 | | |
| N/A | GND | AK30 | | |

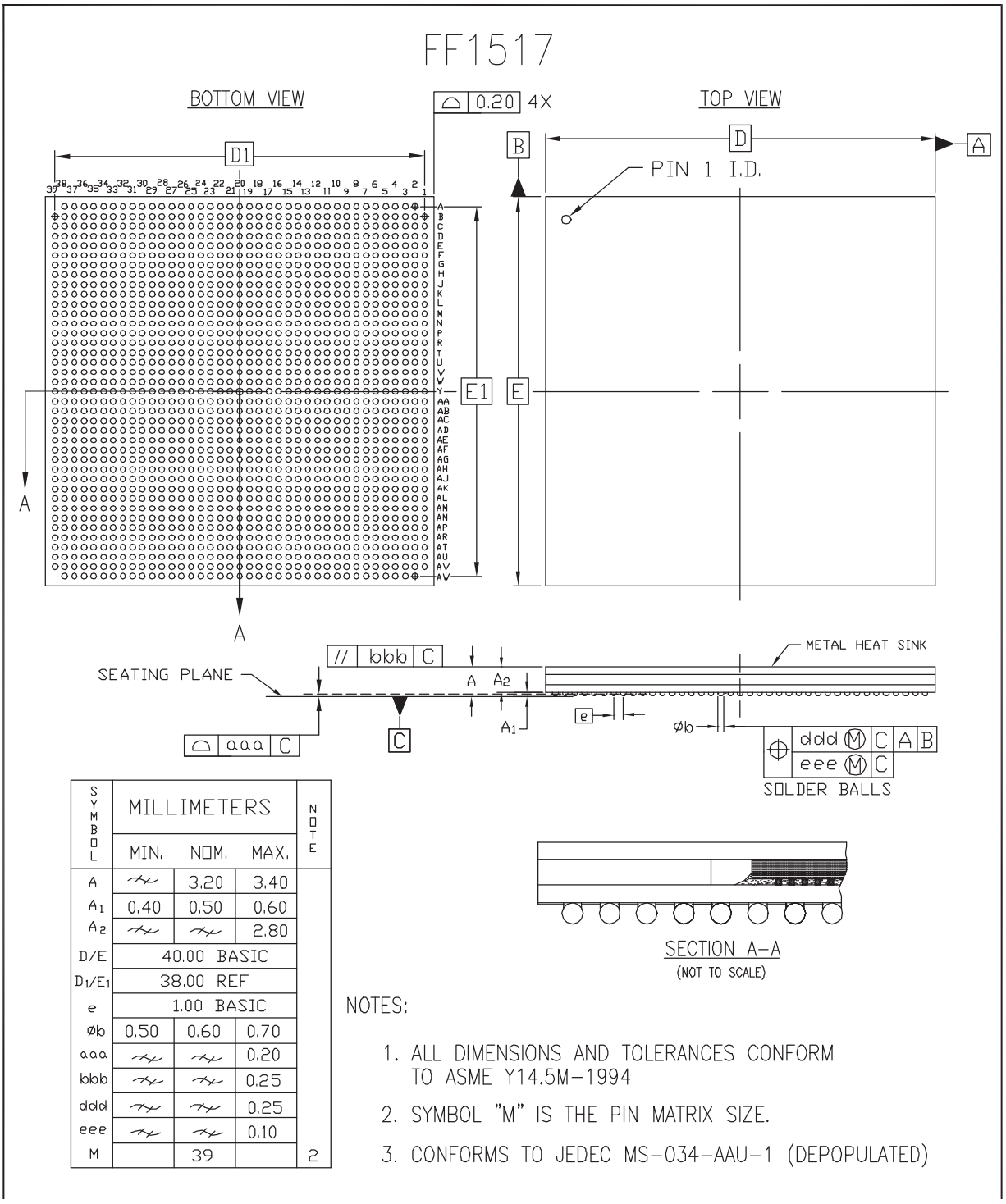
*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 3 | IO_L90P_3 | AA8 | | |
| 3 | IO_L89N_3 | Y11 | | |
| 3 | IO_L89P_3 | Y12 | | |
| 3 | IO_L88N_3 | AA5 | | |
| 3 | IO_L88P_3 | AA6 | | |
| 3 | IO_L87N_3/VREF_3 | AA3 | | |
| 3 | IO_L87P_3 | AA4 | | |
| 3 | IO_L86N_3 | Y13 | | |
| 3 | IO_L86P_3 | AA13 | | |
| 3 | IO_L85N_3 | AB7 | | |
| 3 | IO_L85P_3 | AB8 | | |
| 3 | IO_L60N_3 | AB5 | | |
| 3 | IO_L60P_3 | AB6 | | |
| 3 | IO_L59N_3 | AA9 | | |
| 3 | IO_L59P_3 | AA10 | | |
| 3 | IO_L58N_3 | AB3 | | |
| 3 | IO_L58P_3 | AB4 | | |
| 3 | IO_L57N_3/VREF_3 | AB1 | | |
| 3 | IO_L57P_3 | AB2 | | |
| 3 | IO_L56N_3 | AA11 | | |
| 3 | IO_L56P_3 | AA12 | | |
| 3 | IO_L55N_3 | AC5 | | |
| 3 | IO_L55P_3 | AC6 | | |
| 3 | IO_L54N_3 | AC1 | | |
| 3 | IO_L54P_3 | AC2 | | |
| 3 | IO_L53N_3 | AB9 | | |
| 3 | IO_L53P_3 | AB10 | | |
| 3 | IO_L52N_3 | AC8 | | |
| 3 | IO_L52P_3 | AD8 | | |
| 3 | IO_L51N_3/VREF_3 | AC4 | | |
| 3 | IO_L51P_3 | AD4 | | |
| 3 | IO_L50N_3 | AB11 | | |
| 3 | IO_L50P_3 | AB12 | | |
| 3 | IO_L49N_3 | AD6 | | |
| 3 | IO_L49P_3 | AD7 | | |
| 3 | IO_L48N_3 | AD2 | | |
| 3 | IO_L48P_3 | AD3 | | |
| 3 | IO_L47N_3 | AC9 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 7 | IO_L43N_7 | R37 | | |
| 7 | IO_L42P_7 | R34 | | |
| 7 | IO_L42N_7 | R35 | | |
| 7 | IO_L41P_7 | U28 | | |
| 7 | IO_L41N_7 | T28 | | |
| 7 | IO_L40P_7 | R32 | | |
| 7 | IO_L40N_7/VREF_7 | R33 | | |
| 7 | IO_L39P_7 | P38 | | |
| 7 | IO_L39N_7 | P39 | | |
| 7 | IO_L38P_7 | T29 | | |
| 7 | IO_L38N_7 | T30 | | |
| 7 | IO_L37P_7 | N37 | | |
| 7 | IO_L37N_7 | P37 | | |
| 7 | IO_L36P_7 | P35 | | |
| 7 | IO_L36N_7 | P36 | | |
| 7 | IO_L35P_7 | T27 | | |
| 7 | IO_L35N_7 | R27 | | |
| 7 | IO_L34P_7 | P33 | | |
| 7 | IO_L34N_7/VREF_7 | P34 | | |
| 7 | IO_L33P_7 | N38 | | |
| 7 | IO_L33N_7 | N39 | | |
| 7 | IO_L32P_7 | R28 | | |
| 7 | IO_L32N_7 | R29 | | |
| 7 | IO_L31P_7 | N35 | | |
| 7 | IO_L31N_7 | M36 | | |
| 7 | IO_L30P_7 | N33 | | |
| 7 | IO_L30N_7 | N34 | | |
| 7 | IO_L29P_7 | R30 | | |
| 7 | IO_L29N_7 | R31 | | |
| 7 | IO_L28P_7 | M37 | | |
| 7 | IO_L28N_7/VREF_7 | M38 | | |
| 7 | IO_L27P_7 | M33 | | |
| 7 | IO_L27N_7 | M34 | | |
| 7 | IO_L26P_7 | P28 | | |
| 7 | IO_L26N_7 | P29 | | |
| 7 | IO_L25P_7 | L38 | | |
| 7 | IO_L25N_7 | L39 | | |
| 7 | IO_L24P_7 | L36 | | |

## FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)




| SYMBOL | MILLIMETERS MIN. | NOM. | MAX. | NOTE |
|---|---|---|---|---|
| A | | 3.20 | 3.40 | |
| $A_1$ | 0.40 | 0.50 | 0.60 | |
| $A_2$ | | | 2.80 | |
| D/E | 40.00 BASIC | | | |
| $D_1/E_1$ | 38.00 REF | | | |
| e | 1.00 BASIC | | | |
| øb | 0.50 | 0.60 | 0.70 | |
| aaa | | | 0.20 | |
| bbb | | | 0.25 | |
| ddd | | | 0.25 | |
| eee | | | 0.10 | |
| M | | 39 | | 2 |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAU-1 (DEPOPULATED)

*Figure 8:* **FF1517 Flip-Chip Fine-Pitch BGA Package Specifications**

## FF1704 Flip-Chip Fine-Pitch BGA Package

As shown in Table 13, XC2VP70 and XC2VP100 Virtex-II Pro devices are available in the FF1704 flip-chip fine-pitch BGA package. Following this table are the FF1704 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 0 | IO_L01N_0/VRP_0 | | G34 | | |
| 0 | IO_L01P_0/VRN_0 | | H34 | | |
| 0 | IO_L02N_0 | | F34 | | |
| 0 | IO_L02P_0 | | E34 | | |
| 0 | IO_L03N_0 | | C34 | | |
| 0 | IO_L03P_0/VREF_0 | | D34 | | |
| 0 | IO_L05_0/No_Pair | | K32 | | |
| 0 | IO_L06N_0 | | H33 | | |
| 0 | IO_L06P_0 | | J33 | | |
| 0 | IO_L07N_0 | | F33 | | |
| 0 | IO_L07P_0 | | G33 | | |
| 0 | IO_L08N_0 | | E33 | | |
| 0 | IO_L08P_0 | | D33 | | |
| 0 | IO_L09N_0 | | H32 | | |
| 0 | IO_L09P_0/VREF_0 | | J32 | | |
| 0 | IO_L19N_0 | | E32 | | |
| 0 | IO_L19P_0 | | F32 | | |
| 0 | IO_L20N_0 | | C33 | | |
| 0 | IO_L20P_0 | | C32 | | |
| 0 | IO_L21N_0 | | K31 | | |
| 0 | IO_L21P_0 | | L31 | | |
| 0 | IO_L25N_0 | | H31 | | |
| 0 | IO_L25P_0 | | J31 | | |
| 0 | IO_L26N_0 | | G31 | | |
| 0 | IO_L26P_0 | | F31 | | |
| 0 | IO_L27N_0 | | D31 | | |
| 0 | IO_L27P_0/VREF_0 | | E31 | | |
| 0 | IO_L28N_0 | | L30 | | |
| 0 | IO_L28P_0 | | M30 | | |
| 0 | IO_L29N_0 | | J30 | | |
| 0 | IO_L29P_0 | | K30 | | |
| 0 | IO_L30N_0 | | G30 | | |
| 0 | IO_L30P_0 | | H30 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 5 | IO_L19P_5 | | AV32 | | |
| 5 | IO_L09N_5/VREF_5 | | AP32 | | |
| 5 | IO_L09P_5 | | AR32 | | |
| 5 | IO_L08N_5 | | AW33 | | |
| 5 | IO_L08P_5 | | AV33 | | |
| 5 | IO_L07N_5/VREF_5 | | AT33 | | |
| 5 | IO_L07P_5 | | AU33 | | |
| 5 | IO_L06N_5/VRP_5 | | AP33 | | |
| 5 | IO_L06P_5/VRN_5 | | AR33 | | |
| 5 | IO_L05_5/No_Pair | | AN32 | | |
| 5 | IO_L03N_5/D4 | | AW34 | | |
| 5 | IO_L03P_5/D5 | | AY34 | | |
| 5 | IO_L02N_5/D6 | | AV34 | | |
| 5 | IO_L02P_5/D7 | | AU34 | | |
| 5 | IO_L01N_5/RDWR_B | | AR34 | | |
| 5 | IO_L01P_5/CS_B | | AT34 | | |
| | | | | | |
| 6 | IO_L01P_6/VRN_6 | | AW37 | | |
| 6 | IO_L01N_6/VRP_6 | | AV37 | | |
| 6 | IO_L02P_6 | | AW36 | | |
| 6 | IO_L02N_6 | | AV36 | | |
| 6 | IO_L03P_6 | | AY37 | | |
| 6 | IO_L03N_6/VREF_6 | | AY38 | | |
| 6 | IO_L04P_6 | | AU36 | | |
| 6 | IO_L04N_6 | | AT37 | | |
| 6 | IO_L05P_6 | | AU35 | | |
| 6 | IO_L05N_6 | | AT35 | | |
| 6 | IO_L06P_6 | | AW41 | | |
| 6 | IO_L06N_6 | | AW42 | | |
| 6 | IO_L73P_6 | | AV41 | | |
| 6 | IO_L73N_6 | | AV42 | | |
| 6 | IO_L74P_6 | | AW40 | | |
| 6 | IO_L74N_6 | | AV40 | | |
| 6 | IO_L75P_6 | | AU39 | | |
| 6 | IO_L75N_6/VREF_6 | | AU40 | | |
| 6 | IO_L76P_6 | | AU41 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 7 | IO_L03P_7 | | D37 | | |
| 7 | IO_L03N_7 | | E37 | | |
| 7 | IO_L02P_7 | | D36 | | |
| 7 | IO_L02N_7 | | E36 | | |
| 7 | IO_L01P_7/VRN_7 | | C37 | | |
| 7 | IO_L01N_7/VRP_7 | | C38 | | |
| | | | | | |
| 0 | VCCO_0 | | D25 | | |
| 0 | VCCO_0 | | G23 | | |
| 0 | VCCO_0 | | G28 | | |
| 0 | VCCO_0 | | G32 | | |
| 0 | VCCO_0 | | J25 | | |
| 0 | VCCO_0 | | J29 | | |
| 0 | VCCO_0 | | P22 | | |
| 0 | VCCO_0 | | P23 | | |
| 0 | VCCO_0 | | P24 | | |
| 0 | VCCO_0 | | P25 | | |
| 0 | VCCO_0 | | P26 | | |
| 0 | VCCO_0 | | R22 | | |
| 0 | VCCO_0 | | R23 | | |
| 0 | VCCO_0 | | R24 | | |
| 0 | VCCO_0 | | R25 | | |
| 1 | VCCO_1 | | R21 | | |
| 1 | VCCO_1 | | R20 | | |
| 1 | VCCO_1 | | R19 | | |
| 1 | VCCO_1 | | R18 | | |
| 1 | VCCO_1 | | P21 | | |
| 1 | VCCO_1 | | P20 | | |
| 1 | VCCO_1 | | P19 | | |
| 1 | VCCO_1 | | P18 | | |
| 1 | VCCO_1 | | P17 | | |
| 1 | VCCO_1 | | J18 | | |
| 1 | VCCO_1 | | J14 | | |
| 1 | VCCO_1 | | G20 | | |
| 1 | VCCO_1 | | G15 | | |
| 1 | VCCO_1 | | G11 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| N/A | GND | | AU25 | | |
| N/A | GND | | AU18 | | |
| N/A | GND | | AU6 | | |
| N/A | GND | | AV38 | | |
| N/A | GND | | AV22 | | |
| N/A | GND | | AV21 | | |
| N/A | GND | | AV5 | | |
| N/A | GND | | AW39 | | |
| N/A | GND | | AW32 | | |
| N/A | GND | | AW28 | | |
| N/A | GND | | AW15 | | |
| N/A | GND | | AW11 | | |
| N/A | GND | | AW4 | | |
| N/A | GND | | AY42 | | |
| N/A | GND | | AY41 | | |
| N/A | GND | | AY40 | | |
| N/A | GND | | AY3 | | |
| N/A | GND | | AY2 | | |
| N/A | GND | | AY1 | | |
| N/A | GND | | BA42 | | |
| N/A | GND | | BA1 | | |
| N/A | GND | | AA38 | | |
| N/A | GND | | AA35 | | |
| N/A | GND | | AA32 | | |
| N/A | GND | | AA26 | | |
| N/A | GND | | AA25 | | |
| N/A | GND | | AA24 | | |
| N/A | GND | | AA23 | | |
| N/A | GND | | AA22 | | |
| N/A | GND | | AA21 | | |
| N/A | GND | | AA20 | | |
| N/A | GND | | AA19 | | |
| N/A | GND | | AA18 | | |
| N/A | GND | | AA17 | | |
| N/A | GND | | AA11 | | |
| N/A | GND | | AA8 | | |

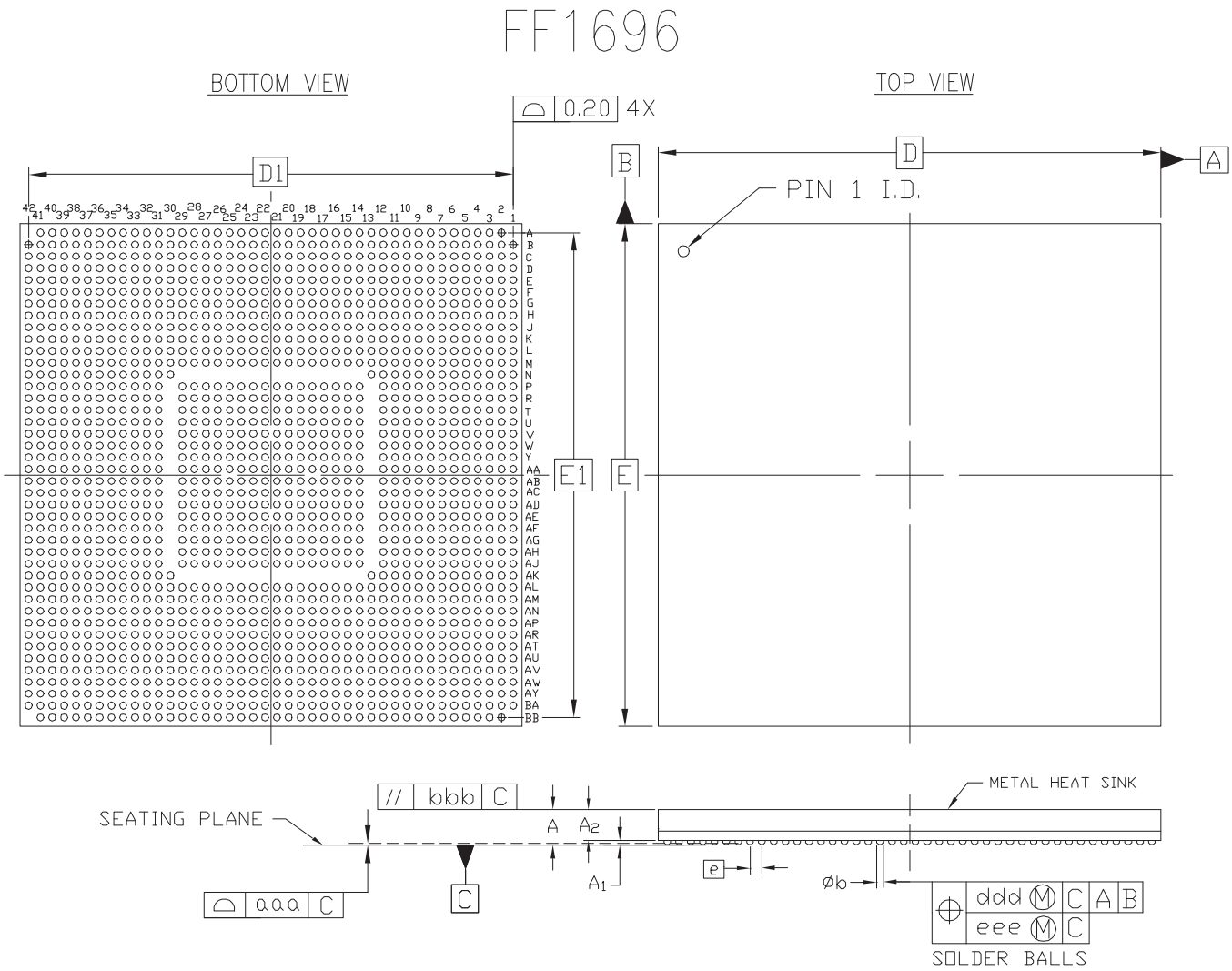
*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 5 | IO_L10N_5 | AW27 | NC |
| 5 | IO_L10P_5 | AW26 | NC |
| 5 | IO_L45N_5/VREF_5 | AN27 | |
| 5 | IO_L45P_5 | AP27 | |
| 5 | IO_L44N_5 | AU27 | |
| 5 | IO_L44P_5 | AV27 | |
| 5 | IO_L43N_5 | AR27 | |
| 5 | IO_L43P_5 | AR26 | |
| 5 | IO_L39N_5 | AL27 | |
| 5 | IO_L39P_5 | AM27 | |
| 5 | IO_L38N_5 | BA28 | |
| 5 | IO_L38P_5 | BB28 | |
| 5 | IO_L37N_5 | AY28 | |
| 5 | IO_L37P_5 | AY27 | |
| 5 | IO_L87N_5/VREF_5 | AN28 | |
| 5 | IO_L87P_5 | AP28 | |
| 5 | IO_L86N_5 | AU28 | |
| 5 | IO_L86P_5 | AV28 | |
| 5 | IO_L85N_5 | AT28 | |
| 5 | IO_L85P_5 | AT27 | |
| 5 | IO_L84N_5 | AL28 | |
| 5 | IO_L84P_5 | AM28 | |
| 5 | IO_L83_5/No_Pair | BA29 | |
| 5 | IO_L80_5/No_Pair | BB29 | |
| 5 | IO_L79N_5 | AY29 | |
| 5 | IO_L79P_5 | AW28 | |
| 5 | IO_L78N_5 | AN29 | |
| 5 | IO_L78P_5 | AP29 | |
| 5 | IO_L77N_5 | AU29 | |
| 5 | IO_L77P_5 | AV29 | |
| 5 | IO_L76N_5 | AT29 | |
| 5 | IO_L76P_5 | AR28 | |
| 5 | IO_L36N_5/VREF_5 | AL29 | |
| 5 | IO_L36P_5 | AM29 | |
| 5 | IO_L35N_5 | AY30 | |
| 5 | IO_L35P_5 | BA30 | |
| 5 | IO_L34N_5 | AT30 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 5 | VCCO_5 | AL30 | |
| 5 | VCCO_5 | AW29 | |
| 5 | VCCO_5 | AR29 | |
| 5 | VCCO_5 | AJ26 | |
| 5 | VCCO_5 | AW25 | |
| 5 | VCCO_5 | AR25 | |
| 5 | VCCO_5 | AJ25 | |
| 5 | VCCO_5 | AH25 | |
| 5 | VCCO_5 | AJ24 | |
| 5 | VCCO_5 | AH24 | |
| 5 | VCCO_5 | AJ23 | |
| 5 | VCCO_5 | AH23 | |
| 5 | VCCO_5 | AJ22 | |
| 5 | VCCO_5 | AH22 | |
| 4 | VCCO_4 | AJ21 | |
| 4 | VCCO_4 | AH21 | |
| 4 | VCCO_4 | AJ20 | |
| 4 | VCCO_4 | AH20 | |
| 4 | VCCO_4 | AJ19 | |
| 4 | VCCO_4 | AH19 | |
| 4 | VCCO_4 | AW18 | |
| 4 | VCCO_4 | AR18 | |
| 4 | VCCO_4 | AJ18 | |
| 4 | VCCO_4 | AH18 | |
| 4 | VCCO_4 | AJ17 | |
| 4 | VCCO_4 | AW14 | |
| 4 | VCCO_4 | AR14 | |
| 4 | VCCO_4 | AL13 | |
| 4 | VCCO_4 | AW10 | |
| 3 | VCCO_3 | AG15 | |
| 3 | VCCO_3 | AF15 | |
| 3 | VCCO_3 | AE15 | |
| 3 | VCCO_3 | AD15 | |
| 3 | VCCO_3 | AC15 | |
| 3 | VCCO_3 | AB15 | |
| 3 | VCCO_3 | AH14 | |
| 3 | VCCO_3 | AG14 | |

## FF1696 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)




| SYMBOL | MILLIMETERS | | | NOTE |
|---|---|---|---|---|
| | MIN. | NOM. | MAX. | |
| A | | 3.20 | 3.45 | |
| $A_1$ | 0.40 | 0.50 | 0.60 | |
| $A_2$ | | | 2.85 | |
| D/E | 42.50 BASIC | | | |
| $D_1/E_1$ | 41.00 REF | | | |
| e | 1.00 BASIC | | | |
| øb | 0.50 | 0.60 | 0.70 | |
| aaa | | | 0.20 | |
| bbb | | | 0.25 | |
| ddd | | | 0.25 | |
| eee | | | 0.10 | |
| M | | 42 | | 2 |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)

*Figure 10:* **FF1696 Flip-Chip Fine-Pitch BGA Package Specifications**