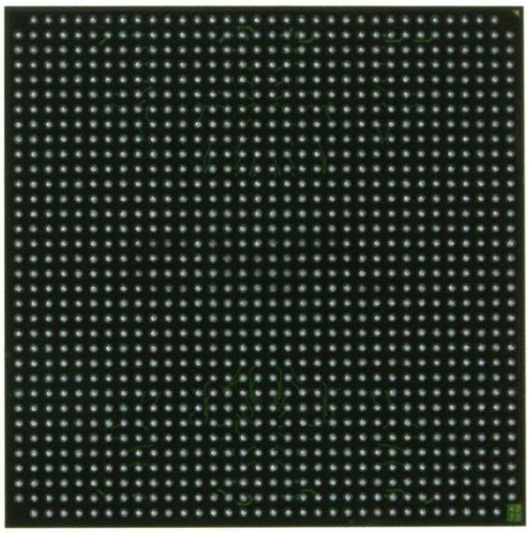

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2320
Number of Logic Elements/Cells	20880
Total RAM Bits	1622016
Number of I/O	564
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp20-6ffg1152i

- Programmable Receiver Equalization
- Internal AC Coupling
- On-Chip 50Ω Termination
  - Eliminates the need for external termination resistors
- Pre- and Post-Driver Serial and Parallel TX-to-RX Internal Loopback Modes for Testing Operability
- Programmable Comma Detection
  - Allows for any protocol
  - Allows for detection of any 10-bit character
- 8B/10B and 64B/66B Encoding Blocks

RocketIO Transceiver Features (All Except XC2VPX20 and XC2VPX70)

- Full-Duplex Serial Transceiver (SERDES) Capable of Baud Rates from 600 Mb/s to 3.125 Gb/s
- 100 Gb/s Duplex Data Rate (20 Channels)
- Monolithic Clock Synthesis and Clock Recovery (CDR)
- Fibre Channel, 10G Fibre Channel, Gigabit Ethernet, 10 Gb Attachment Unit Interface (XAUI), and Infiniband-Compliant Transceivers
- 8-, 16-, or 32-bit Selectable Internal FPGA Interface
- 8B/10B Encoder and Decoder (optional)
- 50Ω/75Ω on-chip Selectable Transmit and Receive Terminations
- Programmable Comma Detection
- Channel Bonding Support (from 2 to 20 Channels)
- Rate Matching via Insertion/Deletion Characters
- Four Levels of Selectable Pre-Emphasis
- Five Levels of Output Differential Voltage
- Per-Channel Internal Loopback Modes
- 2.5V Transceiver Supply Voltage

PowerPC RISC Processor Block Features (All Except XC2VP2)

- Embedded 300+ MHz Harvard Architecture Block
- Low Power Consumption: 0.9 mW/MHz
- Five-Stage Data Path Pipeline
- Hardware Multiply/Divide Unit
- Thirty-Two 32-bit General Purpose Registers
- 16 KB Two-Way Set-Associative Instruction Cache
- 16 KB Two-Way Set-Associative Data Cache
- Memory Management Unit (MMU)
  - 64-entry unified Translation Look-aside Buffers (TLB)
  - Variable page sizes (1 KB to 16 MB)
- Dedicated On-Chip Memory (OCM) Interface
- Supports IBM CoreConnect™ Bus Architecture
- Debug and Trace Support
- Timer Facilities

Virtex-II Pro Platform FPGA Technology (All Devices)

- SelectRAM+ Memory Hierarchy
  - Up to 8 Mb of True Dual-Port RAM in 18 Kb block SelectRAM+ resources
  - Up to 1,378 Kb of distributed SelectRAM+ resources
  - High-performance interfaces to external memory
- Arithmetic Functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible Logic Resources
  - Up to 88,192 internal registers/latches with Clock Enable
  - Up to 88,192 look-up tables (LUTs) or cascadable variable (1 to 16 bits) shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and Sum-of-Products support
  - Internal 3-state busing
- High-Performance Clock Management Circuitry
  - Up to twelve Digital Clock Manager (DCM) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers in all parts
- Active Interconnect Technology
  - Fourth-generation segmented routing structure
  - Fast, predictable routing delay, independent of fanout
  - Deep sub-micron noise immunity benefits
- SelectIO™-Ultra Technology
  - Up to 1,164 user I/Os
  - Twenty-two single-ended standards and ten differential standards
  - Programmable LVCMOS sink/source current (2 mA to 24 mA) per I/O
  - XCITE Digitally Controlled Impedance (DCI) I/O
  - PCI/PCI-X support (1)
  - Differential signaling
    - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
    - On-chip differential termination
    - Bus LVDS I/O

1. Refer to XAPP653 for more information.

- HSTL (1.5V and 1.8V, Class I, II, III, and IV)
- SSTL (1.8V and 2.5V, Class I and II)

The DCI I/O feature automatically provides on-chip termination for each single-ended I/O standard.

The IOB elements also support the following differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V)
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL (2.5V)

Two adjacent pads are used for each differential pair. Two or four IOBs connect to one switch matrix to access the routing resources. On-chip differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards.

Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F & G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM+ memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

Block SelectRAM+ Memory

The block SelectRAM+ memory resources are 18 Kb of True Dual-Port RAM, programmable from 16K x 1 bit to 512 x 36 bit, in various depth and width configurations. Each port is totally synchronous and independent, offering three "read-during-write" modes. Block SelectRAM+ memory is cascadable to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in Table 2.

Table 2: **Dual-Port and Single-Port Configurations**

16K x 1 bit	4K x 4 bits	1K x 18 bits
8K x 2 bits	2K x 9 bits	512 x 36 bits

18 X 18 Bit Multipliers

A multiplier block is associated with each SelectRAM+ memory block. The multiplier block is a dedicated 18 x 18-bit 2s complement signed multiplier, and is optimized for operations based on the block SelectRAM+ content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM+ resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM+ memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clock schemes.

Up to twelve DCM blocks are available. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90-, 180-, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of $^{1}/_{256}$ of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to a fractional or integer multiple of the input clock frequency. For exact timing parameters, see Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics.

Virtex-II Pro devices have 16 global clock MUX buffers, with up to eight clock nets per quadrant. Each clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM can send up to four of its clock outputs to global clock buffers on the same edge. Any global clock pin can drive any DCM on the same edge.

Routing Resources

The IOB, CLB, block SelectRAM+, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines, with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column, as well as massive secondary and local routing resources, provide fast interconnect. Virtex-II Pro buffered interconnects are relatively unaffected by net fanout, and the interconnect layout is designed to minimize crosstalk.

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

Boundary Scan

Boundary-scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II Pro devices, complying with IEEE standards 1149.1 and 1532. A system mode and a test mode are

Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description

DS083 (v5.0) June 21, 2011 **Product Specification**

Virtex-II Pro[1] Array Functional Description

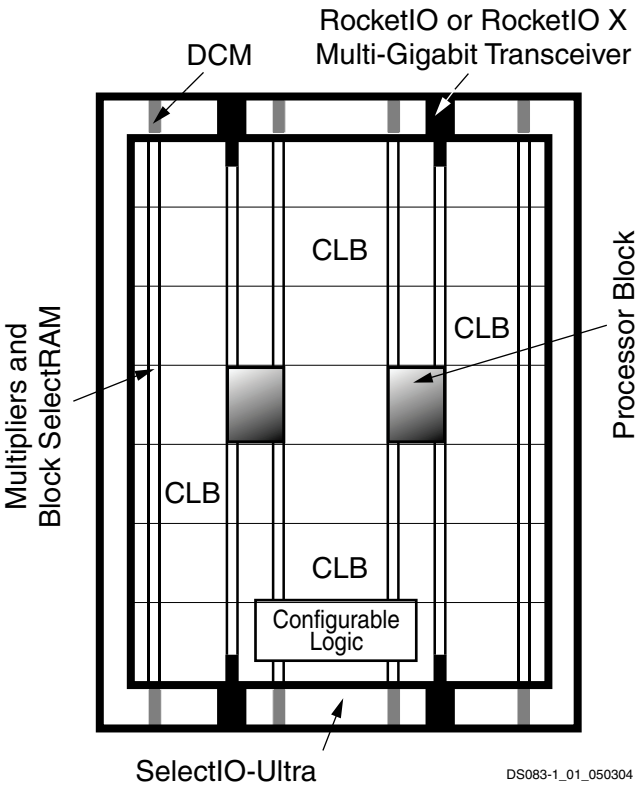

Figure 1: **Virtex-II Pro Generic Architecture Overview**

This module describes the following Virtex™-II Pro functional components, as shown in Figure 1:

- Embedded RocketIO™ (up to 3.125 Gb/s) or RocketIO X (up to 6.25 Gb/s) Multi-Gigabit Transceivers (MGTs)
- Processor blocks with embedded IBM PowerPC™ 405 RISC CPU core (PPC405) and integration circuitry.
- FPGA fabric based on Virtex-II architecture.

Virtex-II Pro User Guides

Virtex-II Pro User Guides cover theory of operation in more detail, and include implementation details, primitives and attributes, command/instruction sets, and many HDL code examples where appropriate. All parameter specifications are given only in Module 3 of this Data Sheet.

These User Guides are available:

- For detailed descriptions of PPC405 embedded core programming models and internal core operations, see **PowerPC Processor Reference Guide** and **PowerPC 405 Processor Block Reference Guide**.
- For detailed RocketIO transceiver digital/analog design considerations, see **RocketIO Transceiver User Guide**.
- For detailed RocketIO X transceiver digital/analog design considerations, see **RocketIO X Transceiver User Guide**,
- For detailed descriptions of the FPGA fabric (CLB, IOB, DCM, etc.), see **Virtex-II Pro Platform FPGA User Guide**.

All of the documents above, as well as a complete listing and description of Xilinx-developed Intellectual Property cores for Virtex-II Pro, are available on the Xilinx website.

Contents of This Module

Virtex-II Pro Compared to Virtex-II Devices

Virtex-II Pro devices are built on the Virtex-II FPGA architecture. Most FPGA features are identical to Virtex-II devices. Major differences are described below:

- The Virtex-II Pro FPGA family is the first to incorporate embedded PPC405 and RocketIO/RocketIO X cores.
- V_{CCAUX}, the auxiliary supply voltage, is 2.5V instead of 3.3V as for Virtex-II devices. Advanced processing at 0.13 µm has resulted in a smaller die, faster speed, and lower power consumption.
- Virtex-II Pro devices are neither bitstream-compatible nor pin-compatible with Virtex-II devices. However, Virtex-II designs can be compiled into Virtex-II Pro devices.
- On-chip input LVDS differential termination is available.
- SSTL3, AGP-2X/AGP, LVPECL_33, LVDS_33, and LVDSEXT_33 standards are not supported.
- The open-drain output pin TDO does not have an internal pull-up resistor.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

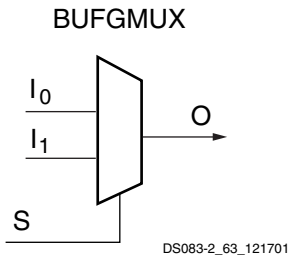

Figure 60: **Virtex-II Pro BUFGMUX Function**

If the presently selected clock is Low while S changes, or if it goes Low after S has changed, the output is kept Low until the other ("to-be-selected") clock has made a transition from High to Low. At that instant, the new clock starts driving the output.

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

All Virtex-II Pro devices have 16 global clock multiplexer buffers.

Figure 61 shows a switchover from I0 to I1.

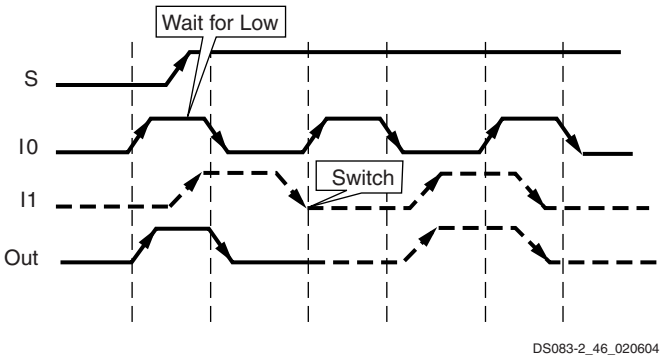

Figure 61: **Clock Multiplexer Waveform Diagram**

- The current clock is CLK0.
- S is activated High.
- If CLK0 is currently High, the multiplexer waits for CLK0 to go Low.
- Once CLK0 is Low, the multiplexer output stays Low until CLK1 transitions High to Low.
- When CLK1 transitions from High to Low, the output switches to CLK1.
- No glitches or short pulses can appear on the output.

Local Clocking

In addition to global clocks, there are local clock resources in the Virtex-II Pro devices. There are more than 72 local clocks in the Virtex-II Pro family. These resources can be used for many different applications, including but not limited to memory interfaces. For example, even using only the left and right I/O banks, Virtex-II Pro FPGAs can support up to 50 local clocks for DDR SDRAM. These interfaces can operate beyond 200 MHz on Virtex-II Pro devices.

Digital Clock Manager (DCM)

The Virtex-II Pro DCM offers a wide range of powerful clock management features.

- **Clock De-skew**: The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock, thus eliminating clock distribution delays.
- **Frequency Synthesis**: The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting**: The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four of the nine DCM clock outputs can drive inputs to global clock buffers or global clock multiplexer buffers simultaneously (see Figure 62). All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers.

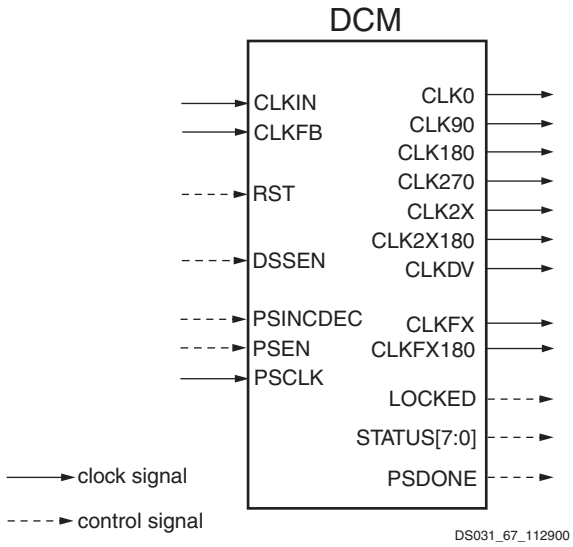

Figure 62: **Digital Clock Manager**

The DCM can be configured to delay the completion of the Virtex-II Pro configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Virtex-II Pro X			Virtex-II Pro			Units
		Min	Typ	Max	Min	Typ	Max	
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	1.25			1.25			V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0			2.0			V
I_{REF}	V_{REF} current per pin			10			10	µA
I_L	Input or output leakage current per pin (sample-tested)			10			10	µA
C_{IN}	Input capacitance (sample-tested)			10			10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0V, V_{CCO} = 2.5V (sample tested)			150			150	µA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 2.5V (sample-tested)			150			150	µA
I_{BATT} (1)	Battery supply current	Note (2)			Note (2)			nA
$I_{CCAUXTX}$	Operating AVCCAUXTX supply current		115			60	105	mA
$I_{CCAUXRX}$	Operating AVCCAUXRX supply current		85			35	75	mA
I_{TTX}	Operating I_{TTX} supply current when transmitter is AC-coupled		55			30		mA
	Operating I_{TTX} supply current when transmitter is DC-coupled	N/A	N/A	N/A		15		mA
I_{TRX}	Operating I_{TRX} supply current when receiver is AC-coupled		15			0		mA
	Operating I_{TRX} supply current when receiver is DC-coupled	N/A	N/A	N/A		15		
P_{CPU}	Power dissipation of PowerPC™ 405 processor block		0.9			0.9		mW/ MHz
P_{RXTX} (3)	Power dissipation of MGT @ 1.25 Gb/s per channel	N/A	N/A	N/A		230		mW
	Power dissipation of MGT @ 2.5 Gb/s per channel		290			310		mW
	Power dissipation of MGT @ 3.125 Gb/s per channel		310			350		mW
	Power dissipation of MGT @ 4.25 Gb/s per channel		450		N/A	N/A	N/A	mW
	Power dissipation of MGT @ 6.25 Gb/s per channel		525		N/A	N/A	N/A	mW

Notes:

1. Characterized, not tested.
2. Battery supply current (I_{BATT}):

	Device Unpowered	Device Powered	Units
25°C:	< 50	< 10	nA
85°C:	N/A	< 10	nA

3. Total dissipation of fully operational PMA and PCS combined. This power is the average power supply dissipation per MGT. The averaging was done by simultaneously turning on all eight transceivers and dividing the total power supply dissipation by eight.

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	GND	L11			
N/A	GND	L10			
N/A	GND	K9			
N/A	GND	K14			
N/A	GND	K13			
N/A	GND	K12			
N/A	GND	K11			
N/A	GND	K10			
N/A	GND	J9			
N/A	GND	J14			
N/A	GND	J13			
N/A	GND	J12			
N/A	GND	J11			
N/A	GND	J10			
N/A	GND	E5			
N/A	GND	E18			
N/A	GND	D4			
N/A	GND	D19			
N/A	GND	C3			
N/A	GND	C20			
N/A	GND	AB22			
N/A	GND	AB12			
N/A	GND	AB1			
N/A	GND	A22			
N/A	GND	A11			
N/A	GND	A1			

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
3	IO_L90N_3	P2			
3	IO_L90P_3	P3			
3	IO_L89N_3	P4			
3	IO_L89P_3	P5			
3	IO_L88N_3	P6			
3	IO_L88P_3	P7			
3	IO_L87N_3/VREF_3	R1			
3	IO_L87P_3	R2			
3	IO_L86N_3	R3			
3	IO_L86P_3	R4			
3	IO_L85N_3	R5			
3	IO_L85P_3	R6			
3	IO_L60N_3	P8	NC		
3	IO_L60P_3	R8	NC		
3	IO_L59N_3	T1	NC		
3	IO_L59P_3	T2	NC		
3	IO_L58N_3	T3	NC		
3	IO_L58P_3	T4	NC		
3	IO_L57N_3/VREF_3	T5	NC		
3	IO_L57P_3	T6	NC		
3	IO_L56N_3	R7	NC		
3	IO_L56P_3	T7	NC		
3	IO_L55N_3	T8	NC		
3	IO_L55P_3	U7	NC		
3	IO_L54N_3	U1	NC		
3	IO_L54P_3	V1	NC		
3	IO_L53N_3	U3	NC		
3	IO_L53P_3	U4	NC		
3	IO_L52N_3	U5	NC		
3	IO_L52P_3	U6	NC		
3	IO_L51N_3/VREF_3	V2	NC		
3	IO_L51P_3	V3	NC		
3	IO_L50N_3	V4	NC		
3	IO_L50P_3	V5	NC		
3	IO_L49N_3	V6	NC		
3	IO_L49P_3	V7	NC		

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
6	IO_L34P_6	AE30				
6	IO_L34N_6	AE31				
6	IO_L35P_6	AD27				
6	IO_L35N_6	AD28				
6	IO_L36P_6	AF33				
6	IO_L36N_6	AE33				
6	IO_L37P_6	AD29				
6	IO_L37N_6	AD30				
6	IO_L38P_6	AB25				
6	IO_L38N_6	AB26				
6	IO_L39P_6	AD31				
6	IO_L39N_6/VREF_6	AD32				
6	IO_L40P_6	AC28				
6	IO_L40N_6	AC29				
6	IO_L41P_6	AB27				
6	IO_L41N_6	AB28				
6	IO_L42P_6	AE34				
6	IO_L42N_6	AD34				
6	IO_L43P_6	AC31				
6	IO_L43N_6	AC32				
6	IO_L44P_6	AA25				
6	IO_L44N_6	AA26				
6	IO_L45P_6	AD33				
6	IO_L45N_6/VREF_6	AC33				
6	IO_L46P_6	AB29				
6	IO_L46N_6	AB30				
6	IO_L47P_6	AA27				
6	IO_L47N_6	AA28				
6	IO_L48P_6	AB31				
6	IO_L48N_6	AB32				
6	IO_L49P_6	AA29				
6	IO_L49N_6	AA30				
6	IO_L50P_6	Y25				
6	IO_L50N_6	Y26				
6	IO_L51P_6	AC34				
6	IO_L51N_6/VREF_6	AB34				
6	IO_L52P_6	AA31				
6	IO_L52N_6	AA32				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
7	VCCO_7	T23				
7	VCCO_7	U23				
N/A	CCLK	AE9				
N/A	PROG_B	J26				
N/A	DONE	AE10				
N/A	M0	AF26				
N/A	M1	AE26				
N/A	M2	AE25				
N/A	TCK	J9				
N/A	TDI	H28				
N/A	TDO	H7				
N/A	TMS	K10				
N/A	PWRDWN_B	AF9				
N/A	HSWAP_EN	K25				
N/A	RSVD	G8				
N/A	VBATT	K9				
N/A	DXP	K26				
N/A	DXN	G27				
N/A	AVCCAUXTX2	B32	NC	NC		
N/A	VTTXPAD2	B33	NC	NC		
N/A	TXNPAD2	A33	NC	NC		
N/A	TXPPAD2	A32	NC	NC		
N/A	GNDA2	C30	NC	NC		
N/A	RXPPAD2	A31	NC	NC		
N/A	RXNPAD2	A30	NC	NC		
N/A	VTRXPAD2	B31	NC	NC		
N/A	AVCCAUXRX2	B30	NC	NC		
N/A	AVCCAUXTX4	B28				
N/A	VTTXPAD4	B29				
N/A	TXNPAD4	A29				
N/A	TXPPAD4	A28				
N/A	GNDA4	C27				
N/A	RXPPAD4	A27				
N/A	RXNPAD4	A26				
N/A	VTRXPAD4	B27				
N/A	AVCCAUXRX4	B26				
N/A	AVCCAUXTX5	B24	NC	NC	NC	

FF1148 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, XC2VP40 and XC2VP50 Virtex-II Pro devices are available in the FF1148 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the FF1148 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L01N_0/VRP_0	E25		
0	IO_L01P_0/VRN_0	F25		
0	IO_L02N_0	J24		
0	IO_L02P_0	K24		
0	IO_L03N_0	C25		
0	IO_L03P_0/VREF_0	D25		
0	IO_L05_0/No_Pair	G25		
0	IO_L06N_0	A25		
0	IO_L06P_0	B25		
0	IO_L07N_0	G24		
0	IO_L07P_0	G23		
0	IO_L08N_0	H23		
0	IO_L08P_0	H22		
0	IO_L09N_0	E24		
0	IO_L09P_0/VREF_0	F24		
0	IO_L19N_0	C24		
0	IO_L19P_0	C23		
0	IO_L20N_0	J23		
0	IO_L20P_0	K23		
0	IO_L21N_0	A24		
0	IO_L21P_0	B24		
0	IO_L25N_0	E23		
0	IO_L25P_0	F23		
0	IO_L26N_0	K22		
0	IO_L26P_0	L22		
0	IO_L27N_0	D23		
0	IO_L27P_0/VREF_0	D22		
0	IO_L37N_0	A23		
0	IO_L37P_0	B23		
0	IO_L38N_0	J21		
0	IO_L38P_0	J20		
0	IO_L39N_0	F22		
0	IO_L39P_0	G22		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
3	IO_L90P_3	AA8		
3	IO_L89N_3	Y11		
3	IO_L89P_3	Y12		
3	IO_L88N_3	AA5		
3	IO_L88P_3	AA6		
3	IO_L87N_3/VREF_3	AA3		
3	IO_L87P_3	AA4		
3	IO_L86N_3	Y13		
3	IO_L86P_3	AA13		
3	IO_L85N_3	AB7		
3	IO_L85P_3	AB8		
3	IO_L60N_3	AB5		
3	IO_L60P_3	AB6		
3	IO_L59N_3	AA9		
3	IO_L59P_3	AA10		
3	IO_L58N_3	AB3		
3	IO_L58P_3	AB4		
3	IO_L57N_3/VREF_3	AB1		
3	IO_L57P_3	AB2		
3	IO_L56N_3	AA11		
3	IO_L56P_3	AA12		
3	IO_L55N_3	AC5		
3	IO_L55P_3	AC6		
3	IO_L54N_3	AC1		
3	IO_L54P_3	AC2		
3	IO_L53N_3	AB9		
3	IO_L53P_3	AB10		
3	IO_L52N_3	AC8		
3	IO_L52P_3	AD8		
3	IO_L51N_3/VREF_3	AC4		
3	IO_L51P_3	AD4		
3	IO_L50N_3	AB11		
3	IO_L50P_3	AB12		
3	IO_L49N_3	AD6		
3	IO_L49P_3	AD7		
3	IO_L48N_3	AD2		
3	IO_L48P_3	AD3		
3	IO_L47N_3	AC9		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L04P_6	AR33		
6	IO_L04N_6	AP33		
6	IO_L05P_6	AM32		
6	IO_L05N_6	AL31		
6	IO_L06P_6	AT34		
6	IO_L06N_6	AR34		
6	IO_L73P_6	AU35	NC	
6	IO_L73N_6	AT35	NC	
6	IO_L75P_6	AT38	NC	
6	IO_L75N_6/VREF_6	AT39	NC	
6	IO_L76P_6	AR37	NC	
6	IO_L76N_6	AR38	NC	
6	IO_L78P_6	AP38	NC	
6	IO_L78N_6	AP39	NC	
6	IO_L79P_6	AP36	NC	
6	IO_L79N_6	AP37	NC	
6	IO_L81P_6	AP35	NC	
6	IO_L81N_6/VREF_6	AN35	NC	
6	IO_L82P_6	AN38	NC	
6	IO_L82N_6	AN39	NC	
6	IO_L84P_6	AN36	NC	
6	IO_L84N_6	AN37	NC	
6	IO_L07P_6	AN33		
6	IO_L07N_6	AN34		
6	IO_L08P_6	AK31		
6	IO_L08N_6	AK32		
6	IO_L09P_6	AM37		
6	IO_L09N_6/VREF_6	AM38		
6	IO_L10P_6	AM36		
6	IO_L10N_6	AL35		
6	IO_L11P_6	AJ31		
6	IO_L11N_6	AH30		
6	IO_L12P_6	AM33		
6	IO_L12N_6	AM34		
6	IO_L13P_6	AL38		
6	IO_L13N_6	AL39		
6	IO_L14P_6	AH29		
6	IO_L14N_6	AG29		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	VCCO_7	P27		
7	VCCO_7	W26		
7	VCCO_7	V26		
7	VCCO_7	U26		
7	VCCO_7	T26		
7	VCCO_7	R26		
6	VCCO_6	AR39		
6	VCCO_6	AC37		
6	VCCO_6	AR36		
6	VCCO_6	AL36		
6	VCCO_6	AG36		
6	VCCO_6	AC33		
6	VCCO_6	AP32		
6	VCCO_6	AL32		
6	VCCO_6	AG32		
6	VCCO_6	AC29		
6	VCCO_6	AG28		
6	VCCO_6	AF27		
6	VCCO_6	AE26		
6	VCCO_6	AD26		
6	VCCO_6	AC26		
6	VCCO_6	AB26		
6	VCCO_6	AA26		
6	VCCO_6	Y26		
5	VCCO_5	AP27		
5	VCCO_5	AK27		
5	VCCO_5	AG26		
5	VCCO_5	AG25		
5	VCCO_5	AF25		
5	VCCO_5	AG24		
5	VCCO_5	AF24		
5	VCCO_5	AP23		
5	VCCO_5	AK23		
5	VCCO_5	AF23		
5	VCCO_5	AF22		
5	VCCO_5	AF21		
4	VCCO_4	AF19		
4	VCCO_4	AF18		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	IO_L48N_1		J17		
1	IO_L48P_1		H17		
1	IO_L47N_1		K17		
1	IO_L47P_1		L17		
1	IO_L46N_1		M17		
1	IO_L46P_1		M18		
1	IO_L45N_1/VREF_1		F16		
1	IO_L45P_1		E16		
1	IO_L44N_1		G16		
1	IO_L44P_1		H16		
1	IO_L43N_1		K16		
1	IO_L43P_1		J16		
1	IO_L39N_1		M16		
1	IO_L39P_1		L16		
1	IO_L38N_1		C15		
1	IO_L38P_1		C14		
1	IO_L37N_1		F15		
1	IO_L37P_1		E15		
1	IO_L87N_1/VREF_1		J15	NC	
1	IO_L87P_1		H15	NC	
1	IO_L86N_1		K15	NC	
1	IO_L86P_1		L15	NC	
1	IO_L85N_1		E14	NC	
1	IO_L85P_1		D14	NC	
1	IO_L84N_1		G14	NC	
1	IO_L84P_1		F14	NC	
1	IO_L83_1/No_Pair		H14	NC	
1	IO_L78N_1		L14	NC	
1	IO_L78P_1		K14	NC	
1	IO_L36N_1/VREF_1		M14		
1	IO_L36P_1		M15		
1	IO_L35N_1		C13		
1	IO_L35P_1		D13		
1	IO_L34N_1		F13		
1	IO_L34P_1		E13		
1	IO_L30N_1		H13		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L02P_2		D7		
2	IO_L03N_2		E6		
2	IO_L03P_2		D6		
2	IO_L04N_2/VREF_2		G6		
2	IO_L04P_2		F7		
2	IO_L05N_2		D3		
2	IO_L05P_2		E3		
2	IO_L06N_2		D1		
2	IO_L06P_2		D2		
2	IO_L73N_2		E1		
2	IO_L73P_2		E2		
2	IO_L74N_2		F4		
2	IO_L74P_2		F3		
2	IO_L75N_2		F1		
2	IO_L75P_2		F2		
2	IO_L76N_2/VREF_2		G3		
2	IO_L76P_2		G4		
2	IO_L77N_2		G2		
2	IO_L77P_2		G1		
2	IO_L78N_2		G5		
2	IO_L78P_2		H6		
2	IO_L79N_2		H4		
2	IO_L79P_2		H5		
2	IO_L80N_2		H3		
2	IO_L80P_2		H2		
2	IO_L81N_2		H7		
2	IO_L81P_2		J8		
2	IO_L82N_2/VREF_2		J6		
2	IO_L82P_2		J7		
2	IO_L83N_2		J5		
2	IO_L83P_2		J4		
2	IO_L84N_2		J1		
2	IO_L84P_2		J2		
2	IO_L07N_2		K9		
2	IO_L07P_2		L10		
2	IO_L08N_2		K6		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	TXPPAD11		A4		
N/A	GNDA11		C4		
N/A	RXPPAD11		A3		
N/A	RXNPAD11		A2		
N/A	VTRXPAD11		B3		
N/A	AVCCAUXRX11		B2		
N/A	AVCCAUXRX14		BA2		
N/A	VTRXPAD14		BA3		
N/A	RXNPAD14		BB2		
N/A	RXPPAD14		BB3		
N/A	GNDA14		AY4		
N/A	TXPPAD14		BB4		
N/A	TXNPAD14		BB5		
N/A	VTTXPAD14		BA5		
N/A	AVCCAUXTX14		BA4		
N/A	AVCCAUXRX15		BA6		
N/A	VTRXPAD15		BA7		
N/A	RXNPAD15		BB6		
N/A	RXPPAD15		BB7		
N/A	GNDA15		AY8		
N/A	TXPPAD15		BB8		
N/A	TXNPAD15		BB9		
N/A	VTTXPAD15		BA9		
N/A	AVCCAUXTX15		BA8		
N/A	AVCCAUXRX16		BA10		
N/A	VTRXPAD16		BA11		
N/A	RXNPAD16		BB10		
N/A	RXPPAD16		BB11		
N/A	GNDA16		AY12		
N/A	TXPPAD16		BB12		
N/A	TXNPAD16		BB13		
N/A	VTTXPAD16		BA13		
N/A	AVCCAUXTX16		BA12		
N/A	AVCCAUXRX17		BA14		
N/A	VTRXPAD17		BA15		
N/A	RXNPAD17		BB14		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L06N_3	BA8	
3	IO_L06P_3	BB8	
3	IO_L05N_3	AW8	
3	IO_L05P_3	AW9	
3	IO_L04N_3	BA7	
3	IO_L04P_3	BB7	
3	IO_L03N_3/VREF_3	BA6	
3	IO_L03P_3	BB6	
3	IO_L02N_3	AY9	
3	IO_L02P_3	BA9	
3	IO_L01N_3/VRP_3	BA4	
3	IO_L01P_3/VRN_3	BB4	
4	IO_L01N_4/BUSY/DOUT(1)	AL11	
4	IO_L01P_4/INIT_B	AL12	
4	IO_L02N_4/D0/DIN(1)	AV10	
4	IO_L02P_4/D1	AU10	
4	IO_L03N_4/D2	AN11	
4	IO_L03P_4/D3	AM11	
4	IO_L05_4/No_Pair	AT10	
4	IO_L06N_4/VRP_4	AY11	
4	IO_L06P_4/VRN_4	AY10	
4	IO_L07N_4	BB10	
4	IO_L07P_4/VREF_4	BA10	
4	IO_L08N_4	AU11	
4	IO_L08P_4	AT11	
4	IO_L09N_4	AR11	
4	IO_L09P_4/VREF_4	AP11	
4	IO_L19N_4	AW11	
4	IO_L19P_4	AV11	
4	IO_L20N_4	BB11	
4	IO_L20P_4	BA11	
4	IO_L21N_4	AN12	
4	IO_L21P_4	AM12	
4	IO_L25N_4	AR13	
4	IO_L25P_4	AT12	
4	IO_L26N_4	AV12	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L52P_6	AF40	
6	IO_L52N_6	AF41	
6	IO_L53P_6	AC36	
6	IO_L53N_6	AC37	
6	IO_L54P_6	AE41	
6	IO_L54N_6	AE42	
6	IO_L55P_6	AE40	
6	IO_L55N_6	AD40	
6	IO_L56P_6	AC31	
6	IO_L56N_6	AC32	
6	IO_L57P_6	AE38	
6	IO_L57N_6/VREF_6	AE39	
6	IO_L58P_6	AD41	
6	IO_L58N_6	AD42	
6	IO_L59P_6	AB35	
6	IO_L59N_6	AB36	
6	IO_L60P_6	AD37	
6	IO_L60N_6	AD38	
6	IO_L85P_6	AC40	
6	IO_L85N_6	AC41	
6	IO_L86P_6	AB33	
6	IO_L86N_6	AB34	
6	IO_L87P_6	AC39	
6	IO_L87N_6/VREF_6	AB39	
6	IO_L88P_6	AB40	
6	IO_L88N_6	AB41	
6	IO_L89P_6	AB31	
6	IO_L89N_6	AB32	
6	IO_L90P_6	AB37	
6	IO_L90N_6	AB38	
7	IO_L90P_7	AA40	
7	IO_L90N_7	AA41	
7	IO_L89P_7	AA35	
7	IO_L89N_7	AA36	
7	IO_L88P_7	Y39	
7	IO_L88N_7/VREF_7	AA39	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	M2	AM33	
N/A	TCK	K10	
N/A	TDI	M32	
N/A	TDO	M11	
N/A	TMS	L10	
N/A	PWRDWN_B	AP10	
N/A	HSWAP_EN	K33	
N/A	RSVD	J10	
N/A	VBATT	M12	
N/A	DXP	M31	
N/A	DXN	L33	
N/A	VCCINT	AK30	
N/A	VCCINT	N30	
N/A	VCCINT	AJ29	
N/A	VCCINT	P29	
N/A	VCCINT	AJ28	
N/A	VCCINT	AH28	
N/A	VCCINT	R28	
N/A	VCCINT	P28	
N/A	VCCINT	AJ27	
N/A	VCCINT	AH27	
N/A	VCCINT	AG27	
N/A	VCCINT	AF27	
N/A	VCCINT	AE27	
N/A	VCCINT	AD27	
N/A	VCCINT	AC27	
N/A	VCCINT	AB27	
N/A	VCCINT	AA27	
N/A	VCCINT	Y27	
N/A	VCCINT	W27	
N/A	VCCINT	V27	
N/A	VCCINT	U27	
N/A	VCCINT	T27	
N/A	VCCINT	R27	
N/A	VCCINT	P27	
N/A	VCCINT	AH26	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	E13	
N/A	GND	A13	
N/A	GND	AD12	
N/A	GND	W12	
N/A	GND	BB9	
N/A	GND	AV9	
N/A	GND	AP9	
N/A	GND	AK9	
N/A	GND	AF9	
N/A	GND	AC9	
N/A	GND	Y9	
N/A	GND	U9	
N/A	GND	N9	
N/A	GND	J9	
N/A	GND	E9	
N/A	GND	A9	
N/A	GND	BB5	
N/A	GND	AV5	
N/A	GND	AP5	
N/A	GND	AK5	
N/A	GND	AF5	
N/A	GND	AC5	
N/A	GND	Y5	
N/A	GND	U5	
N/A	GND	N5	
N/A	GND	J5	
N/A	GND	E5	
N/A	GND	A5	
N/A	GND	BA3	
N/A	GND	B3	
N/A	GND	BA2	
N/A	GND	AY2	
N/A	GND	C2	
N/A	GND	B2	
N/A	GND	AV1	
N/A	GND	AP1	
N/A	GND	AK1	