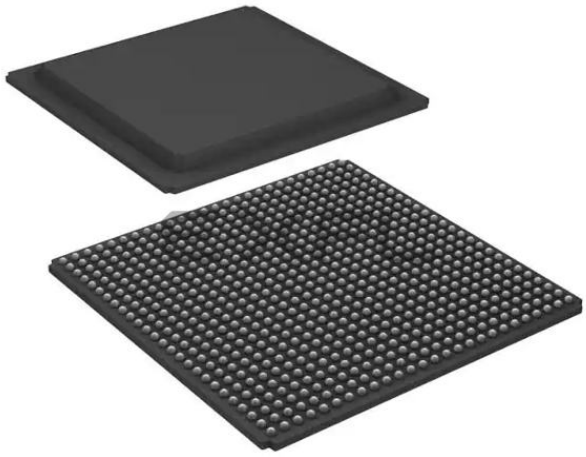

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2320
Number of Logic Elements/Cells	20880
Total RAM Bits	1622016
Number of I/O	404
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp20-6fg676i

implemented. In system mode, a Virtex-II Pro device will continue to function while executing non-test Boundary-Scan instructions. In test mode, Boundary-Scan test instructions control the I/O pins for testing purposes. The Virtex-II Pro Test Access Port (TAP) supports BYPASS, PRELOAD, SAMPLE, IDCODE, and USERCODE non-test instructions. The EXTEST, INTEST, and HIGHZ test instructions are also supported.

Configuration

Virtex-II Pro / Virtex-II Pro devices are configured by loading the bitstream into internal configuration memory using one of the following modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532)

A Data Encryption Standard (DES) decryptor is available on-chip to secure the bitstreams. One or two triple-DES key sets can be used to optionally encrypt the configuration data.

The Xilinx System Advanced Configuration Enviornment (System ACE) family offers high-capacity and flexible solution for FPGA configuration as well as program/data storage for the processor. See **DS080**, *System ACE CompactFlash Solution* for more information.

Readback and Integrated Logic Analyzer

Configuration data stored in Virtex-II Pro / Virtex-II Pro configuration memory can be read back for verification. Along with the configuration data, the contents of all flip-flops and latches, distributed SelectRAM+, and block SelectRAM+ memory resources can be read back. This capability is useful for real-time debugging.

The Xilinx ChipScope Integrated Logic Analyzer (ILA) cores and Integrated Bus Analyzer (IBA) cores, along with the ChipScope Pro Analyzer software, provide a complete solution for accessing and verifying user designs within Virtex-II Pro devices.

IP Core and Reference Support

Intellectual Property is part of the Platform FPGA solution. In addition to the existing FPGA fabric cores, the list below shows some of the currently available hardware and software intellectual properties specially developed for Virtex-II Pro / Virtex-II Pro X by Xilinx. Each IP core is modular, portable, Real-Time Operating System (RTOS) independent, and CoreConnect compatible for ease of design migration. Refer to **www.xilinx.com/ipcenter** for the latest and most complete list of cores.

Hardware Cores

- Bus Infrastructure cores (arbiters, bridges, and more)
- Memory cores (DDR, Flash, and more)
- Peripheral cores (UART, IIC, and more)
- Networking cores (ATM, Ethernet, and more)

Software Cores

- Boot code
- Test code
- Device drivers
- Protocol stacks
- RTOS integration
- Customized board support package

The top half of the figure shows the transmission of words split across four transceivers (channels or lanes). PPPP, QQQQ, RRRR, SSSS, and TTTT represent words sent over the four channels.

The bottom-left portion of Figure 13 shows the initial situation in the FPGA's receivers at the other end of the four channels. Due to variations in transmission delay—especially if the channels are routed through repeaters—the FPGA fabric might not correctly assemble the bytes into complete words. The bottom-left illustration shows the incorrect assembly of data words PQPP, QRQQ, RSRR, and so forth.

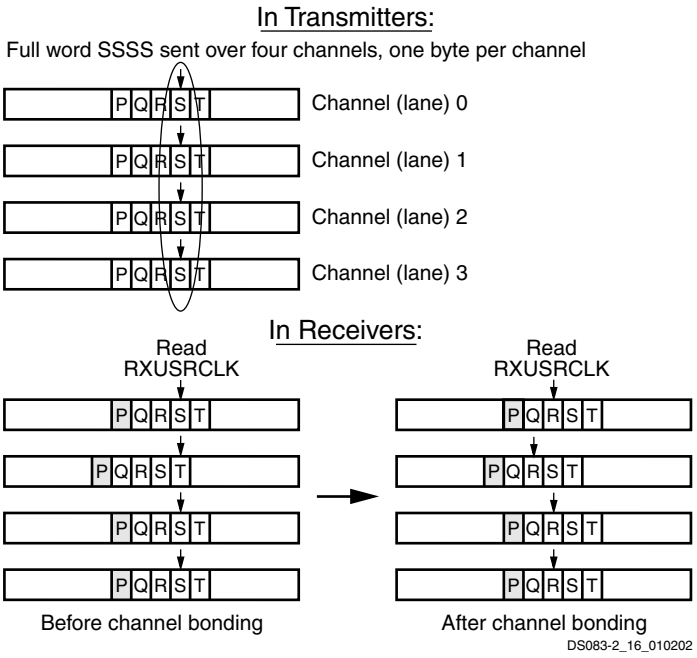

Figure 13: **Channel Bonding (Alignment)**

To support correction of this misalignment, the data stream includes special byte sequences that define corresponding points in the several channels. In the bottom half of Figure 13, the shaded "P" bytes represent these special characters. Each receiver recognizes the "P" channel bonding character, and remembers its location in the buffer. At some point, one transceiver designated as the master instructs all the transceivers to align to the channel bonding character "P" (or to some location relative to the channel bonding character).

After this operation, words transmitted to the FPGA fabric are properly aligned: RRRR, SSSS, TTTT, and so forth, as shown in the bottom-right portion of Figure 13. To ensure that the channels remain properly aligned following the channel bonding operation, the master transceiver must also control the clock correction operations described in the previous section for all channel-bonded transceivers.

Transmitter Buffer

The transmitter's buffer write pointer (TXUSRCLK) is frequency-locked to its read pointer (REFCLK). Therefore, clock correction and channel bonding are not required. The purpose of the transmitter's buffer is to accommodate a phase difference between TXUSRCLK and REFCLK. A simple FIFO suffices for this purpose. A FIFO depth of four will permit reliable operation with simple detection of overflow or underflow, which could occur if the clocks are not frequency-locked.

RocketIO Configuration

This section outlines functions that can be selected or controlled by configuration. Xilinx implementation software supports 16 transceiver primitives, as shown in Table 6.

Each of the primitives in Table 6 defines default values for the configuration attributes, allowing some number of them to be modified by the user. Refer to the ***RocketIO Transceiver User Guide*** for more details.

Table 6: **Supported RocketIO MGT Protocol Primitives**

GT_CUSTOM	Fully customizable by user
GT_FIBRE_CHAN_1	Fibre Channel, 1-byte data path
GT_FIBRE_CHAN_2	Fibre Channel, 2-byte data path
GT_FIBRE_CHAN_4	Fibre Channel, 4-byte data path
GT_ETHERNET_1	Gigabit Ethernet, 1-byte data path
GT_ETHERNET_2	Gigabit Ethernet, 2-byte data path
GT_ETHERNET_4	Gigabit Ethernet, 4-byte data path
GT_XAUI_1	10-gigabit Ethernet, 1-byte data path
GT_XAUI_2	10-gigabit Ethernet, 2-byte data path
GT_XAUI_4	10-gigabit Ethernet, 4-byte data path
GT_INFINIBAND_1	Infiniband, 1-byte data path
GT_INFINIBAND_2	Infiniband, 2-byte data path
GT_INFINIBAND_4	Infiniband, 4-byte data path
GT_AURORA_1(1)	1-byte data path
GT_AURORA_2(1)	2-byte data path
GT_AURORA_4(1)	4-byte data path

Notes:
1. For more information on the Aurora protocol, visit http://www.xilinx.com.

Other RocketIO Features and Notes

CRC

The RocketIO transceiver CRC logic supports the 32-bit invariant CRC calculation used by Infiniband, FibreChannel, and Gigabit Ethernet.

On the transmitter side, the CRC logic recognizes where the CRC bytes should be inserted and replaces four placeholder bytes at the tail of a data packet with the computed CRC. For Gigabit Ethernet and FibreChannel, transmitter

Table 9: **Supported Differential Signal I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Output V_{OD}
LDT_25	2.5	N/R	N/R	0.500 – 0.740
LVDS_25	2.5	N/R	N/R	0.247 – 0.454
LVDSEXT_25	2.5	N/R	N/R	0.440 – 0.820
BLVDS_25	2.5	N/R	N/R	0.250 – 0.450
ULVDS_25	2.5	N/R	N/R	0.500 – 0.740
LVPECL_25	2.5	N/R	N/R	0.345 – 1.185
LDT_25_DT(1)	2.5	2.5	N/R	0.500 – 0.740
LVDS_25_DT(1)	2.5	2.5	N/R	0.247 – 0.454
LVDSEXT_25_DT(1)	2.5	2.5	N/R	0.330 – 0.700
ULVDS_25_DT(1)	2.5	2.5	N/R	0.500 – 0.740

Notes:
1. These standards support on-chip 100Ω termination.
2. N/R = no requirement.

Table 10: **Supported DCI I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Termination Type
LVDCI_33(1)	3.3	3.3	N/R	Series
LVDCI_25	2.5	2.5	N/R	Series
LVDCI_DV2_25	2.5	2.5	N/R	Series
LVDCI_18	1.8	1.8	N/R	Series
LVDCI_DV2_18	1.8	1.8	N/R	Series
LVDCI_15	1.5	1.5	N/R	Series
LVDCI_DV2_15	1.5	1.5	N/R	Series
GTL_DCI	1.2	1.2	0.8	Single
GTLP_DCI	1.5	1.5	1.0	Single
HSTL_I_DCI	1.5	1.5	0.75	Split
HSTL_II_DCI	1.5	1.5	0.75	Split
HSTL_III_DCI	1.5	1.5	0.9	Single
HSTL_IV_DCI	1.5	1.5	0.9	Single
HSTL_I_DCI_18	1.8	1.8	0.9	Split
HSTL_II_DCI_18	1.8	1.8	0.9	Split
HSTL_III_DCI_18	1.8	1.8	1.1	Single
HSTL_IV_DCI_18	1.8	1.8	1.1	Single
SSTL2_I_DCI(2)	2.5	2.5	1.25	Split
SSTL2_II_DCI(2)	2.5	2.5	1.25	Split
SSTL18_I_DCI (3)	1.8	1.8	0.9	Split
SSTL18_II_DCI	1.8	1.8	0.9	Split

Table 10: **Supported DCI I/O Standards *(Continued)***

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Termination Type
LVDS_25_DCI	2.5	2.5	N/R	Split
LVDSEXT_25_DCI	2.5	2.5	N/R	Split

Notes:
1. LVDCI_XX is LVCMOS output controlled impedance buffers, matching all or half of the reference resistors.
2. These are SSTL compatible.
3. SSTL18_I is not a JEDEC-supported standard.
4. N/R = no requirement.

Logic Resources

IOB blocks include six storage elements, as shown in Figure 19.

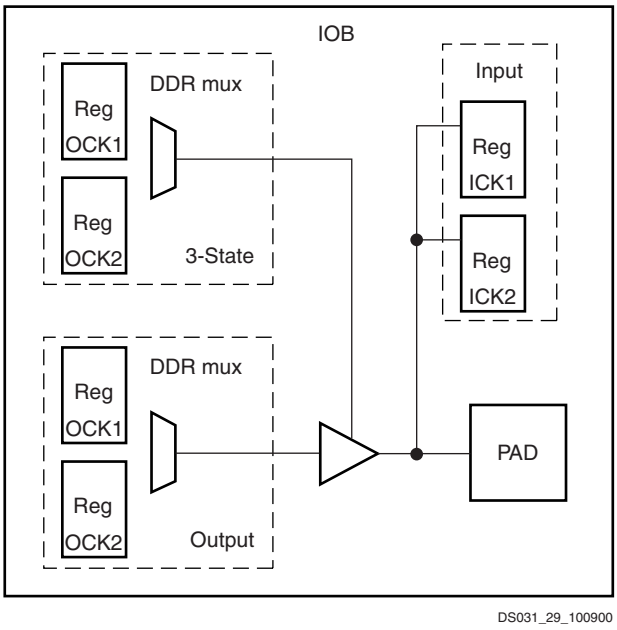

Figure 19: **Virtex-II Pro IOB Block**

Each storage element can be configured either as an edge-triggered D-type flip-flop or as a level-sensitive latch. On the input, output, and 3-state path, one or two DDR registers can be used.

Double data rate is directly accomplished by the two registers on each path, clocked by the rising edges (or falling edges) from two different clock nets. The two clock signals are generated by the DCM and must be 180 degrees out of phase, as shown in Figure 20. There are two input, output, and 3-state data signals, each being alternately clocked out.

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 39. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous; however, the storage element or flip-flop is available to implement a synchronous read. Any of the 16 bits can be read out asynchronously by varying the address. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

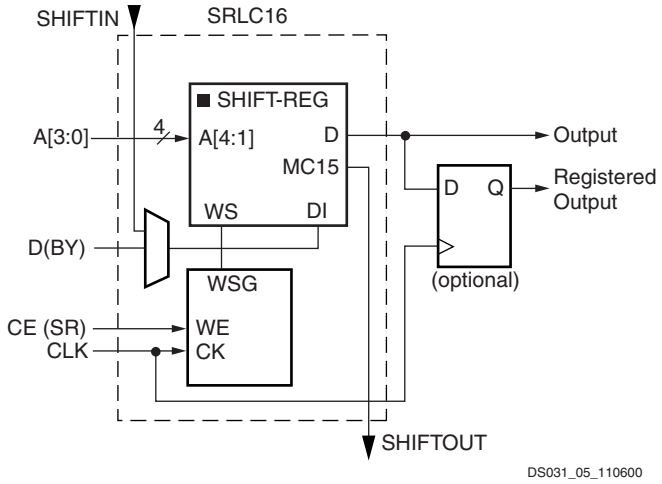

Figure 39: **Shift Register Configurations**

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See Figure 40.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

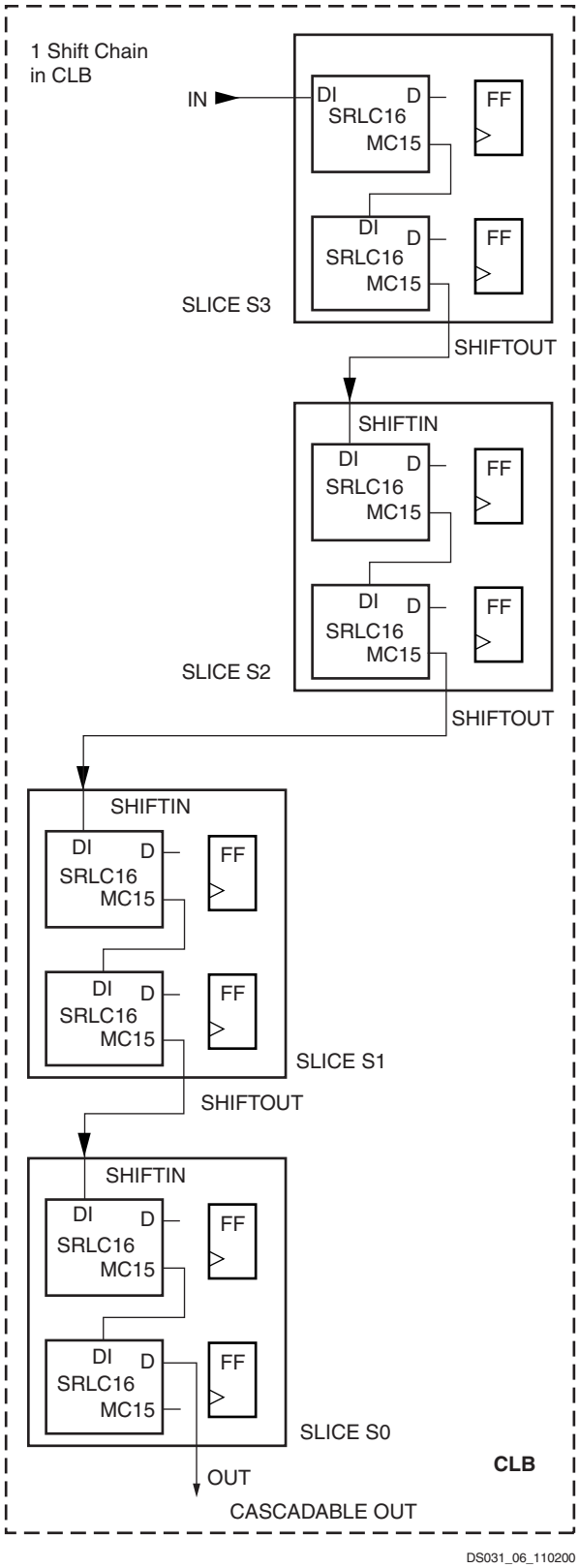

Figure 40: **Cascadable Shift Register**

Virtex-II Pro Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM

Table 53: **Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
LVCMOS25 Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 28.						
Global Clock and OFF with DCM	$T_{ICKOFDCM}$	XC2VP2	1.55	1.59	1.62	ns
		XC2VP4	1.58	1.61	1.65	ns
		XC2VP7	1.63	1.68	1.72	ns
		XC2VP20	1.68	1.74	1.79	ns
		XC2VPX20	1.68	1.74	1.79	ns
		XC2VP30	1.68	1.75	1.80	ns
		XC2VP40	1.71	1.86	1.92	ns
		XC2VP50	1.80	2.00	2.07	ns
		XC2VP70	1.87	2.07	2.24	ns
		XC2VPX70	1.87	2.07	2.24	ns
		XC2VP100	N/A	2.38	2.45	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 6. For other I/O standards, see Table 40.
3. DCM output jitter is already included in the timing calculation.

Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *Without* DCM

Table 54: **Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *Without* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
LVCMOS25 Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 28.						
Global Clock and OFF without DCM	T_{ICKOF}	XC2VP2	3.19	3.52	3.82	ns
		XC2VP4	3.39	3.91	4.27	ns
		XC2VP7	3.59	4.00	4.36	ns
		XC2VP20	3.62	4.08	4.46	ns
		XC2VPX20	3.62	4.08	4.46	ns
		XC2VP30	3.73	4.12	4.50	ns
		XC2VP40	3.89	4.28	4.67	ns
		XC2VP50	4.00	4.43	4.84	ns
		XC2VP70	4.38	4.87	5.33	ns
		XC2VPX70	4.38	4.87	5.33	ns
		XC2VP100	N/A	5.32	5.82	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 6. For other I/O standards, see Table 40.
3. DCM output jitter is already included in the timing calculation.

Table 3: **Virtex-II Pro Available I/Os and RocketIO MGT Pins per Device/Package Combination *(Continued)***

Virtex-II Pro Device	User I/Os & RocketIO MGT Pins	Virtex-II Pro Package[1]									
		FG256/ FGG256	FG456/ FGG456	FG676/ FGG456	FF672	FF896	FF1152	FF1148	FF1517	FF1704	FF1696
XC2VP70	Available User I/Os	-	-		-	-	-	-	964	996	-
	RocketIO MGT Pins	-	-		-	-	-	-	144	180	-
	Differential I/O Pairs	-	-		-	-	-	-	476	492	-
XC2VPX70	**Available User I/Os**	**-**	**-**		**-**	**-**	**-**	**-**	**-**	**992**	**-**
	RocketIO X MGT Pins	**-**	**-**		**-**	**-**	**-**	**-**	**-**	**180**	**-**
	Differential I/O Pairs	**-**	**-**		**-**	**-**	**-**	**-**	**-**	**490**	**-**
XC2VP100	Available User I/Os	-	-		-	-	-	-	-	1040	1164
	RocketIO MGT Pins	-	-		-	-	-	-	-	180	0
	Differential I/O Pairs	-	-		-	-	-	-	-	512	572

Notes:
1. Wire-bond packages include FGG*nnn* Pb-free versions. See Virtex-II Pro Ordering Examples (Module 1)

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
4	IO_L05_4/No_Pair	Y8			
4	IO_L06N_4/VRP_4	AB8			
4	IO_L06P_4/VRN_4	AB9			
4	IO_L07N_4	AC8			
4	IO_L07P_4/VREF_4	AD8			
4	IO_L08N_4	AE8			
4	IO_L08P_4	AF8			
4	IO_L09N_4	Y9			
4	IO_L09P_4/VREF_4	AA9			
4	IO_L37N_4	AC9	NC	NC	
4	IO_L37P_4	AD9	NC	NC	
4	IO_L38N_4	Y10	NC	NC	
4	IO_L38P_4	W11	NC	NC	
4	IO_L39N_4	AA10	NC	NC	
4	IO_L39P_4	AA11	NC	NC	
4	IO_L43N_4	AB10	NC	NC	
4	IO_L43P_4	AC10	NC	NC	
4	IO_L44N_4	Y11	NC	NC	
4	IO_L44P_4	Y12	NC	NC	
4	IO_L45N_4	AB11	NC	NC	
4	IO_L45P_4/VREF_4	AC11	NC	NC	
4	IO_L67N_4	AA12			
4	IO_L67P_4	AB12			
4	IO_L68N_4	AC12			
4	IO_L68P_4	AD12			
4	IO_L69N_4	W12			
4	IO_L69P_4/VREF_4	W13			
4	IO_L73N_4	Y13			
4	IO_L73P_4	AA13			
4	IO_L74N_4/GCLK3S	AB13			
4	IO_L74P_4/GCLK2P	AC13			
4	IO_L75N_4/GCLK1S	AD13			
4	IO_L75P_4/GCLK0P	AE13			
5	IO_L75N_5/GCLK7S	AE14			
5	IO_L75P_5/GCLK6P	AD14			
5	IO_L74N_5/GCLK5S	AC14			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	VCCO_7	L18			
7	VCCO_7	M18			
7	VCCO_7	N18			
N/A	CCLK	W7			
N/A	PROG_B	D22			
N/A	DONE	AB6			
N/A	M0	AC22			
N/A	M1	W20			
N/A	M2	AB21			
N/A	TCK	G8			
N/A	TDI	H20			
N/A	TDO	H7			
N/A	TMS	F7			
N/A	PWRDWN_B	AC5			
N/A	HSWAP_EN	E21			
N/A	RSVD	D5			
N/A	VBATT	E6			
N/A	DXP	F20			
N/A	DXN	G19			
N/A	AVCCAUXTX7	B11			
N/A	VTTXPAD7	B12			
N/A	TXNPAD7	A12			
N/A	TXPPAD7	A11			
N/A	GNDA7	C11			
N/A	RXPPAD7	A10			
N/A	RXNPAD7	A9			
N/A	VTRXPAD7	B10			
N/A	AVCCAUXRX7	B9			
N/A	AVCCAUXTX9	B6	NC	NC	
N/A	VTTXPAD9	B7	NC	NC	
N/A	TXNPAD9	A7	NC	NC	
N/A	TXPPAD9	A6	NC	NC	
N/A	GNDA9	C5	NC	NC	
N/A	RXPPAD9	A5	NC	NC	
N/A	RXNPAD9	A4	NC	NC	
N/A	VTRXPAD9	B5	NC	NC	

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
5	IO_L48N_5		AH20	NC		
5	IO_L48P_5		AH21	NC		
5	IO_L47N_5		AE19	NC		
5	IO_L47P_5		AE20	NC		
5	IO_L46N_5		AD18	NC		
5	IO_L46P_5		AC18	NC		
5	IO_L45N_5/VREF_5		AJ22			
5	IO_L45P_5		AH22			
5	IO_L44N_5		AE21			
5	IO_L44P_5		AE22			
5	IO_L43N_5		AD19			
5	IO_L43P_5		AC19			
5	IO_L39N_5		AG21			
5	IO_L39P_5		AF21			
5	IO_L38N_5		AF22			
5	IO_L38P_5		AF23			
5	IO_L37N_5		AD20			
5	IO_L37P_5		AC20			
5	IO_L09N_5/VREF_5		AK23			
5	IO_L09P_5		AJ23			
5	IO_L08N_5		AE23			
5	IO_L08P_5		AE24			
5	IO_L07N_5/VREF_5		AD21			
5	IO_L07P_5		AC21			
5	IO_L06N_5/VRP_5		AH23			
5	IO_L06P_5/VRN_5		AG23			
5	IO_L05_5/No_Pair		AD23			
5	IO_L03N_5/D4		AH24			
5	IO_L03P_5/D5		AG24			
5	IO_L02N_5/D6		AD22			
5	IO_L02P_5/D7		AC22			
5	IO_L01N_5/RDWR_B		AF24			
5	IO_L01P_5/CS_B		AG25			
6	IO_L01P_6/VRN_6		AK28			
6	IO_L01N_6/VRP_6		AJ28			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
6	IO_L86P_6		T23			
6	IO_L86N_6		T24			
6	IO_L87P_6		U28			
6	IO_L87N_6/VREF_6		U29			
6	IO_L88P_6		T27			
6	IO_L88N_6		T28			
6	IO_L89P_6		T25			
6	IO_L89N_6		T26			
6	IO_L90P_6		V30			
6	IO_L90N_6		U30			
7	IO_L90P_7		R28			
7	IO_L90N_7		R27			
7	IO_L89P_7		R26			
7	IO_L89N_7		R25			
7	IO_L88P_7		T29			
7	IO_L88N_7/VREF_7		R29			
7	IO_L87P_7		P27			
7	IO_L87N_7		P26			
7	IO_L86P_7		R24			
7	IO_L86N_7		R23			
7	IO_L85P_7		P29			
7	IO_L85N_7		P28			
7	IO_L60P_7		N28			
7	IO_L60N_7		N27			
7	IO_L59P_7		P24			
7	IO_L59N_7		P23			
7	IO_L58P_7		P30			
7	IO_L58N_7/VREF_7		N30			
7	IO_L57P_7		M28			
7	IO_L57N_7		M27			
7	IO_L56P_7		R22			
7	IO_L56N_7		P22			
7	IO_L55P_7		N29			
7	IO_L55N_7		M29			
7	IO_L54P_7		L27			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	GND		U18			
N/A	GND		U17			
N/A	GND		U16			
N/A	GND		U15			
N/A	GND		U14			
N/A	GND		U13			
N/A	GND		U12			
N/A	GND		U6			
N/A	GND		T19			
N/A	GND		T18			
N/A	GND		T17			
N/A	GND		T16			
N/A	GND		T15			
N/A	GND		T14			
N/A	GND		T13			
N/A	GND		T12			
N/A	GND		R19			
N/A	GND		R18			
N/A	GND		R17			
N/A	GND		R16			
N/A	GND		R15			
N/A	GND		R14			
N/A	GND		R13			
N/A	GND		R12			
N/A	GND		P25			
N/A	GND		P19			
N/A	GND		P18			
N/A	GND		P17			
N/A	GND		P16			
N/A	GND		P15			
N/A	GND		P14			
N/A	GND		P13			
N/A	GND		P12			
N/A	GND		P6			
N/A	GND		N19			
N/A	GND		N18			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
1	VCCO_1	L15				
1	VCCO_1	M13				
1	VCCO_1	M14				
1	VCCO_1	M15				
1	VCCO_1	M16				
1	VCCO_1	M17				
2	VCCO_2	F3				
2	VCCO_2	K6				
2	VCCO_2	M11				
2	VCCO_2	N11				
2	VCCO_2	N12				
2	VCCO_2	P11				
2	VCCO_2	P12				
2	VCCO_2	R5				
2	VCCO_2	R11				
2	VCCO_2	R12				
2	VCCO_2	T12				
2	VCCO_2	U12				
3	VCCO_3	V12				
3	VCCO_3	W12				
3	VCCO_3	Y5				
3	VCCO_3	Y11				
3	VCCO_3	Y12				
3	VCCO_3	AA11				
3	VCCO_3	AA12				
3	VCCO_3	AB11				
3	VCCO_3	AB12				
3	VCCO_3	AC11				
3	VCCO_3	AE6				
3	VCCO_3	AJ3				
4	VCCO_4	AC13				
4	VCCO_4	AC14				
4	VCCO_4	AC15				
4	VCCO_4	AC16				
4	VCCO_4	AC17				
4	VCCO_4	AD12				
4	VCCO_4	AD13				
4	VCCO_4	AD14				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
2	IO_L59P_2	U11		
2	IO_L60N_2	R1		
2	IO_L60P_2	R2		
2	IO_L85N_2	T3		
2	IO_L85P_2	T4		
2	IO_L86N_2	U8		
2	IO_L86P_2	U9		
2	IO_L87N_2	U2		
2	IO_L87P_2	T2		
2	IO_L88N_2/VREF_2	U4		
2	IO_L88P_2	U5		
2	IO_L89N_2	U6		
2	IO_L89P_2	U7		
2	IO_L90N_2	V3		
2	IO_L90P_2	U3		
3	IO_L90N_3	V6		
3	IO_L90P_3	V7		
3	IO_L89N_3	V10		
3	IO_L89P_3	V11		
3	IO_L88N_3	V4		
3	IO_L88P_3	V5		
3	IO_L87N_3/VREF_3	V2		
3	IO_L87P_3	W2		
3	IO_L86N_3	V8		
3	IO_L86P_3	V9		
3	IO_L85N_3	W6		
3	IO_L85P_3	W7		
3	IO_L60N_3	W3		
3	IO_L60P_3	W4		
3	IO_L59N_3	W10		
3	IO_L59P_3	W11		
3	IO_L58N_3	Y5		
3	IO_L58P_3	Y6		
3	IO_L57N_3/VREF_3	Y3		
3	IO_L57P_3	AA3		
3	IO_L56N_3	W8		
3	IO_L56P_3	Y7		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
N/A	GND	AF30		
N/A	GND	AB30		
N/A	GND	W30		
N/A	GND	T30		
N/A	GND	N30		
N/A	GND	J30		
N/A	GND	E30		
N/A	GND	A30		
N/A	GND	AP26		
N/A	GND	AK26		
N/A	GND	AB26		
N/A	GND	W26		
N/A	GND	T26		
N/A	GND	N26		
N/A	GND	E26		
N/A	GND	A26		
N/A	GND	AE25		
N/A	GND	K25		
N/A	GND	AP22		
N/A	GND	AK22		
N/A	GND	AF22		
N/A	GND	J22		
N/A	GND	E22		
N/A	GND	A22		
N/A	GND	Y21		
N/A	GND	W21		
N/A	GND	V21		
N/A	GND	U21		
N/A	GND	T21		
N/A	GND	R21		
N/A	GND	AA20		
N/A	GND	Y20		
N/A	GND	W20		
N/A	GND	V20		
N/A	GND	U20		
N/A	GND	T20		
N/A	GND	R20		
N/A	GND	P20		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
1	IO_L36N_1/VREF_1	E13	NC	
1	IO_L36P_1	D13	NC	
1	IO_L35N_1	K15	NC	
1	IO_L35P_1	J15	NC	
1	IO_L34N_1	G13	NC	
1	IO_L34P_1	F12	NC	
1	IO_L30N_1	J13	NC	
1	IO_L30P_1	H13	NC	
1	IO_L29N_1	L15	NC	
1	IO_L29P_1	L14	NC	
1	IO_L28N_1	E12	NC	
1	IO_L28P_1	D12	NC	
1	IO_L27N_1/VREF_1	J12		
1	IO_L27P_1	H12		
1	IO_L26N_1	K14		
1	IO_L26P_1	J14		
1	IO_L25N_1	D11		
1	IO_L25P_1	C11		
1	IO_L21N_1	F11		
1	IO_L21P_1	E11		
1	IO_L20N_1	M14		
1	IO_L20P_1	M13		
1	IO_L19N_1	H11		
1	IO_L19P_1	G11		
1	IO_L09N_1/VREF_1	J11		
1	IO_L09P_1	J10		
1	IO_L08N_1	L13		
1	IO_L08P_1	L12		
1	IO_L07N_1	D10		
1	IO_L07P_1	C10		
1	IO_L06N_1	F10		
1	IO_L06P_1	E10		
1	IO_L05_1/No_Pair	K10		
1	IO_L03N_1/VREF_1	H10		
1	IO_L03P_1	G10		
1	IO_L02N_1	K12		
1	IO_L02P_1	K11		
1	IO_L01N_1/VRP_1	E9		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
4	IO_L38P_4	AH16		
4	IO_L39N_4	AR14		
4	IO_L39P_4	AP14		
4	IO_L43N_4	AU14		
4	IO_L43P_4	AT14		
4	IO_L44N_4	AH17		
4	IO_L44P_4	AG17		
4	IO_L45N_4	AN15		
4	IO_L45P_4/VREF_4	AM15		
4	IO_L46N_4	AR15		
4	IO_L46P_4	AP15		
4	IO_L47N_4	AK16		
4	IO_L47P_4	AJ17		
4	IO_L48N_4	AU15		
4	IO_L48P_4	AT15		
4	IO_L49N_4	AM16		
4	IO_L49P_4	AL16		
4	IO_L50_4/No_Pair	AM17		
4	IO_L53_4/No_Pair	AL17		
4	IO_L54N_4	AP16		
4	IO_L54P_4	AN17		
4	IO_L55N_4	AR16		
4	IO_L55P_4	AR17		
4	IO_L56N_4	AH18		
4	IO_L56P_4	AG18		
4	IO_L57N_4	AU17		
4	IO_L57P_4/VREF_4	AT17		
4	IO_L58N_4	AM18		
4	IO_L58P_4	AL18		
4	IO_L59N_4	AK18		
4	IO_L59P_4	AJ18		
4	IO_L60N_4	AP18		
4	IO_L60P_4	AN18		
4	IO_L64N_4	AT18		
4	IO_L64P_4	AR18		
4	IO_L65N_4	AH19		
4	IO_L65P_4	AG19		
4	IO_L66N_4	AU18		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L16N_6		AM42		
6	IO_L17P_6		AL33		
6	IO_L17N_6		AL34		
6	IO_L18P_6		AL35		
6	IO_L18N_6		AL36		
6	IO_L19P_6		AL38		
6	IO_L19N_6		AL39		
6	IO_L20P_6		AL31		
6	IO_L20N_6		AL32		
6	IO_L21P_6		AL40		
6	IO_L21N_6/VREF_6		AL41		
6	IO_L22P_6		AK35		
6	IO_L22N_6		AK36		
6	IO_L23P_6		AK33		
6	IO_L23N_6		AK34		
6	IO_L24P_6		AK37		
6	IO_L24N_6		AK38		
6	IO_L25P_6		AK39		
6	IO_L25N_6		AK40		
6	IO_L26P_6		AK31		
6	IO_L26N_6		AK32		
6	IO_L27P_6		AK41		
6	IO_L27N_6/VREF_6		AK42		
6	IO_L28P_6		AJ35		
6	IO_L28N_6		AJ36		
6	IO_L29P_6		AJ33		
6	IO_L29N_6		AJ34		
6	IO_L30P_6		AJ37		
6	IO_L30N_6		AJ38		
6	IO_L31P_6		AJ41		
6	IO_L31N_6		AJ42		
6	IO_L32P_6		AJ31		
6	IO_L32N_6		AJ32		
6	IO_L33P_6		AH33		
6	IO_L33N_6/VREF_6		AH34		
6	IO_L34P_6		AH37		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
1	IO_L87N_1/VREF_1	C15	
1	IO_L87P_1	C16	
1	IO_L86N_1	K15	
1	IO_L86P_1	J15	
1	IO_L85N_1	F15	
1	IO_L85P_1	E15	
1	IO_L84N_1	G15	
1	IO_L84P_1	G16	
1	IO_L83_1/No_Pair	M15	
1	IO_L80_1/No_Pair	L15	
1	IO_L79N_1	B14	
1	IO_L79P_1	A14	
1	IO_L78N_1	C14	
1	IO_L78P_1	D15	
1	IO_L77N_1	K14	
1	IO_L77P_1	J14	
1	IO_L76N_1	F14	
1	IO_L76P_1	E14	
1	IO_L36N_1/VREF_1	G14	
1	IO_L36P_1	H15	
1	IO_L35N_1	M14	
1	IO_L35P_1	L14	
1	IO_L34N_1	C13	
1	IO_L34P_1	B13	
1	IO_L30N_1	G13	
1	IO_L30P_1	F13	
1	IO_L29N_1	L13	
1	IO_L29P_1	K13	
1	IO_L28N_1	C12	
1	IO_L28P_1	B12	
1	IO_L27N_1/VREF_1	D12	
1	IO_L27P_1	D13	
1	IO_L26N_1	J12	
1	IO_L26P_1	H12	
1	IO_L25N_1	F12	
1	IO_L25P_1	E12	
1	IO_L21N_1	G12	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L22N_2/VREF_2	L4	
2	IO_L22P_2	L5	
2	IO_L23N_2	T8	
2	IO_L23P_2	T9	
2	IO_L24N_2	L3	
2	IO_L24P_2	K3	
2	IO_L25N_2	L1	
2	IO_L25P_2	L2	
2	IO_L26N_2	U12	
2	IO_L26P_2	V12	
2	IO_L27N_2	M7	
2	IO_L27P_2	L6	
2	IO_L28N_2/VREF_2	M5	
2	IO_L28P_2	M6	
2	IO_L29N_2	U10	
2	IO_L29P_2	U11	
2	IO_L30N_2	M3	
2	IO_L30P_2	M4	
2	IO_L31N_2	N6	
2	IO_L31P_2	N7	
2	IO_L32N_2	U7	
2	IO_L32P_2	U8	
2	IO_L33N_2	N3	
2	IO_L33P_2	N4	
2	IO_L34N_2/VREF_2	N2	
2	IO_L34P_2	M2	
2	IO_L35N_2	V10	
2	IO_L35P_2	V11	
2	IO_L36N_2	P6	
2	IO_L36P_2	P7	
2	IO_L37N_2	P1	
2	IO_L37P_2	P2	
2	IO_L38N_2	V8	
2	IO_L38P_2	V9	
2	IO_L39N_2	R6	
2	IO_L39P_2	P5	
2	IO_L40N_2/VREF_2	R4	