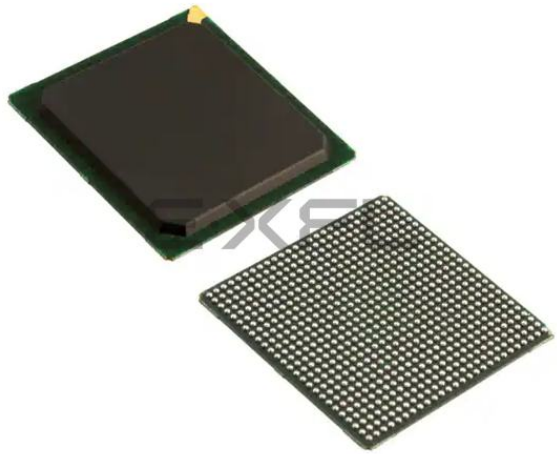

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2320
Number of Logic Elements/Cells	20880
Total RAM Bits	1622016
Number of I/O	404
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp20-6fgg676c

ing character, and remembers its location in the buffer. At some point, one transceiver designated as the master instructs all the transceivers to align to the channel bonding character "P" (or to some location relative to the channel bonding character).

After this operation, words transmitted to the FPGA fabric are properly aligned: RRRR, SSSS, TTTT, and so forth, as shown in the bottom-right portion of Figure 7. To ensure that the channels remain properly aligned following the channel bonding operation, the master transceiver must also control the clock correction operations described in the previous section for all channel-bonded transceivers.

Transmitter Buffer

The transmitter's buffer write pointer (TXUSRCLK) is frequency-locked to its read pointer (REFCLK). Therefore, clock correction and channel bonding are not required. The purpose of the transmitter's buffer is to accommodate a phase difference between TXUSRCLK and REFCLK. A simple FIFO suffices for this purpose. A FIFO depth of four will permit reliable operation with simple detection of overflow or underflow, which could occur if the clocks are not frequency-locked.

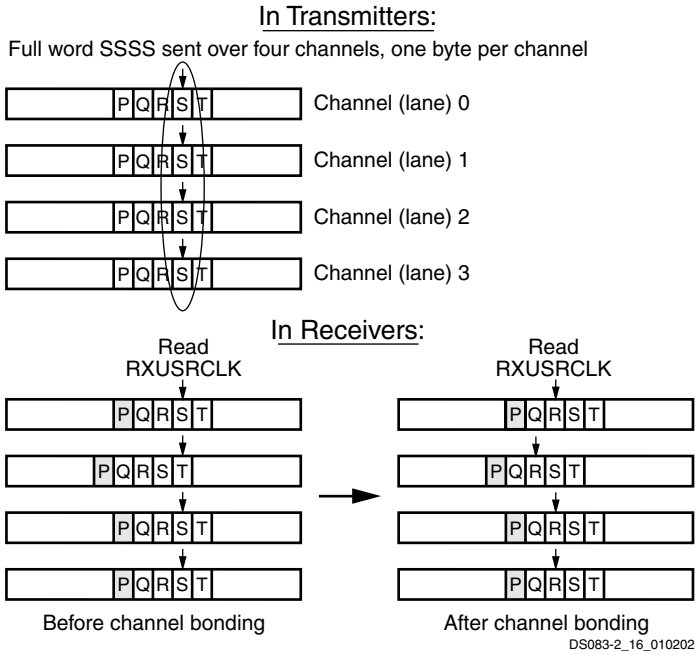

Figure 7: **Channel Bonding (Alignment)**

RocketIO X Configuration

This section outlines functions that can be selected or controlled by configuration. Xilinx implementation software supports the transceiver primitives shown in Table 3.

Table 3: **Supported RocketIO X Transceiver Primitives**

Primitive	Description
GT10_CUSTOM	Fully customizable by user
GT10_OC48_1	SONET OC-48, 1-byte data path
GT10_OC48_2	SONET OC-48, 2-byte data path
GT10_OC48_4	SONET OC-48, 4-byte data path
GT10_PCI_EXPRESS_1	PCI Express, 1-byte data path
GT10_PCI_EXPRESS_2	PCI Express, 2-byte data path
GT10_PCI_EXPRESS_4	PCI Express, 4-byte data path
GT10_INFINIBAND_1	Infiniband, 1-byte data path
GT10_INFINIBAND_2	Infiniband, 2-byte data path
GT10_INFINIBAND_4	Infiniband, 4-byte data path

Table 5: **Clock Ratios for Various Data Widths**

Fabric Data Width	Frequency Ratio of USRCLK:USRCLK2
1-byte	1:2 (1)
2-byte	1:1
4-byte	2:1 (1)

Notes:
1. Each edge of slower clock must align with falling edge of faster clock.

FPGA Transmit Interface

The FPGA can send either one, two, or four characters of data to the transmitter. Each character can be either 8 bits or 10 bits wide. If 8-bit data is applied, the additional inputs become control signals for the 8B/10B encoder. When the 8B/10B encoder is bypassed, the 10-bit character order is generated as follows:

TXCHARDISPMODE[0] (first bit transmitted)
TXCHARDISPVAL[0]
TXDATA[7:0] (last bit transmitted is TXDATA[0])

Disparity Control

The 8B/10B encoder is initialized with a negative running disparity. Unique control allows forcing the current running disparity state.

TXRUNDISP signals its current running disparity. This may be useful in those cases where there is a need to manipulate the initial running disparity value.

Bits TXCHARDISPMODE and TXCHARDISPVAL control the generation of running disparity before each byte.

For example, the transceiver can generate the sequence

```
K28.5+ K28.5+ K28.5- K28.5-
```

or

```
K28.5- K28.5- K28.5+ K28.5+
```

by specifying inverted running disparity for the second and fourth bytes.

Transmit FIFO

Proper operation of the circuit is only possible if the FPGA clock (TXUSRCLK) is frequency-locked to the reference clock (REFCLK). Phase variations up to one clock cycle are allowable. The FIFO has a depth of four. Overflow or underflow conditions are detected and signaled at the interface. Bypassing of this FIFO is programmable.

8B/10B Encoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

A bypassable 8B/10B encoder is included. The encoder uses the same 256 data characters and 12 control characters used by Gigabit Ethernet, Fibre Channel, and InfiniBand.

The encoder accepts 8 bits of data along with a K-character signal for a total of 9 bits per character applied, and generates a 10 bit character for transmission. If the K-character signal is High, the data is encoded into one of the twelve possible K-characters available in the 8B/10B code. If the K-character input is Low, the 8 bits are encoded as standard data. If the K-character input is High, and a user applies other than one of the twelve possible combinations, TXKERR indicates the error.

8B/10B Decoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

An optional 8B/10B decoder is included. A programmable option allows the decoder to be bypassed. When the 8B/10B decoder is bypassed, the 10-bit character order is, for example,

RXCHARISK[0] (first bit received)
RXRUNDISP[0]
RXDATA[7:0] (last bit received is RXDATA[0])

The decoder uses the same table that is used for Gigabit Ethernet, Fibre Channel, and InfiniBand. In addition to decoding all data and K-characters, the decoder has several extra features. The decoder separately detects both “disparity errors” and “out-of-band” errors. A disparity error is the reception of 10-bit character that exists within the 8B/10B table but has an incorrect disparity. An out-of-band error is the reception of a 10-bit character that does not exist within the 8B/10B table. It is possible to obtain an out-of-band error without having a disparity error. The proper disparity is always computed for both legal and illegal characters. The current running disparity is available at the RXRUNDISP signal.

The 8B/10B decoder performs a unique operation if out-of-band data is detected. If out-of-band data is detected, the decoder signals the error and passes the illegal 10-bits through and places them on the outputs. This can be used for debugging purposes if desired.

The decoder also signals the reception of one of the 12 valid K-characters. In addition, a programmable comma detect is included. The comma detect signal registers a comma on the receipt of any comma+, comma–, or both. Since the comma is defined as a 7-bit character, this includes several out-of-band characters. Another option allows the decoder to detect only the three defined commas (K28.1, K28.5, and K28.7) as comma+, comma–, or both. In total, there are six possible options, three for valid commas and three for "any comma."

Note that all bytes (1, 2, or 4) at the RX FPGA interface each have their own individual 8B/10B indicators (K-character, disparity error, out-of-band error, current running disparity, and comma detect).

- Execution unit
- Timers
- Debug logic unit

It operates on instructions in a five stage pipeline consisting of a fetch, decode, execute, write-back, and load write-back stage. Most instructions execute in a single cycle, including loads and stores.

Instruction and Data Cache

The embedded PPC405 core provides an instruction cache unit (ICU) and a data cache unit (DCU) that allow concurrent accesses and minimize pipeline stalls. The instruction and data cache array are 16 KB each. Both cache units are two-way set associative. Each way is organized into 256 lines of 32 bytes (eight words). The instruction set provides a rich assortment of cache control instructions, including instructions to read tag information and data arrays.

The PPC405 core accesses external memory through the instruction (ICU) and data cache units (DCU). The cache units each include a 64-bit PLB master interface, cache arrays, and a cache controller. The ICU and DCU handle cache misses as requests over the PLB to another PLB device such as an external bus interface unit. Cache hits are handled as single cycle memory accesses to the instruction and data caches.

Instruction Cache Unit (ICU)

The ICU provides one or two instructions per cycle to the instruction queue over a 64-bit bus. A line buffer (built into the output of the array for manufacturing test) enables the ICU to be accessed only once for every four instructions, to reduce power consumption by the array.

The ICU can forward any or all of the four or eight words of a line fill to the EXU to minimize pipeline stalls caused by cache misses. The ICU aborts speculative fetches abandoned by the EXU, eliminating unnecessary line fills and enabling the ICU to handle the next EXU fetch. Aborting abandoned requests also eliminates unnecessary external bus activity, thereby increasing external bus utilization.

Data Cache Unit (DCU)

The DCU transfers one, two, three, four, or eight bytes per cycle, depending on the number of byte enables presented by the CPU. The DCU contains a single-element command and store data queue to reduce pipeline stalls; this queue enables the DCU to independently process load/store and cache control instructions. Dynamic PLB request prioritization reduces pipeline stalls even further. When the DCU is busy with a low-priority request while a subsequent storage operation requested by the CPU is stalled; the DCU automatically increases the priority of the current request to the PLB.

The DCU provides additional features that allow the programmer to tailor its performance for a given application. The DCU can function in write-back or write-through mode, as controlled by the Data Cache Write-through Register (DCWR) or the Translation Look-aside Buffer (TLB); the cache controller can be tuned for a balance of performance and memory coherency. Write-on-allocate, controlled by the store word on allocate (SWOA) field of the Core Configuration Register 0 (CCR0), can inhibit line fills caused by store misses, to further reduce potential pipeline stalls and unwanted external bus traffic.

Fetch and Decode Logic

The fetch/decode logic maintains a steady flow of instructions to the execution unit by placing up to two instructions in the fetch queue. The fetch queue consists of three buffers: pre-fetch buffer 1 (PFB1), pre-fetch buffer 0 (PFB0), and decode (DCD). The fetch logic ensures that instructions proceed directly to decode when the queue is empty.

Static branch prediction as implemented on the PPC405 core takes advantage of some standard statistical properties of code. Branches with negative address displacement are by default assumed taken. Branches that do not test the condition or count registers are also predicted as taken. The PPC405 core bases branch prediction upon these default conditions when a branch is not resolved and speculatively fetches along the predicted path. The default prediction can be overridden by software at assembly or compile time.

Branches are examined in the decode and pre-fetch buffer 0 fetch queue stages. Two branch instructions can be handled simultaneously. If the branch in decode is not taken, the fetch logic fetches along the predicted path of the branch instruction in pre-fetch buffer 0. If the branch in decode is taken, the fetch logic ignores the branch instruction in pre-fetch buffer 0.

Execution Unit

The embedded PPC405 core has a single issue execution unit (EXU) containing the register file, arithmetic logic unit (ALU), and the multiply-accumulate (MAC) unit. The execution unit performs all 32-bit PowerPC integer instructions in hardware.

The register file is comprised of thirty-two 32-bit general purpose registers (GPR), which are accessed with three read ports and two write ports. During the decode stage, data is read out of the GPRs and fed to the execution unit. Likewise, during the write-back stage, results are written to the GPR. The use of the five ports on the register file enables either a load or a store operation to execute in parallel with an ALU operation.

Memory Management Unit (MMU)

The embedded PPC405 core has a 4 GB address space, which is presented as a flat address space.

The MMU provides address translation, protection functions, and storage attribute control for embedded applications. The MMU supports demand-paged virtual memory and other management schemes that require precise control of logical-to-physical address mapping and flexible

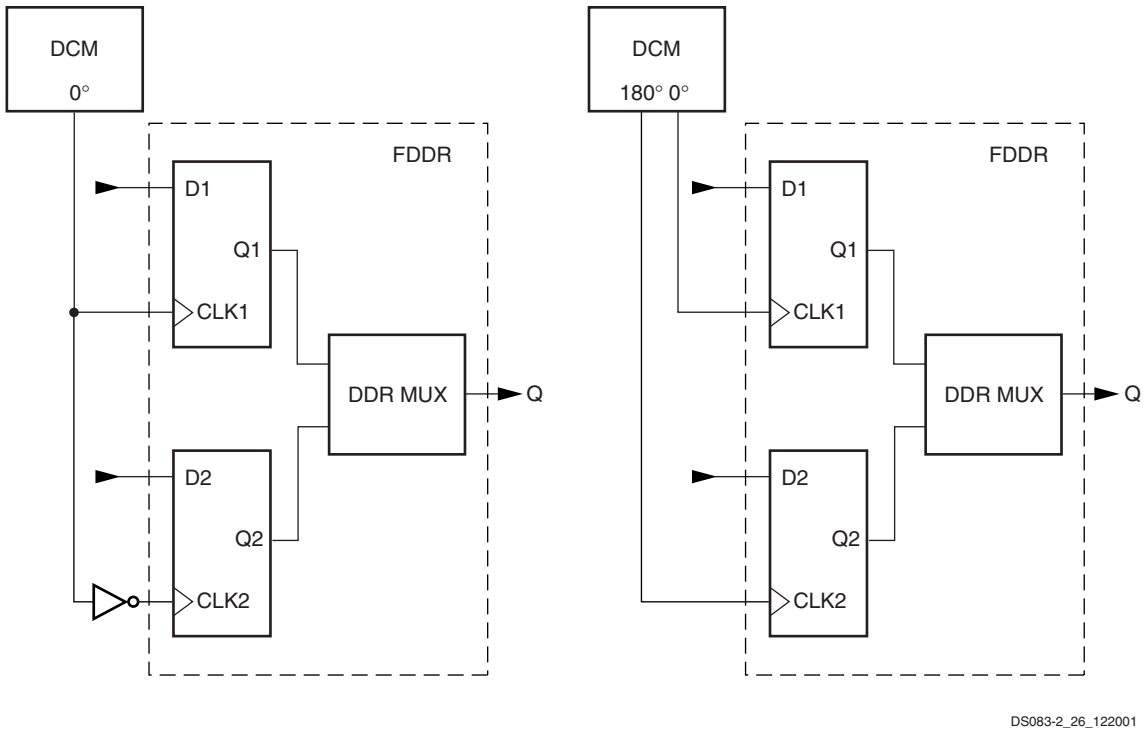

Figure 20: **Double Data Rate Registers**

This DDR mechanism can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay. It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. Virtex-II Pro devices can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals). Two neighboring IOBs have a shared routing resource connecting the ICLK and OTCLK pins on pairs of IOBs. If two adjacent IOBs using DDR registers do not share the same clock signals on their clock pins (ICLK1, ICLK2, OTCLK1, and OTCLK2), one of the clock signals will be unroutable.

The IOB pairing is identical to the LVDS IOB pairs. Hence, the package pin-out table can also be used for pin assignment to avoid conflict.

SR forces the storage element into the state specified by the SRHIGH or SRLOW attribute. SRHIGH forces a logic 1. SRLOW forces a logic “0”. When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default, the SRLOW attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLOW, INIT0, and INIT1 attributes are independent. Synchronous or asynchronous set / reset is consistent in an IOB block.

All the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Each register or latch, independent of all other registers or latches, can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.

Refer to Figure 21.

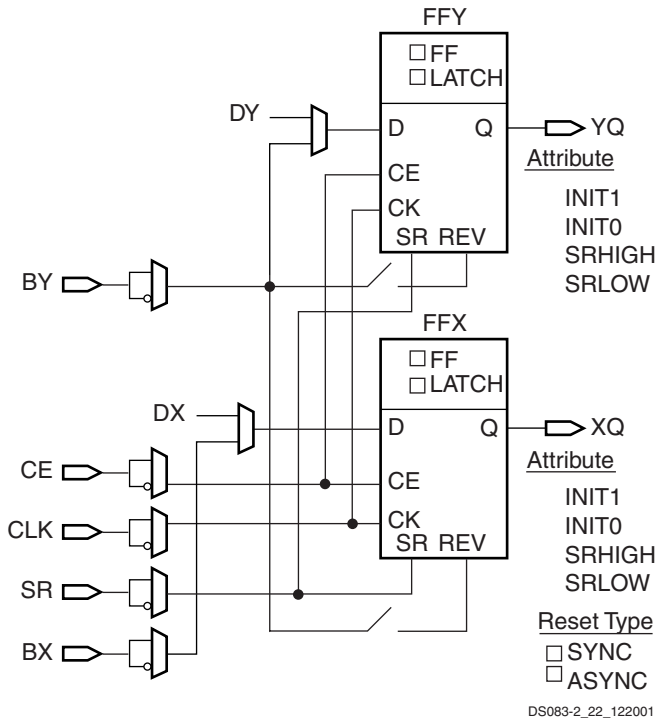

Figure 35: **Register / Latch Configuration in a Slice**

The set and reset functionality of a register or a latch can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

Distributed SelectRAM+ Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM+ element. SelectRAM+ elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8-bit RAM
- Single-Port 32 x 4-bit RAM
- Single-Port 64 x 2-bit RAM
- Single-Port 128 x 1-bit RAM
- Dual-Port 16 x 4-bit RAM
- Dual-Port 32 x 2-bit RAM
- Dual-Port 64 x 1-bit RAM

Distributed SelectRAM+ memory modules are synchronous (write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM+ memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.

Table 16 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM+ configuration.

Table 16: **Distributed SelectRAM+ Configurations**

RAM	Number of LUTs
16 x 1S	1
16 x 1D	2
32 x 1S	2
32 x 1D	4
64 x 1S	4
64 x 1D	8
128 x 1S	8

Notes:
1. S = single-port configuration; D = dual-port configuration

For single-port configurations, distributed SelectRAM+ memory has one address port for synchronous writes and asynchronous reads.

For dual-port configurations, distributed SelectRAM+ memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).

In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port

CLB/Slice Configurations

Table 19 summarizes the logic resources in one CLB. All of the CLBs are identical and each CLB or slice can be implemented in one of the configurations listed. Table 20 shows the available resources in all CLBs.

Table 19: **Logic Resources in One CLB**

Slices	LUTs	Flip-Flops	MULT_ANDs	Arithmetic & Carry-Chains	SOP Chains	Distributed SelectRAM+	Shift Registers	TBUF
4	8	8	8	2	2	128 bits	128 bits	2

Table 20: **Virtex-II Pro Logic Resources Available in All CLBs**

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry-Chains(1)	Number of SOP Chains(1)
XC2VP2	16 x 22	1,408	2,816	45,056	2,816	44	32
XC2VP4	40 x 22	3,008	6,016	96,256	6,016	44	80
XC2VP7	40 x 34	4,928	9,856	157,696	9,856	68	80
XC2VP20	56 x 46	9,280	18,560	296,960	18,560	92	112
XC2VPX20	56 x 46	9,792	19,584	313,334	18,560	92	112
XC2VP30	80 x 46	13,696	27,392	438,272	27,392	92	160
XC2VP40	88 x 58	19,392	38,784	620,544	38,784	116	176
XC2VP50	88 x 70	23,616	47,232	755,712	47,232	140	176
XC2VP70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VPX70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VP100	120 x 94	44,096	88,192	1,411,072	88,192	188	240

Notes:
1. The carry-chains and SOP chains can be split or cascaded.

18 Kb Block SelectRAM+ Resources

Introduction

Virtex-II Pro devices incorporate large amounts of 18 Kb block SelectRAM+ resources. These complement the distributed SelectRAM+ resources that provide shallow RAM structures implemented in CLBs. Each Virtex-II Pro block SelectRAM+ resource is an 18 Kb true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical. CLK, EN, WE, and SSR polarities are defined through configuration.

Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for write) and Data/parity data outputs (for read).

Operation is synchronous; the block SelectRAM+ behaves like a register. Control, address and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, a configuration option) clock edge. Data outputs change as a result of the same clock edge.

Configuration

Virtex-II Pro block SelectRAM+ supports various configurations, including single- and dual-port RAM and various data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 21.

Table 21: **Dual- and Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

Single-Port Configuration

As a single-port RAM, the block SelectRAM+ has access to the 18 Kb memory locations in any of the 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations and to 16 Kb memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of the 9-bit, 18-bit and 36-bit widths is the ability to store a parity bit for each eight bits. Parity bits must be generated or checked exter-

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
4	IO_L69P_4/VREF_4	AA12			
4	IO_L74N_4/GCLK3S	U12			
4	IO_L74P_4/GCLK2P	V12			
4	IO_L75N_4/GCLK1S	W12			
4	IO_L75P_4/GCLK0P	Y12			
5	IO_L75N_5/GCLK7S	Y11			
5	IO_L75P_5/GCLK6P	W11			
5	IO_L74N_5/GCLK5S	V11			
5	IO_L74P_5/GCLK4P	U11			
5	IO_L69N_5/VREF_5	AA11			
5	IO_L69P_5	Y10			
5	IO_L67N_5	V10			
5	IO_L67P_5	U10			
5	IO_L09N_5/VREF_5	W10			
5	IO_L09P_5	W9			
5	IO_L07N_5/VREF_5	V9			
5	IO_L07P_5	U9			
5	IO_L06N_5/VRP_5	Y8			
5	IO_L06P_5/VRN_5	W8			
5	IO_L05_5/No_Pair	V8			
5	IO_L03N_5/D4	Y7			
5	IO_L03P_5/D5	W7			
5	IO_L02N_5/D6	V7			
5	IO_L02P_5/D7	V6			
5	IO_L01N_5/RDWR_B	W6			
5	IO_L01P_5/CS_B	W5			
6	IO_L01P_6/VRN_6	AB2			
6	IO_L01N_6/VRP_6	AA1			
6	IO_L02P_6	Y2			
6	IO_L02N_6	Y1			
6	IO_L03P_6	W2			
6	IO_L03N_6/VREF_6	W1			
6	IO_L05P_6	V4			
6	IO_L05N_6	V3			
6	IO_L06P_6	V2			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
7	IO_L52P_7	M7			
7	IO_L52N_7/VREF_7	L7			
7	IO_L50P_7	K1			
7	IO_L50N_7	K2			
7	IO_L49P_7	L3			
7	IO_L49N_7	K3			
7	IO_L48P_7	K4			
7	IO_L48N_7	K5			
7	IO_L46P_7	L8			
7	IO_L46N_7/VREF_7	K8			
7	IO_L44P_7	J1			
7	IO_L44N_7	J2			
7	IO_L43P_7	J3			
7	IO_L43N_7	J4			
7	IO_L42P_7	J5			
7	IO_L42N_7	J6			
7	IO_L40P_7	J7			
7	IO_L40N_7/VREF_7	J8			
7	IO_L38P_7	H1			
7	IO_L38N_7	H2			
7	IO_L37P_7	H6			
7	IO_L37N_7	H7			
7	IO_L36P_7	G1			
7	IO_L36N_7	G2			
7	IO_L34P_7	G3			
7	IO_L34N_7/VREF_7	G4			
7	IO_L32P_7	H5			
7	IO_L32N_7	G5			
7	IO_L31P_7	F1			
7	IO_L31N_7	F2			
7	IO_L24P_7	F3	NC		
7	IO_L24N_7	F4	NC		
7	IO_L06P_7	G6			
7	IO_L06N_7	F6			
7	IO_L04P_7	E1			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
4	VCCO_4		AA11			
4	VCCO_4		AA10			
5	VCCO_5		AB21			
5	VCCO_5		AB20			
5	VCCO_5		AB19			
5	VCCO_5		AB18			
5	VCCO_5		AA21			
5	VCCO_5		AA20			
5	VCCO_5		AA19			
5	VCCO_5		AA18			
5	VCCO_5		AA17			
5	VCCO_5		AA16			
6	VCCO_6		AB22			
6	VCCO_6		AA22			
6	VCCO_6		Y22			
6	VCCO_6		Y21			
6	VCCO_6		W22			
6	VCCO_6		W21			
6	VCCO_6		V22			
6	VCCO_6		V21			
6	VCCO_6		U21			
6	VCCO_6		T21			
7	VCCO_7		R21			
7	VCCO_7		P21			
7	VCCO_7		N22			
7	VCCO_7		N21			
7	VCCO_7		M22			
7	VCCO_7		M21			
7	VCCO_7		L22			
7	VCCO_7		L21			
7	VCCO_7		K22			
7	VCCO_7		J22			
N/A	CCLK		AC7			
N/A	PROG_B		G24			
N/A	DONE		AC8			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
4	IO_L73P_4	AG17				
4	IO_L74N_4/GCLK3S	AH17				
4	IO_L74P_4/GCLK2P	AJ17				
4	IO_L75N_4/GCLK1S	AK17				
4	IO_L75P_4/GCLK0P	AL17				
5	IO_L75N_5/GCLK7S	AL18				
5	IO_L75P_5/GCLK6P	AK18				
5	IO_L74N_5/GCLK5S	AJ18				
5	IO_L74P_5/GCLK4P	AH18				
5	IO_L73N_5	AG18				
5	IO_L73P_5	AF18				
5	IO_L69N_5/VREF_5	AL19				
5	IO_L69P_5	AK19				
5	IO_L68N_5	AJ19				
5	IO_L68P_5	AH19				
5	IO_L67N_5	AE18				
5	IO_L67P_5	AD18				
5	IO_L57N_5/VREF_5	AL20				
5	IO_L57P_5	AL21				
5	IO_L56N_5	AJ20				
5	IO_L56P_5	AH20				
5	IO_L55N_5	AG19				
5	IO_L55P_5	AF19				
5	IO_L54N_5	AM22				
5	IO_L54P_5	AM21				
5	IO_L53_5/No_Pair	AK21				
5	IO_L50_5/No_Pair	AJ21				
5	IO_L49N_5	AE19				
5	IO_L49P_5	AD19				
5	IO_L48N_5	AL23				
5	IO_L48P_5	AL22				
5	IO_L47N_5	AH21				
5	IO_L47P_5	AG21				
5	IO_L46N_5	AF20				
5	IO_L46P_5	AE20				
5	IO_L45N_5/VREF_5	AM24				
5	IO_L45P_5	AL24				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	VTTXPAD21	AN29				
N/A	AVCCAUXTX21	AN28				
N/A	AVCCAUXRX23	AN30	NC	NC		
N/A	VTRXPAD23	AN31	NC	NC		
N/A	RXNPAD23	AP30	NC	NC		
N/A	RXPPAD23	AP31	NC	NC		
N/A	GNDA23	AM30	NC	NC		
N/A	TXPPAD23	AP32	NC	NC		
N/A	TXNPAD23	AP33	NC	NC		
N/A	VTTXPAD23	AN33	NC	NC		
N/A	AVCCAUXTX23	AN32	NC	NC		
N/A	VCCINT	L11				
N/A	VCCINT	L24				
N/A	VCCINT	M12				
N/A	VCCINT	M23				
N/A	VCCINT	N13				
N/A	VCCINT	N14				
N/A	VCCINT	N15				
N/A	VCCINT	N16				
N/A	VCCINT	N17				
N/A	VCCINT	N18				
N/A	VCCINT	N19				
N/A	VCCINT	N20				
N/A	VCCINT	N21				
N/A	VCCINT	N22				
N/A	VCCINT	P13				
N/A	VCCINT	P22				
N/A	VCCINT	R13				
N/A	VCCINT	R22				
N/A	VCCINT	T13				
N/A	VCCINT	T22				
N/A	VCCINT	U13				
N/A	VCCINT	U22				
N/A	VCCINT	V13				
N/A	VCCINT	V22				
N/A	VCCINT	W13				
N/A	VCCINT	W22				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
3	IO_L36N_3	AE4		
3	IO_L36P_3	AF4		
3	IO_L35N_3	AC10		
3	IO_L35P_3	AD10		
3	IO_L34N_3	AE1		
3	IO_L34P_3	AE2		
3	IO_L33N_3/VREF_3	AF6		
3	IO_L33P_3	AF7		
3	IO_L32N_3	AC8		
3	IO_L32P_3	AC9		
3	IO_L31N_3	AF2		
3	IO_L31P_3	AF3		
3	IO_L30N_3	AG5		
3	IO_L30P_3	AG6		
3	IO_L29N_3	AD9		
3	IO_L29P_3	AE9		
3	IO_L28N_3	AG4		
3	IO_L28P_3	AH3		
3	IO_L27N_3/VREF_3	AG2		
3	IO_L27P_3	AG3		
3	IO_L26N_3	AD7		
3	IO_L26P_3	AE7		
3	IO_L25N_3	AH6		
3	IO_L25P_3	AH7		
3	IO_L24N_3	AH5		
3	IO_L24P_3	AJ5		
3	IO_L23N_3	AE8		
3	IO_L23P_3	AF8		
3	IO_L22N_3	AH1		
3	IO_L22P_3	AH2		
3	IO_L21N_3/VREF_3	AJ6		
3	IO_L21P_3	AK6		
3	IO_L20N_3	AG7		
3	IO_L20P_3	AG8		
3	IO_L19N_3	AJ3		
3	IO_L19P_3	AJ4		
3	IO_L18N_3	AJ1		
3	IO_L18P_3	AJ2		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L30N_2	N6		
2	IO_L30P_2	N7		
2	IO_L31N_2	M4		
2	IO_L31P_2	N5		
2	IO_L32N_2	R11		
2	IO_L32P_2	R12		
2	IO_L33N_2	N1		
2	IO_L33P_2	N2		
2	IO_L34N_2/VREF_2	P6		
2	IO_L34P_2	P7		
2	IO_L35N_2	R13		
2	IO_L35P_2	T13		
2	IO_L36N_2	P4		
2	IO_L36P_2	P5		
2	IO_L37N_2	P3		
2	IO_L37P_2	N3		
2	IO_L38N_2	T10		
2	IO_L38P_2	T11		
2	IO_L39N_2	P1		
2	IO_L39P_2	P2		
2	IO_L40N_2/VREF_2	R7		
2	IO_L40P_2	R8		
2	IO_L41N_2	T12		
2	IO_L41P_2	U12		
2	IO_L42N_2	R5		
2	IO_L42P_2	R6		
2	IO_L43N_2	R3		
2	IO_L43P_2	R4		
2	IO_L44N_2	U8		
2	IO_L44P_2	T8		
2	IO_L45N_2	R1		
2	IO_L45P_2	R2		
2	IO_L46N_2/VREF_2	T6		
2	IO_L46P_2	T7		
2	IO_L47N_2	U9		
2	IO_L47P_2	U10		
2	IO_L48N_2	T2		
2	IO_L48P_2	T3		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	IO_L75N_1/GCLK3P		G21		
1	IO_L75P_1/GCLK2S		F21		
1	IO_L74N_1/GCLK1P		J21		
1	IO_L74P_1/GCLK0S		K21		
1	IO_L73N_1		D20		
1	IO_L73P_1		C20		
1	IO_L69N_1/VREF_1		F20		
1	IO_L69P_1		E20		
1	IO_L68N_1		H20		
1	IO_L68P_1		J20		
1	IO_L67N_1		L20		
1	IO_L67P_1		K20		
1	IO_L66N_1/VREF_1		M20		
1	IO_L66P_1		M21		
1	IO_L65N_1		C19		
1	IO_L65P_1		D19		
1	IO_L64N_1		F19		
1	IO_L64P_1		E19		
1	IO_L60N_1		H19		
1	IO_L60P_1		G19		
1	IO_L59N_1		K19		
1	IO_L59P_1		J19		
1	IO_L58N_1		M19		
1	IO_L58P_1		L19		
1	IO_L57N_1/VREF_1		C17		
1	IO_L57P_1		C18		
1	IO_L56N_1		E18		
1	IO_L56P_1		E17		
1	IO_L55N_1		H18		
1	IO_L55P_1		G18		
1	IO_L54N_1		L18		
1	IO_L54P_1		K18		
1	IO_L53_1/No_Pair		D17		
1	IO_L50_1/No_Pair		D16		
1	IO_L49N_1		G17		
1	IO_L49P_1		F17		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L52N_6		AE42		
6	IO_L53P_6		AE32		
6	IO_L53N_6		AE33		
6	IO_L54P_6		AD35		
6	IO_L54N_6		AD36		
6	IO_L55P_6		AD37		
6	IO_L55N_6		AD38		
6	IO_L56P_6		AD31		
6	IO_L56N_6		AD32		
6	IO_L57P_6		AD39		
6	IO_L57N_6/VREF_6		AD40		
6	IO_L58P_6		AD41		
6	IO_L58N_6		AD42		
6	IO_L59P_6		AD33		
6	IO_L59N_6		AD34		
6	IO_L60P_6		AC33		
6	IO_L60N_6		AC34		
6	IO_L85P_6		AC36		
6	IO_L85N_6		AC37		
6	IO_L86P_6		AC31		
6	IO_L86N_6		AC32		
6	IO_L87P_6		AC39		
6	IO_L87N_6/VREF_6		AC40		
6	IO_L88P_6		AB33		
6	IO_L88N_6		AB34		
6	IO_L89P_6		AB36		
6	IO_L89N_6		AB37		
6	IO_L90P_6		AB39		
6	IO_L90N_6		AB40		
7	IO_L90P_7		AA39		
7	IO_L90N_7		AA40		
7	IO_L89P_7		AB31		
7	IO_L89N_7		AA31		
7	IO_L88P_7		AA36		
7	IO_L88N_7/VREF_7		AA37		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L87P_7		AA33		
7	IO_L87N_7		AA34		
7	IO_L86P_7		Y31		
7	IO_L86N_7		Y32		
7	IO_L85P_7		Y39		
7	IO_L85N_7		Y40		
7	IO_L60P_7		Y36		
7	IO_L60N_7		Y37		
7	IO_L59P_7		Y33		
7	IO_L59N_7		Y34		
7	IO_L58P_7		W41		
7	IO_L58N_7/VREF_7		W42		
7	IO_L57P_7		W39		
7	IO_L57N_7		W40		
7	IO_L56P_7		W31		
7	IO_L56N_7		W32		
7	IO_L55P_7		W37		
7	IO_L55N_7		W38		
7	IO_L54P_7		W35		
7	IO_L54N_7		W36		
7	IO_L53P_7		W33		
7	IO_L53N_7		W34		
7	IO_L52P_7		V41		
7	IO_L52N_7/VREF_7		V42		
7	IO_L51P_7		V38		
7	IO_L51N_7		V39		
7	IO_L50P_7		V31		
7	IO_L50N_7		U32		
7	IO_L49P_7		V35		
7	IO_L49N_7		V36		
7	IO_L48P_7		V32		
7	IO_L48N_7		V33		
7	IO_L47P_7		U31		
7	IO_L47N_7		T31		
7	IO_L46P_7		U41		
7	IO_L46N_7/VREF_7		U42		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	VCCO_1		D18		
2	VCCO_2		AA15		
2	VCCO_2		AA14		
2	VCCO_2		Y15		
2	VCCO_2		Y14		
2	VCCO_2		Y8		
2	VCCO_2		Y5		
2	VCCO_2		W15		
2	VCCO_2		W14		
2	VCCO_2		V15		
2	VCCO_2		V14		
2	VCCO_2		V3		
2	VCCO_2		U15		
2	VCCO_2		U14		
2	VCCO_2		T15		
2	VCCO_2		T14		
2	VCCO_2		R14		
2	VCCO_2		T9		
2	VCCO_2		P4		
2	VCCO_2		M6		
2	VCCO_2		J3		
2	VCCO_2		F5		
3	VCCO_3		AU5		
3	VCCO_3		AP3		
3	VCCO_3		AL6		
3	VCCO_3		AJ4		
3	VCCO_3		AH14		
3	VCCO_3		AG15		
3	VCCO_3		AG14		
3	VCCO_3		AG9		
3	VCCO_3		AF15		
3	VCCO_3		AF14		
3	VCCO_3		AE15		
3	VCCO_3		AE14		
3	VCCO_3		AE3		
3	VCCO_3		AD15		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
5	IO_L66P_5	BA23	
5	IO_L65N_5	AL23	
5	IO_L65P_5	AL22	
5	IO_L64N_5	AT23	
5	IO_L64P_5	AU23	
5	IO_L60N_5	BA24	
5	IO_L60P_5	BB24	
5	IO_L59N_5	AN24	
5	IO_L59P_5	AP24	
5	IO_L58N_5	AW24	
5	IO_L58P_5	AW23	
5	IO_L57N_5/VREF_5	AU24	
5	IO_L57P_5	AV24	
5	IO_L56N_5	AN25	
5	IO_L56P_5	AP25	
5	IO_L55N_5	AR24	
5	IO_L55P_5	AR23	
5	IO_L54N_5	BA25	
5	IO_L54P_5	BB25	
5	IO_L53_5/No_Pair	AM25	
5	IO_L50_5/No_Pair	AM24	
5	IO_L49N_5	AY25	
5	IO_L49P_5	AY24	
5	IO_L48N_5	AU25	
5	IO_L48P_5	AV25	
5	IO_L47N_5	AM26	
5	IO_L47P_5	AN26	
5	IO_L46N_5	AT25	
5	IO_L46P_5	AT24	
5	IO_L18N_5/VREF_5	AY26	NC
5	IO_L18P_5	BA26	NC
5	IO_L16N_5	AT26	NC
5	IO_L16P_5	AU26	NC
5	IO_L12N_5	AL26	NC
5	IO_L12P_5	AL25	NC
5	IO_L11N_5	BA27	NC
5	IO_L11P_5	BB27	NC

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L15P_6	AP39	
6	IO_L15N_6/VREF_6	AP40	
6	IO_L16P_6	AP36	
6	IO_L16N_6	AP37	
6	IO_L17P_6	AH31	
6	IO_L17N_6	AG31	
6	IO_L18P_6	AN41	
6	IO_L18N_6	AN42	
6	IO_L19P_6	AN40	
6	IO_L19N_6	AM40	
6	IO_L20P_6	AG34	
6	IO_L20N_6	AG35	
6	IO_L21P_6	AN37	
6	IO_L21N_6/VREF_6	AN38	
6	IO_L22P_6	AN36	
6	IO_L22N_6	AM36	
6	IO_L23P_6	AG32	
6	IO_L23N_6	AG33	
6	IO_L24P_6	AM41	
6	IO_L24N_6	AM42	
6	IO_L25P_6	AM38	
6	IO_L25N_6	AM39	
6	IO_L26P_6	AF35	
6	IO_L26N_6	AF36	
6	IO_L27P_6	AM37	
6	IO_L27N_6/VREF_6	AL36	
6	IO_L28P_6	AL41	
6	IO_L28N_6	AK41	
6	IO_L29P_6	AF32	
6	IO_L29N_6	AF33	
6	IO_L30P_6	AL39	
6	IO_L30N_6	AL40	
6	IO_L31P_6	AL37	
6	IO_L31N_6	AL38	
6	IO_L32P_6	AF31	
6	IO_L32N_6	AE31	
6	IO_L33P_6	AK39	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCAUX	A2	
N/A	VCCAUX	BA1	
N/A	VCCAUX	AY1	
N/A	VCCAUX	AL1	
N/A	VCCAUX	AB1	
N/A	VCCAUX	AA1	
N/A	VCCAUX	M1	
N/A	VCCAUX	C1	
N/A	VCCAUX	B1	
N/A	GND	AV42	
N/A	GND	AP42	
N/A	GND	AK42	
N/A	GND	AF42	
N/A	GND	AC42	
N/A	GND	Y42	
N/A	GND	U42	
N/A	GND	N42	
N/A	GND	J42	
N/A	GND	E42	
N/A	GND	BA41	
N/A	GND	AY41	
N/A	GND	C41	
N/A	GND	B41	
N/A	GND	BA40	
N/A	GND	B40	
N/A	GND	BB38	
N/A	GND	AV38	
N/A	GND	AP38	
N/A	GND	AK38	
N/A	GND	AF38	
N/A	GND	AC38	
N/A	GND	Y38	
N/A	GND	U38	
N/A	GND	N38	
N/A	GND	J38	
N/A	GND	E38	
N/A	GND	A38	