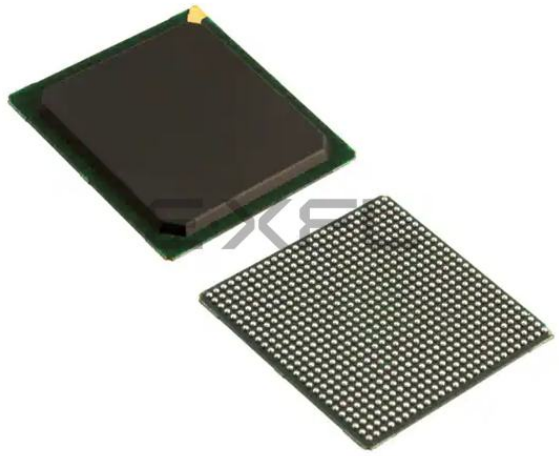

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2320 |
| Number of Logic Elements/Cells | 20880 |
| Total RAM Bits | 1622016 |
| Number of I/O | 404 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 676-BGA |
| Supplier Device Package | 676-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2vp20-6fgg676i |

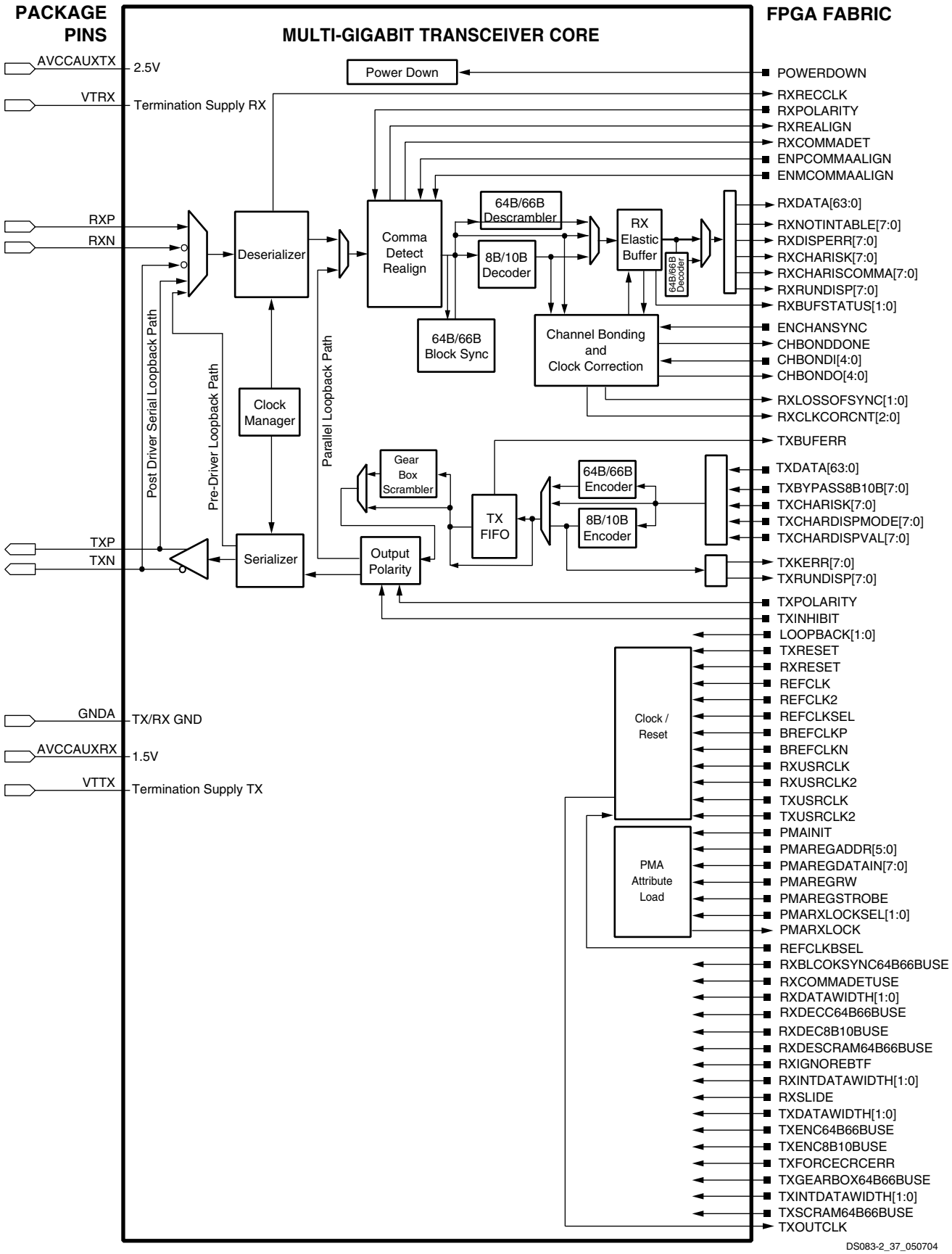


*Figure 4:* **RocketIO X Transceiver Block Diagram**

### *Receiver Buffer*

The receiver includes buffers (FIFOs) in the datapath. This section gives the reasons for including the buffers and outlines their operation.

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

The receiver uses an *elastic buffer,* where "elastic" refers to the ability to modify the read pointer for clock correction and channel bonding.

#### Comma Detection

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indication is given at the receiver interface. The realignment indicator is a distinct output.

The transceiver continuously monitors the data for the presence of the 10-bit character(s). Upon each occurrence of a 10-bit character, the data is checked for word alignment. If comma detect is disabled, the data is not aligned to any particular pattern. The programmable option allows a user to align data on comma+, comma–, both, or a unique user-defined and programmed sequence.

#### Clock Correction

RXRECCLK (the recovered clock) reflects the data rate of the incoming data. RXUSRCLK defines the rate at which the FPGA fabric consumes the data. Ideally, these rates are identical. However, since the clocks typically have different sources, one of the clocks will be faster than the other. The receiver buffer accommodates this difference between the clock rates. See Figure 12.

Nominally, the buffer is always half full. This is shown in the top buffer, Figure 12, where the shaded area represents buffered data not yet read. Received data is inserted via the write pointer under control of RXRECCLK. The FPGA fabric reads data via the read pointer under control of RXUSRCLK. The half full/half empty condition of the buffer gives a cushion for the differing clock rates. This operation continues indefinitely, regardless of whether or not "meaningful" data is being received. When there is no meaningful data to be received, the incoming data will consist of IDLE characters or other padding.

If RXUSRCLK is faster than RXRECCLK, the buffer becomes more empty over time. The clock correction logic corrects for this by decrementing the read pointer to reread a repeatable byte sequence. This is shown in the middle buffer, Figure 12, where the solid read pointer decrements to the value represented by the dashed pointer.

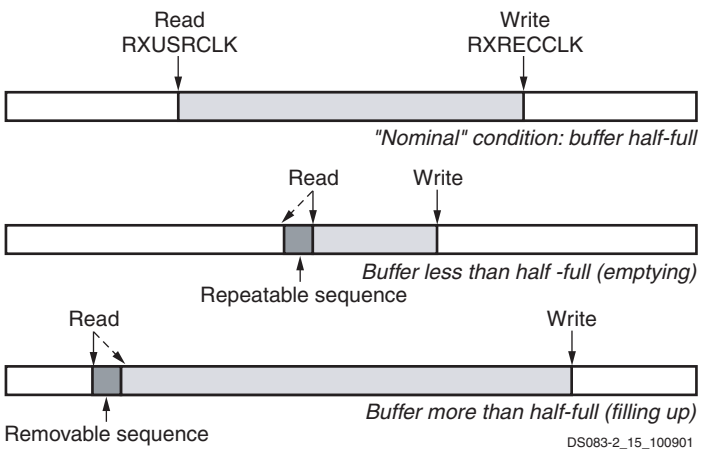


*Figure 12:* **Clock Correction in Receiver**

By decrementing the read pointer instead of incrementing it in the usual fashion, the buffer is partially refilled. The transceiver design will repeat a single repeatable byte sequence when necessary to refill a buffer. If the byte sequence length is greater than one, and if attribute CLK_COR_REPEAT_WAIT is 0, then the transceiver may repeat the same sequence multiple times until the buffer is refilled to the desired extent.

Similarly, if RXUSRCLK is slower than RXRECCLK, the buffer will fill up over time. The clock correction logic corrects for this by incrementing the read pointer to skip over a removable byte sequence that need not appear in the final FPGA fabric byte stream. This is shown in the bottom buffer, Figure 12, where the solid read pointer increments to the value represented by the dashed pointer. This accelerates the emptying of the buffer, preventing its overflow. The transceiver design will skip a single byte sequence when necessary to partially empty a buffer. If attribute CLK_COR_REPEAT_WAIT is 0, the transceiver may also skip two consecutive removable byte sequences in one step to further empty the buffer when necessary.

These operations require the clock correction logic to recognize a byte sequence that can be freely repeated or omitted in the incoming data stream. This sequence is generally an IDLE sequence, or other sequence comprised of special values that occur in the gaps separating packets of meaningful data. These gaps are required to occur sufficiently often to facilitate the timely execution of clock correction.

#### Channel Bonding

Some gigabit I/O standards such as Infiniband specify the use of multiple transceivers in parallel for even higher data rates. Words of data are split into bytes, with each byte sent over a separate channel (transceiver). See Figure 13.

# Functional Description: Processor Block

This section briefly describes the interfaces and components of the Processor Block. The subsequent section, Functional Description: Embedded PowerPC 405 Core beginning on page 20, offers a summary of major PPC405 core features. For an in-depth discussion on both the Processor Block and PPC405, see tthe **PowerPC Processor Reference Guide** and the **PowerPC 405 Processor Block Reference Guide** available on the Xilinx website at **http://www.xilinx.com**.

## Processor Block Overview

Figure 14 shows the internal architecture of the Processor Block.

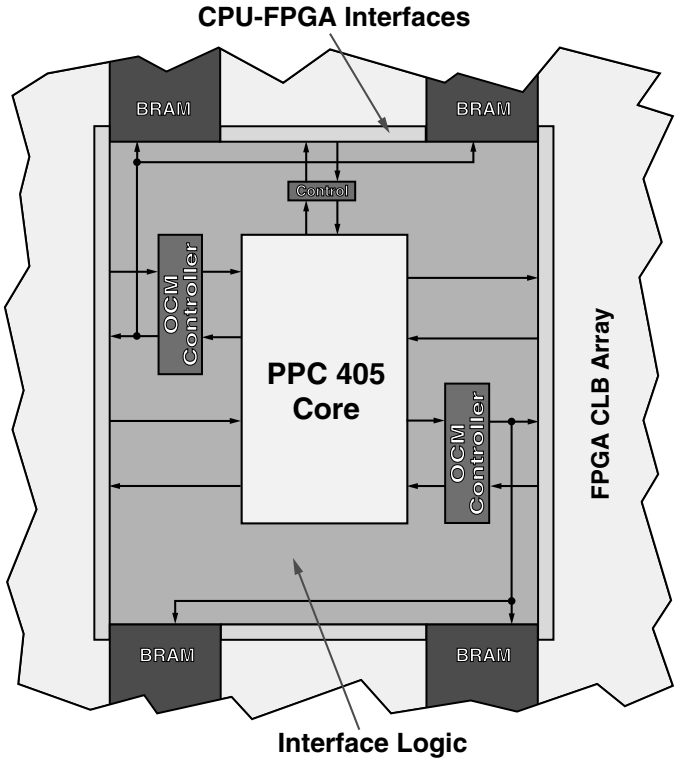


*Figure 14:* **Processor Block Architecture**

Within the Virtex-II Pro Processor Block, there are four components:

- Embedded IBM PowerPC 405-D5 RISC CPU core
- On-Chip Memory (OCM) controllers and interfaces
- Clock/control interface logic
- CPU-FPGA Interfaces

## Embedded PowerPC 405 RISC Core

The PowerPC 405D5 core is a 0.13 µm implementation of the IBM PowerPC 405D4 core. The advanced process technology enables the embedded PowerPC 405 (PPC405) core to operate at 300+ MHz while maintaining low power consumption. Specially designed interface logic integrates the core with the surrounding CLBs, block RAMs, and general routing resources. Up to four Processor Blocks can be available in a single Virtex-II Pro device.

The embedded PPC405 core implements the PowerPC User Instruction Set Architecture (UISA), user-level registers, programming model, data types, and addressing modes for 32-bit fixed-point operations. 64-bit operations, auxiliary processor operations, and floating-point operations are trapped and can be emulated in software.

Most of the PPC405 core features are compatible with the specifications for the PowerPC Virtual Environment Architecture (VEA) and Operating Environment Architecture (OEA). They also provide a number of optimizations and extensions to the lower layers of the PowerPC Architecture. The full architecture of the PPC405 is defined by the PowerPC Embedded Environment and PowerPC UISA documentation, available from IBM.

## On-Chip Memory (OCM) Controllers

### *Introduction*

The OCM controllers serve as dedicated interfaces between the block RAMs in the FPGA fabric (see 18 Kb Block SelectRAM+ Resources, page 44) and OCM signals available on the embedded PPC405 core. The OCM signals on the PPC405 core are designed to provide very quick access to a fixed amount of instruction and data memory space. The OCM controller provides an interface to both the 64-bit Instruction-Side Block RAM (ISBRAM) and the 32-bit Data-Side Block RAM (DSBRAM). The designer can choose to implement:

- ISBRAM only
- DSBRAM only
- Both ISBRAM and DSBRAM
- No ISBRAM and no DSBRAM

One of OCM's primary advantages is that it guarantees a fixed latency of execution for a higher level of determinism. Additionally, it reduces cache pollution and thrashing, since the cache remains available for caching code from other memory resources.

Typical applications for DSOCM include scratch-pad memory, as well as use of the dual-port feature of block RAM to enable bidirectional data transfer between processor and FPGA. Typical applications for ISOCM include storage of interrupt service routines.

### *Functional Features*

#### Common Features

- Separate Instruction and Data memory interface between processor core and BRAMs in FPGA
- Dedicated interface to Device Control Register (DCR) bus for ISOCM and DSOCM

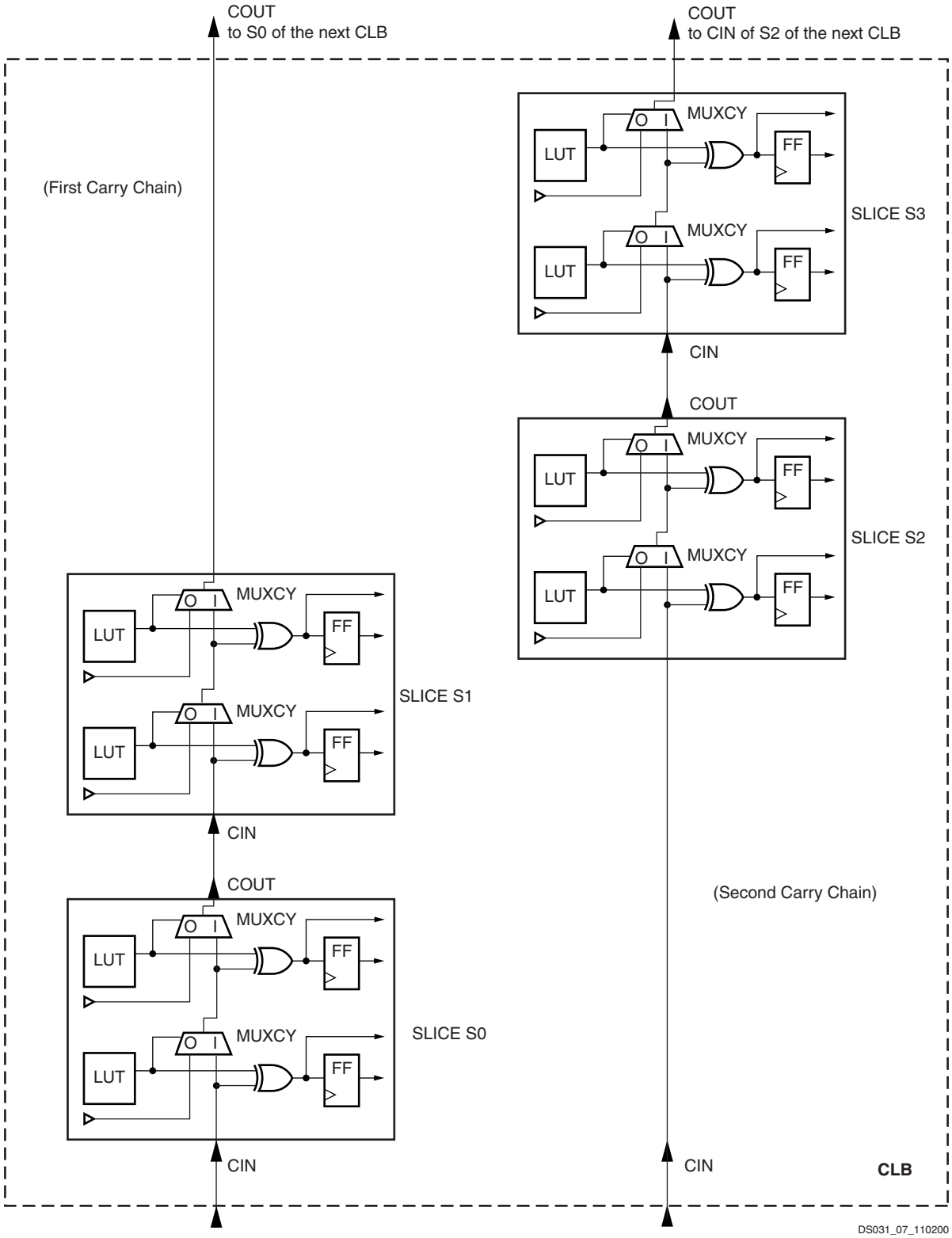


*Figure 42:* **Fast Carry Logic Path**

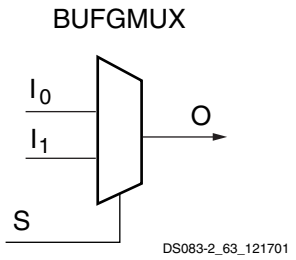


*Figure 60:* **Virtex-II Pro BUFGMUX Function**

If the presently selected clock is Low while S changes, or if it goes Low after S has changed, the output is kept Low until the other ("to-be-selected") clock has made a transition from High to Low. At that instant, the new clock starts driving the output.

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

All Virtex-II Pro devices have 16 global clock multiplexer buffers.

Figure 61 shows a switchover from I0 to I1.

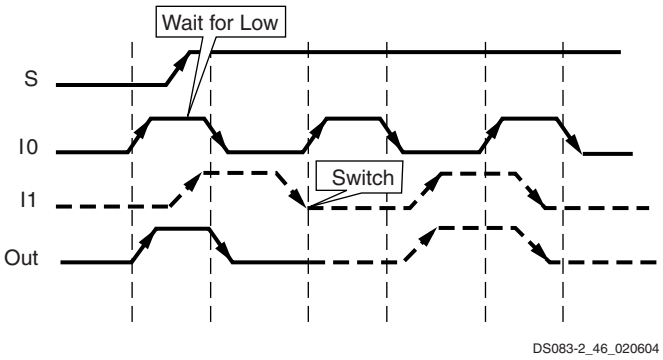


*Figure 61:* **Clock Multiplexer Waveform Diagram**

- The current clock is CLK0.
- S is activated High.
- If CLK0 is currently High, the multiplexer waits for CLK0 to go Low.
- Once CLK0 is Low, the multiplexer output stays Low until CLK1 transitions High to Low.
- When CLK1 transitions from High to Low, the output switches to CLK1.
- No glitches or short pulses can appear on the output.

## Local Clocking

In addition to global clocks, there are local clock resources in the Virtex-II Pro devices. There are more than 72 local clocks in the Virtex-II Pro family. These resources can be used for many different applications, including but not limited to memory interfaces. For example, even using only the left and right I/O banks, Virtex-II Pro FPGAs can support up to 50 local clocks for DDR SDRAM. These interfaces can operate beyond 200 MHz on Virtex-II Pro devices.

## Digital Clock Manager (DCM)

The Virtex-II Pro DCM offers a wide range of powerful clock management features.

- **Clock De-skew**: The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock, thus eliminating clock distribution delays.
- **Frequency Synthesis**: The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting**: The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four of the nine DCM clock outputs can drive inputs to global clock buffers or global clock multiplexer buffers simultaneously (see Figure 62). All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers.

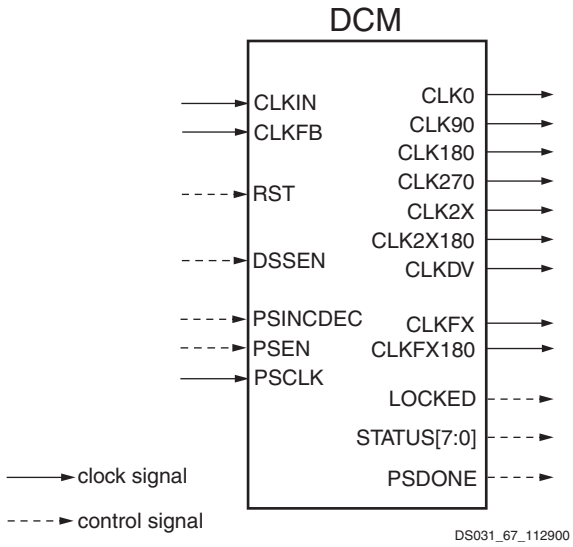


*Figure 62:* **Digital Clock Manager**

The DCM can be configured to delay the completion of the Virtex-II Pro configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

# Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics

DS083 (v5.0) June 21, 2011 **Product Specification**

## Virtex-II Pro[1] Electrical Characteristics

Virtex™-II Pro devices are provided in -7, -6, and -5 speed grades, with -7 having the highest performance.

Virtex-II Pro DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -6 speed grade industrial device are the same as for a -6 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

### Virtex-II Pro DC Characteristics

*Table 1:* **Absolute Maximum Ratings**

| Symbol | Description[1] | | Virtex-II Pro X | Virtex-II Pro | Units |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND | | –0.5 to 1.6 | | V |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | | –0.5 to 3.0 | | V |
| $V_{CCO}$ | Output drivers supply voltage relative to GND | | –0.5 to 3.75 | | V |
| $V_{BATT}$ | Key memory battery backup supply | | –0.5 to 4.05 | | V |
| $V_{REF}$ | Input reference voltage | | –0.3 to 3.75 | | V |
| $V_{IN}$ | 3.3V I/O input voltage relative to GND (user and dedicated I/Os) | | –0.3 to 4.05[3] | | V |
| | 2.5V or below I/O input voltage relative to GND (user and dedicated I/Os) | | –0.5 to $V_{CCO}$ + 0.5 | | V |
| $V_{TS}$ | Voltage applied to 3-state 3.3V output (user and dedicated I/Os) | | –0.3 to 4.05[3] | | V |
| | Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os) | | –0.5 to $V_{CCO}$ + 0.5 | | V |
| AVCCAUXRX | Receive auxilliary supply voltage relative to GNDA (analog ground) | | –0.5 to 2.0 | –0.5 to 3.0 | V |
| AVCCAUXTX | Transmit auxilliary supply voltage relative to GNDA (analog ground) | | –0.5 to 3.0 | –0.5 to 3.0 | V |
| $V_{TRX}$ | Terminal receive supply voltage relative to GND | | –0.5 to 3.0 | –0.5 to 3.0 | V |
| $V_{TTX}$ | Terminal transmit supply voltage relative to GND | | –0.5 to 1.6 | –0.5 to 3.0 | V |
| $T_{STG}$ | Storage temperature (ambient) | | –65 to +150 | | °C |
| $T_{SOL}$ | Maximum soldering temperature[2] | All regular FG/FF flip-chip packages | +220 | | °C |
| | | Pb-free FGG256 wire-bond package | N/A | +260 | °C |
| | | Pb-free FGG456 and FGG676 wire-bond packages | N/A | +250 | °C |
| $T_J$ | Maximum junction temperature[2] | | +125 | | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see the **Device Packaging and Thermal Characteristics Guide** information on the Xilinx website.
3. 3.3V I/O Absolute Maximum limit applied to DC and AC signals. Refer to **XAPP659** for more details.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

# Virtex-II Pro Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

## Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM

*Table 55:* **Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM**

| | | | Speed Grade | | | |
|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Device** | **-7** | **-6** | **-5** | **Units** |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)<br>For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25. | | | | | | |
| No Delay<br>Global Clock and IFF(2) with DCM | $T_{PSDCM}/T_{PHDCM}$ | XC2VP2 | 1.54/–0.58 | 1.54/–0.57 | 1.54/–0.56 | ns |
| | | XC2VP4 | 1.59/–0.59 | 1.59/–0.58 | 1.59/–0.57 | ns |
| | | XC2VP7 | 1.66/–0.61 | 1.66/–0.59 | 1.66/–0.57 | ns |
| | | XC2VP20 | 1.68/–0.53 | 1.68/–0.53 | 1.68/–0.50 | ns |
| | | XC2VPX20 | 1.68/–0.53 | 1.68/–0.53 | 1.68/–0.50 | ns |
| | | XC2VP30 | 1.81/–0.74 | 1.81/–0.74 | 1.81/–0.71 | ns |
| | | XC2VP40 | 1.85/–0.65 | 1.85/–0.64 | 1.85/–0.60 | ns |
| | | XC2VP50 | 1.85/–0.57 | 1.85/–0.54 | 1.85/–0.50 | ns |
| | | XC2VP70 | 1.86/–0.45 | 1.86/–0.39 | 1.86/–0.30 | ns |
| | | XC2VPX70 | 1.86/–0.45 | 1.86/–0.39 | 1.86/–0.30 | ns |
| | | XC2VP100 | N/A | 1.86/–0.35 | 1.87/–0.28 | ns |

**Notes:**

1. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case duty-cycle distortion using CLK0 and CLK180, $T_{DCD\_CLK180}$.
3. IFF = Input Flip-Flop or Latch

| Date | Version | Revision |
|---|---|---|
| 12/03/02 | 2.5 | Updated parametric information in:<br>• Table 1: Correct lower limit of voltage range of $V_{IN}$ and $V_{TS}$ from –0.5V to –0.3V for 3.3V.<br>• Table 2: Add footnote (2) regarding $V_{CCAUX}$ voltage droop. Renumbered other notes.<br>• Table 12: Add waveform diagrams (Figure 1 and Figure 2) illustrating $DV_{OUT}$ (single-ended) and $DV_{PPOUT}$ (differential).<br>• Table 23: Indicate REFCLK upper frequency limitation; relate REFCLK parameters to REFCLK2, BREFCLK, and BREFCLK2; correct $T_{RCLK}$ and $T_{FCLK}$ values and unit of measurement.<br>• Table 60: Add qualifying footnote to CLKOUT_DUTY_CYCLE_DLL. |
| 01/20/03 | 2.6 | Updated parametric information in:<br>• Table 12: Correct $DV_{IN}$ Min (200 mV to 175 mV) and $DV_{IN}$ Max (1000 mV to 2000 mV).<br>• Table 23: Correct $T_{RCLK}$ /$T_{FCLK}$ Typ (400 ps to 600 ps) and Max (600 ps to 1000 ps). Add footnote (2) to qualify Max $T_{GJTT}$ parameter.<br>• Table 59: Correct hyperlink in footnote (1) to point directly to Answer Record 13645.<br>• Move clock parameters from Table 18, Table 19, Table 20, and Table 21 to Table 16. |
| 03/24/03 | 2.7 | • Added/updated timing parameters from speedsfile **v1.76**.<br>• Table 2: Delete first table footnote and renumber all others.<br>• Table 3: Add "sample-tested" to $I_L$. Remove "Device" column, unnecessary.<br>• Table 8: Update $V_{OCM}$ (Typ) to 1.250V.<br>• Table 10: Update LVPECL_25 DC parameters.<br>• Table 23: Update $F_{GCLK}$ frequency ranges. Break out $T_{GJTT}$ by operating speed.<br>• Table 27: Update $F_{GTX}$ frequency ranges. Correct $T_{DJ}$ to 0.17 UI, $T_{RJ}$ to o.18 UI.<br>• Table 39: Update $V_{REF}$ (Typ) for HSTL Class I/II from 1.08V to 0.90V.<br>• Table 43, Table 44: Correct parameter name "CE input (WS)" to "SR input".<br>• Table 64: Break out $T_{DCD\_CLK0}$ by device type. |
| 05/27/03 | 2.8 | • Updated time and frequency parameters as per speedsfile **v1.78**.<br>• Table 3: Added values for $I_{REF}$, $I_L$, $I_{RPU}$, $I_{RPD}$<br>• Corrected $I_{CCINTQ}$ (Table 4) and $I_{CCINTMIN}$ (Table 5) for XC2VP20 to 600 mA.<br>• Table 4: Updated/Added Typ and Max quiescent current values for XC2VP7 and XC2VP20. Added footnote specifying parameters are for Commercial Grade parts.<br>• Table 5: Added footnote specifying parameters are for Commercial Grade parts.<br>• Table 6: Corrected $V_{IH}$ (Max) for LVTTL and LVCMOS33 standards from 3.6V to 3.45V. Changed $V_{IL}$ (Min) for all standards to –0.2V. Corrected $V_{IL}$ (Max) for LVCMOS15 and LVCMOS18 from 20% $V_{CCO}$ to 30% $V_{CCO}$.<br>• Table 10: Corrected LVPECL_25 Min and Max values for $V_{IH}$ and $V_{IL}$. Added explanatory text above table.<br>• Table 13 and Table 14 (pin-pin and reg-reg performance): Changed device specified from XC2VP7FF672-6 to XC2VP20FF1152-6.<br>• Table 15: Updated to show devices XC2VP7 and XC2VP20 as Preliminary for the -6 speed grade and Production for the -5 speed grade.<br>• Removed former Table 32, Standard Capacitive Loads.<br>• Table 52: Updated $T_{TAPTCK}$ from 4.0 ns to 5.5 ns.<br>• Table 59: Modified footnote referenced at CLKFX/CLKFX180 to point to the online Jitter Calculator.<br>• Added Figure 6 and accompanying procedure for measuring standard adjustments. |
| 05/27/03 (cont'd) | 2.8 (cont'd) | • Table 1: Footnote (2) rewritten to specify “one or more banks.”<br>• Table 57: Some DCM parameters were erroneously missing from v2.8 (single-module version) due to a document compilation error. The concatenated full data sheet version was not affected. These parameters have been restored. |

*Table 7:* **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 |
| N/A | GND | R15 | | | |
| N/A | GND | R16 | | | |
| N/A | GND | R24 | | | |
| N/A | GND | T11 | | | |
| N/A | GND | T12 | | | |
| N/A | GND | T13 | | | |
| N/A | GND | T14 | | | |
| N/A | GND | T15 | | | |
| N/A | GND | T16 | | | |
| N/A | GND | U6 | | | |
| N/A | GND | U21 | | | |
| N/A | GND | W4 | | | |
| N/A | GND | W23 | | | |
| N/A | GND | AA10 | | | |
| N/A | GND | AA17 | | | |
| N/A | GND | AC4 | | | |
| N/A | GND | AC8 | | | |
| N/A | GND | AC19 | | | |
| N/A | GND | AC23 | | | |
| N/A | GND | AD3 | | | |
| N/A | GND | AD24 | | | |
| N/A | GND | AE2 | | | |
| N/A | GND | AE25 | | | |
| N/A | GND | AF1 | | | |
| N/A | GND | AF26 | | | |

**Notes:**
1. See Table 4 for an explanation of the signals available on this pin.

*Table 8:* **FF672 — XC2VP2, XC2VP4, and XC2VP7**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP2 | XC2VP4 | XC2VP7 |
| 2 | IO_L48P_2 | H1 | NC | | |
| 2 | IO_L49N_2 | J7 | NC | | |
| 2 | IO_L49P_2 | J6 | NC | | |
| 2 | IO_L50N_2 | J5 | NC | | |
| 2 | IO_L50P_2 | J4 | NC | | |
| 2 | IO_L51N_2 | J3 | NC | | |
| 2 | IO_L51P_2 | J2 | NC | | |
| 2 | IO_L52N_2/VREF_2 | K6 | NC | | |
| 2 | IO_L52P_2 | K5 | NC | | |
| 2 | IO_L53N_2 | K4 | NC | | |
| 2 | IO_L53P_2 | K3 | NC | | |
| 2 | IO_L54N_2 | J1 | NC | | |
| 2 | IO_L54P_2 | K1 | NC | | |
| 2 | IO_L55N_2 | K7 | NC | | |
| 2 | IO_L55P_2 | L8 | NC | | |
| 2 | IO_L56N_2 | L7 | NC | | |
| 2 | IO_L56P_2 | M7 | NC | | |
| 2 | IO_L57N_2 | L6 | NC | | |
| 2 | IO_L57P_2 | L5 | NC | | |
| 2 | IO_L58N_2/VREF_2 | L4 | NC | | |
| 2 | IO_L58P_2 | L3 | NC | | |
| 2 | IO_L59N_2 | L2 | NC | | |
| 2 | IO_L59P_2 | L1 | NC | | |
| 2 | IO_L60N_2 | M8 | NC | | |
| 2 | IO_L60P_2 | N8 | NC | | |
| 2 | IO_L85N_2 | M6 | | | |
| 2 | IO_L85P_2 | M5 | | | |
| 2 | IO_L86N_2 | M4 | | | |
| 2 | IO_L86P_2 | M3 | | | |
| 2 | IO_L87N_2 | M2 | | | |
| 2 | IO_L87P_2 | M1 | | | |
| 2 | IO_L88N_2/VREF_2 | N7 | | | |
| 2 | IO_L88P_2 | N6 | | | |
| 2 | IO_L89N_2 | N5 | | | |
| 2 | IO_L89P_2 | N4 | | | |
| 2 | IO_L90N_2 | N3 | | | |
| 2 | IO_L90P_2 | N2 | | | |

## FF1152 Flip-Chip Fine-Pitch BGA Package

As shown in Table 10, XC2VP20, XC2VP30, XC2VP40, and XC2VP50 Virtex-II Pro devices are available in the FF1152 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

*Table 10:* **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | | | |
|---|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 |
| 0 | IO_L01N_0/VRP_0 | E29 | | | | |
| 0 | IO_L01P_0/VRN_0 | E28 | | | | |
| 0 | IO_L02N_0 | H26 | | | | |
| 0 | IO_L02P_0 | G26 | | | | |
| 0 | IO_L03N_0 | H25 | | | | |
| 0 | IO_L03P_0/VREF_0 | G25 | | | | |
| 0 | IO_L05_0/No_Pair | J25 | | | | |
| 0 | IO_L06N_0 | K24 | | | | |
| 0 | IO_L06P_0 | J24 | | | | |
| 0 | IO_L07N_0 | F26 | | | | |
| 0 | IO_L07P_0 | E26 | | | | |
| 0 | IO_L08N_0 | D30 | | | | |
| 0 | IO_L08P_0 | D29 | | | | |
| 0 | IO_L09N_0 | K23 | | | | |
| 0 | IO_L09P_0/VREF_0 | J23 | | | | |
| 0 | IO_L19N_0 | F24 | NC | NC | | |
| 0 | IO_L19P_0 | E24 | NC | NC | | |
| 0 | IO_L20N_0 | D28 | NC | NC | | |
| 0 | IO_L20P_0 | C28 | NC | NC | | |
| 0 | IO_L21N_0 | H24 | NC | NC | | |
| 0 | IO_L21P_0 | G24 | NC | NC | | |
| 0 | IO_L25N_0 | G23 | NC | NC | | |
| 0 | IO_L25P_0 | F23 | NC | NC | | |
| 0 | IO_L26N_0 | E27 | NC | NC | | |
| 0 | IO_L26P_0 | D27 | NC | NC | | |
| 0 | IO_L27N_0 | K22 | NC | NC | | |
| 0 | IO_L27P_0/VREF_0 | J22 | NC | NC | | |
| 0 | IO_L37N_0 | H22 | | | | |
| 0 | IO_L37P_0 | G22 | | | | |
| 0 | IO_L38N_0 | D26 | | | | |
| 0 | IO_L38P_0 | C26 | | | | |
| 0 | IO_L39N_0 | K21 | | | | |
| 0 | IO_L39P_0 | J21 | | | | |
| 0 | IO_L43N_0 | F22 | | | | |

*Table 10:* **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | | | |
|---|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 |
| 1 | IO_L37N_1 | G13 | | | | |
| 1 | IO_L37P_1 | H13 | | | | |
| 1 | IO_L27N_1/VREF_1 | J13 | NC | NC | | |
| 1 | IO_L27P_1 | K13 | NC | NC | | |
| 1 | IO_L26N_1 | D8 | NC | NC | | |
| 1 | IO_L26P_1 | E8 | NC | NC | | |
| 1 | IO_L25N_1 | F12 | NC | NC | | |
| 1 | IO_L25P_1 | G12 | NC | NC | | |
| 1 | IO_L21N_1 | G11 | NC | NC | | |
| 1 | IO_L21P_1 | H11 | NC | NC | | |
| 1 | IO_L20N_1 | C7 | NC | NC | | |
| 1 | IO_L20P_1 | D7 | NC | NC | | |
| 1 | IO_L19N_1 | E11 | NC | NC | | |
| 1 | IO_L19P_1 | F11 | NC | NC | | |
| 1 | IO_L09N_1/VREF_1 | J12 | | | | |
| 1 | IO_L09P_1 | K12 | | | | |
| 1 | IO_L08N_1 | D6 | | | | |
| 1 | IO_L08P_1 | D5 | | | | |
| 1 | IO_L07N_1 | E9 | | | | |
| 1 | IO_L07P_1 | F9 | | | | |
| 1 | IO_L06N_1 | J11 | | | | |
| 1 | IO_L06P_1 | K11 | | | | |
| 1 | IO_L05_1/No_Pair | J10 | | | | |
| 1 | IO_L03N_1/VREF_1 | G10 | | | | |
| 1 | IO_L03P_1 | H10 | | | | |
| 1 | IO_L02N_1 | G9 | | | | |
| 1 | IO_L02P_1 | H9 | | | | |
| 1 | IO_L01N_1/VRP_1 | E7 | | | | |
| 1 | IO_L01P_1/VRN_1 | E6 | | | | |
| | | | | | | |
| 2 | IO_L01N_2/VRP_2 | D2 | | | | |
| 2 | IO_L01P_2/VRN_2 | D1 | | | | |
| 2 | IO_L02N_2 | F8 | | | | |
| 2 | IO_L02P_2 | F7 | | | | |
| 2 | IO_L03N_2 | E4 | | | | |
| 2 | IO_L03P_2 | E3 | | | | |
| 2 | IO_L04N_2/VREF_2 | E2 | | | | |
| 2 | IO_L04P_2 | E1 | | | | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| N/A | VCCINT | M23 | | |
| N/A | VCCINT | AB22 | | |
| N/A | VCCINT | AA22 | | |
| N/A | VCCINT | Y22 | | |
| N/A | VCCINT | W22 | | |
| N/A | VCCINT | V22 | | |
| N/A | VCCINT | U22 | | |
| N/A | VCCINT | T22 | | |
| N/A | VCCINT | R22 | | |
| N/A | VCCINT | P22 | | |
| N/A | VCCINT | N22 | | |
| N/A | VCCINT | AB21 | | |
| N/A | VCCINT | N21 | | |
| N/A | VCCINT | AB20 | | |
| N/A | VCCINT | N20 | | |
| N/A | VCCINT | AB19 | | |
| N/A | VCCINT | N19 | | |
| N/A | VCCINT | AB18 | | |
| N/A | VCCINT | N18 | | |
| N/A | VCCINT | AB17 | | |
| N/A | VCCINT | N17 | | |
| N/A | VCCINT | AB16 | | |
| N/A | VCCINT | N16 | | |
| N/A | VCCINT | AB15 | | |
| N/A | VCCINT | N15 | | |
| N/A | VCCINT | AB14 | | |
| N/A | VCCINT | N14 | | |
| N/A | VCCINT | AB13 | | |
| N/A | VCCINT | AA13 | | |
| N/A | VCCINT | Y13 | | |
| N/A | VCCINT | W13 | | |
| N/A | VCCINT | V13 | | |
| N/A | VCCINT | U13 | | |
| N/A | VCCINT | T13 | | |
| N/A | VCCINT | R13 | | |
| N/A | VCCINT | P13 | | |
| N/A | VCCINT | N13 | | |
| N/A | VCCINT | AC12 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 0 | IO_L59P_0 | N21 | | |
| 0 | IO_L60N_0 | E23 | | |
| 0 | IO_L60P_0 | F22 | | |
| 0 | IO_L64N_0 | D22 | | |
| 0 | IO_L64P_0 | E22 | | |
| 0 | IO_L65N_0 | H21 | | |
| 0 | IO_L65P_0 | H20 | | |
| 0 | IO_L66N_0 | G22 | | |
| 0 | IO_L66P_0/VREF_0 | G21 | | |
| 0 | IO_L67N_0 | D21 | | |
| 0 | IO_L67P_0 | E21 | | |
| 0 | IO_L68N_0 | J21 | | |
| 0 | IO_L68P_0 | K21 | | |
| 0 | IO_L69N_0 | C22 | | |
| 0 | IO_L69P_0/VREF_0 | C21 | | |
| 0 | IO_L73N_0 | F21 | | |
| 0 | IO_L73P_0 | F20 | | |
| 0 | IO_L74N_0/GCLK7P | L21 | | |
| 0 | IO_L74P_0/GCLK6S | M21 | | |
| 0 | IO_L75N_0/GCLK5P | D20 | | |
| 0 | IO_L75P_0/GCLK4S | E20 | | |
| | | | | |
| 1 | IO_L75N_1/GCLK3P | K20 | | |
| 1 | IO_L75P_1/GCLK2S | J20 | | |
| 1 | IO_L74N_1/GCLK1P | N20 | | |
| 1 | IO_L74P_1/GCLK0S | M20 | | |
| 1 | IO_L73N_1 | E19 | | |
| 1 | IO_L73P_1 | D19 | | |
| 1 | IO_L69N_1/VREF_1 | G19 | | |
| 1 | IO_L69P_1 | F19 | | |
| 1 | IO_L68N_1 | L19 | | |
| 1 | IO_L68P_1 | K19 | | |
| 1 | IO_L67N_1 | J19 | | |
| 1 | IO_L67P_1 | H19 | | |
| 1 | IO_L66N_1/VREF_1 | C19 | | |
| 1 | IO_L66P_1 | C18 | | |
| 1 | IO_L65N_1 | N19 | | |
| 1 | IO_L65P_1 | M19 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 3 | IO_L47P_3 | AC10 | | |
| 3 | IO_L46N_3 | AE7 | | |
| 3 | IO_L46P_3 | AE8 | | |
| 3 | IO_L45N_3/VREF_3 | AE5 | | |
| 3 | IO_L45P_3 | AE6 | | |
| 3 | IO_L44N_3 | AB13 | | |
| 3 | IO_L44P_3 | AC13 | | |
| 3 | IO_L43N_3 | AE3 | | |
| 3 | IO_L43P_3 | AE4 | | |
| 3 | IO_L42N_3 | AE1 | | |
| 3 | IO_L42P_3 | AE2 | | |
| 3 | IO_L41N_3 | AD10 | | |
| 3 | IO_L41P_3 | AD11 | | |
| 3 | IO_L40N_3 | AF6 | | |
| 3 | IO_L40P_3 | AF7 | | |
| 3 | IO_L39N_3/VREF_3 | AF4 | | |
| 3 | IO_L39P_3 | AF5 | | |
| 3 | IO_L38N_3 | AC12 | | |
| 3 | IO_L38P_3 | AD12 | | |
| 3 | IO_L37N_3 | AF1 | | |
| 3 | IO_L37P_3 | AF2 | | |
| 3 | IO_L36N_3 | AG6 | | |
| 3 | IO_L36P_3 | AG7 | | |
| 3 | IO_L35N_3 | AE9 | | |
| 3 | IO_L35P_3 | AE10 | | |
| 3 | IO_L34N_3 | AF3 | | |
| 3 | IO_L34P_3 | AG3 | | |
| 3 | IO_L33N_3/VREF_3 | AG1 | | |
| 3 | IO_L33P_3 | AG2 | | |
| 3 | IO_L32N_3 | AE11 | | |
| 3 | IO_L32P_3 | AE12 | | |
| 3 | IO_L31N_3 | AH6 | | |
| 3 | IO_L31P_3 | AH7 | | |
| 3 | IO_L30N_3 | AG5 | | |
| 3 | IO_L30P_3 | AH4 | | |
| 3 | IO_L29N_3 | AD13 | | |
| 3 | IO_L29P_3 | AE13 | | |
| 3 | IO_L28N_3 | AH2 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 4 | IO_L87P_4/VREF_4 | | AP15 | NC | |
| 4 | IO_L37N_4 | | AV15 | | |
| 4 | IO_L37P_4 | | AU15 | | |
| 4 | IO_L38N_4 | | AY14 | | |
| 4 | IO_L38P_4 | | AY15 | | |
| 4 | IO_L39N_4 | | AM16 | | |
| 4 | IO_L39P_4 | | AL16 | | |
| 4 | IO_L43N_4 | | AP16 | | |
| 4 | IO_L43P_4 | | AN16 | | |
| 4 | IO_L44N_4 | | AR16 | | |
| 4 | IO_L44P_4 | | AT16 | | |
| 4 | IO_L45N_4 | | AV16 | | |
| 4 | IO_L45P_4/VREF_4 | | AU16 | | |
| 4 | IO_L46N_4 | | AL18 | | |
| 4 | IO_L46P_4 | | AL17 | | |
| 4 | IO_L47N_4 | | AM17 | | |
| 4 | IO_L47P_4 | | AN17 | | |
| 4 | IO_L48N_4 | | AR17 | | |
| 4 | IO_L48P_4 | | AP17 | | |
| 4 | IO_L49N_4 | | AU17 | | |
| 4 | IO_L49P_4 | | AT17 | | |
| 4 | IO_L50_4/No_Pair | | AW16 | | |
| 4 | IO_L53_4/No_Pair | | AW17 | | |
| 4 | IO_L54N_4 | | AN18 | | |
| 4 | IO_L54P_4 | | AM18 | | |
| 4 | IO_L55N_4 | | AT18 | | |
| 4 | IO_L55P_4 | | AR18 | | |
| 4 | IO_L56N_4 | | AV17 | | |
| 4 | IO_L56P_4 | | AV18 | | |
| 4 | IO_L57N_4 | | AY18 | | |
| 4 | IO_L57P_4/VREF_4 | | AY17 | | |
| 4 | IO_L58N_4 | | AM19 | | |
| 4 | IO_L58P_4 | | AL19 | | |
| 4 | IO_L59N_4 | | AP19 | | |
| 4 | IO_L59P_4 | | AN19 | | |
| 4 | IO_L60N_4 | | AT19 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| N/A | RXPPAD17 | | BB15 | | |
| N/A | GNDA17 | | AY16 | | |
| N/A | TXPPAD17 | | BB16 | | |
| N/A | TXNPAD17 | | BB17 | | |
| N/A | VTTXPAD17 | | BA17 | | |
| N/A | AVCCAUXTX17 | | BA16 | | |
| N/A | AVCCAUXRX18 | | BA18 | | |
| N/A | VTRXPAD18 | | BA19 | | |
| N/A | RXNPAD18 | | BB18 | | |
| N/A | RXPPAD18 | | BB19 | | |
| N/A | GNDA18 | | AY21 | | |
| N/A | TXPPAD18 | | BB20 | | |
| N/A | TXNPAD18 | | BB21 | | |
| N/A | VTTXPAD18 | | BA21 | | |
| N/A | AVCCAUXTX18 | | BA20 | | |
| N/A | AVCCAUXRX19 | | BA22 | | |
| N/A | VTRXPAD19 | | BA23 | | |
| N/A | RXNPAD19 | | BB22 | | |
| N/A | RXPPAD19 | | BB23 | | |
| N/A | GNDA19 | | AY22 | | |
| N/A | TXPPAD19 | | BB24 | | |
| N/A | TXNPAD19 | | BB25 | | |
| N/A | VTTXPAD19 | | BA25 | | |
| N/A | AVCCAUXTX19 | | BA24 | | |
| N/A | AVCCAUXRX20 | | BA26 | | |
| N/A | VTRXPAD20 | | BA27 | | |
| N/A | RXNPAD20 | | BB26 | | |
| N/A | RXPPAD20 | | BB27 | | |
| N/A | GNDA20 | | AY27 | | |
| N/A | TXPPAD20 | | BB28 | | |
| N/A | TXNPAD20 | | BB29 | | |
| N/A | VTTXPAD20 | | BA29 | | |
| N/A | AVCCAUXTX20 | | BA28 | | |
| N/A | AVCCAUXRX21 | | BA30 | | |
| N/A | VTRXPAD21 | | BA31 | | |
| N/A | RXNPAD21 | | BB30 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| N/A | GND | | AB18 | | |
| N/A | GND | | AB17 | | |
| N/A | GND | | AB11 | | |
| N/A | GND | | AB8 | | |
| N/A | GND | | AB5 | | |
| N/A | GND | | AC41 | | |
| N/A | GND | | AC26 | | |
| N/A | GND | | AC25 | | |
| N/A | GND | | AC24 | | |
| N/A | GND | | AC23 | | |
| N/A | GND | | AC22 | | |
| N/A | GND | | AC21 | | |
| N/A | GND | | AC20 | | |
| N/A | GND | | AC19 | | |
| N/A | GND | | AC18 | | |
| N/A | GND | | AC17 | | |
| N/A | GND | | AC2 | | |
| N/A | GND | | AD26 | | |
| N/A | GND | | AD25 | | |
| N/A | GND | | AD24 | | |
| N/A | GND | | AD23 | | |
| N/A | GND | | AD22 | | |
| N/A | GND | | AD21 | | |
| N/A | GND | | AD20 | | |
| N/A | GND | | AD19 | | |
| N/A | GND | | AD18 | | |
| N/A | GND | | AD17 | | |
| N/A | GND | | AE37 | | |
| N/A | GND | | AE34 | | |
| N/A | GND | | AE26 | | |
| N/A | GND | | AE25 | | |
| N/A | GND | | AE24 | | |
| N/A | GND | | AE23 | | |
| N/A | GND | | AE22 | | |
| N/A | GND | | AE21 | | |
| N/A | GND | | AE20 | | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 0 | IO_L34P_0 | C30 | |
| 0 | IO_L35N_0 | L29 | |
| 0 | IO_L35P_0 | M29 | |
| 0 | IO_L36N_0 | H28 | |
| 0 | IO_L36P_0/VREF_0 | G29 | |
| 0 | IO_L76N_0 | E29 | |
| 0 | IO_L76P_0 | F29 | |
| 0 | IO_L77N_0 | J29 | |
| 0 | IO_L77P_0 | K29 | |
| 0 | IO_L78N_0 | D28 | |
| 0 | IO_L78P_0 | C29 | |
| 0 | IO_L79N_0 | A29 | |
| 0 | IO_L79P_0 | B29 | |
| 0 | IO_L80_0/No_Pair | L28 | |
| 0 | IO_L83_0/No_Pair | M28 | |
| 0 | IO_L84N_0 | G27 | |
| 0 | IO_L84P_0 | G28 | |
| 0 | IO_L85N_0 | E28 | |
| 0 | IO_L85P_0 | F28 | |
| 0 | IO_L86N_0 | J28 | |
| 0 | IO_L86P_0 | K28 | |
| 0 | IO_L87N_0 | C27 | |
| 0 | IO_L87P_0/VREF_0 | C28 | |
| 0 | IO_L37N_0 | A28 | |
| 0 | IO_L37P_0 | B28 | |
| 0 | IO_L38N_0 | L27 | |
| 0 | IO_L38P_0 | M27 | |
| 0 | IO_L39N_0 | H26 | |
| 0 | IO_L39P_0 | H27 | |
| 0 | IO_L43N_0 | E27 | |
| 0 | IO_L43P_0 | F27 | |
| 0 | IO_L44N_0 | J27 | |
| 0 | IO_L44P_0 | K27 | |
| 0 | IO_L45N_0 | D26 | |
| 0 | IO_L45P_0/VREF_0 | D27 | |
| 0 | IO_L10N_0 | A27 | NC |
| 0 | IO_L10P_0 | B27 | NC |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 4 | IO_L58P_4 | AW19 | |
| 4 | IO_L59N_4 | AP19 | |
| 4 | IO_L59P_4 | AN19 | |
| 4 | IO_L60N_4 | BB19 | |
| 4 | IO_L60P_4 | BA19 | |
| 4 | IO_L64N_4 | AU20 | |
| 4 | IO_L64P_4 | AT20 | |
| 4 | IO_L65N_4 | AL21 | |
| 4 | IO_L65P_4 | AL20 | |
| 4 | IO_L66N_4 | BA20 | |
| 4 | IO_L66P_4/VREF_4 | AY20 | |
| 4 | IO_L67N_4 | AR21 | |
| 4 | IO_L67P_4 | AP21 | |
| 4 | IO_L68N_4 | AN20 | |
| 4 | IO_L68P_4 | AM20 | |
| 4 | IO_L69N_4 | AU21 | |
| 4 | IO_L69P_4/VREF_4 | AT21 | |
| 4 | IO_L73N_4 | AW21 | |
| 4 | IO_L73P_4 | AV21 | |
| 4 | IO_L74N_4/GCLK3S | AN21 | |
| 4 | IO_L74P_4/GCLK2P | AM21 | |
| 4 | IO_L75N_4/GCLK1S | BA21 | |
| 4 | IO_L75P_4/GCLK0P | AY21 | |
| | | | |
| 5 | IO_L75N_5/GCLK7S | AY22 | |
| 5 | IO_L75P_5/GCLK6P | BA22 | |
| 5 | IO_L74N_5/GCLK5S | AM22 | |
| 5 | IO_L74P_5/GCLK4P | AN22 | |
| 5 | IO_L73N_5 | AV22 | |
| 5 | IO_L73P_5 | AW22 | |
| 5 | IO_L69N_5/VREF_5 | AT22 | |
| 5 | IO_L69P_5 | AU22 | |
| 5 | IO_L68N_5 | AM23 | |
| 5 | IO_L68P_5 | AN23 | |
| 5 | IO_L67N_5 | AP22 | |
| 5 | IO_L67P_5 | AR22 | |
| 5 | IO_L66N_5/VREF_5 | AY23 | |