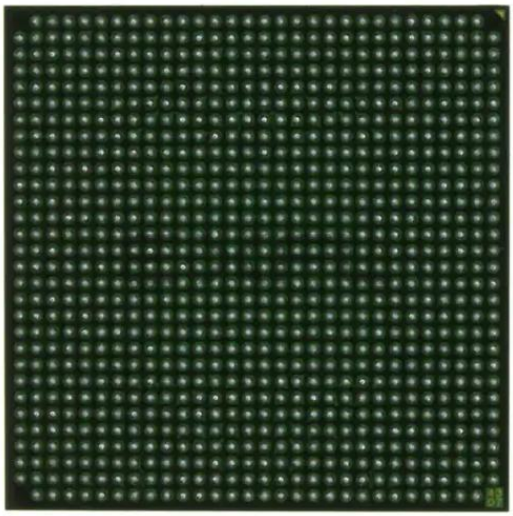

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2320
Number of Logic Elements/Cells	20880
Total RAM Bits	1622016
Number of I/O	556
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp20-7ffg896c

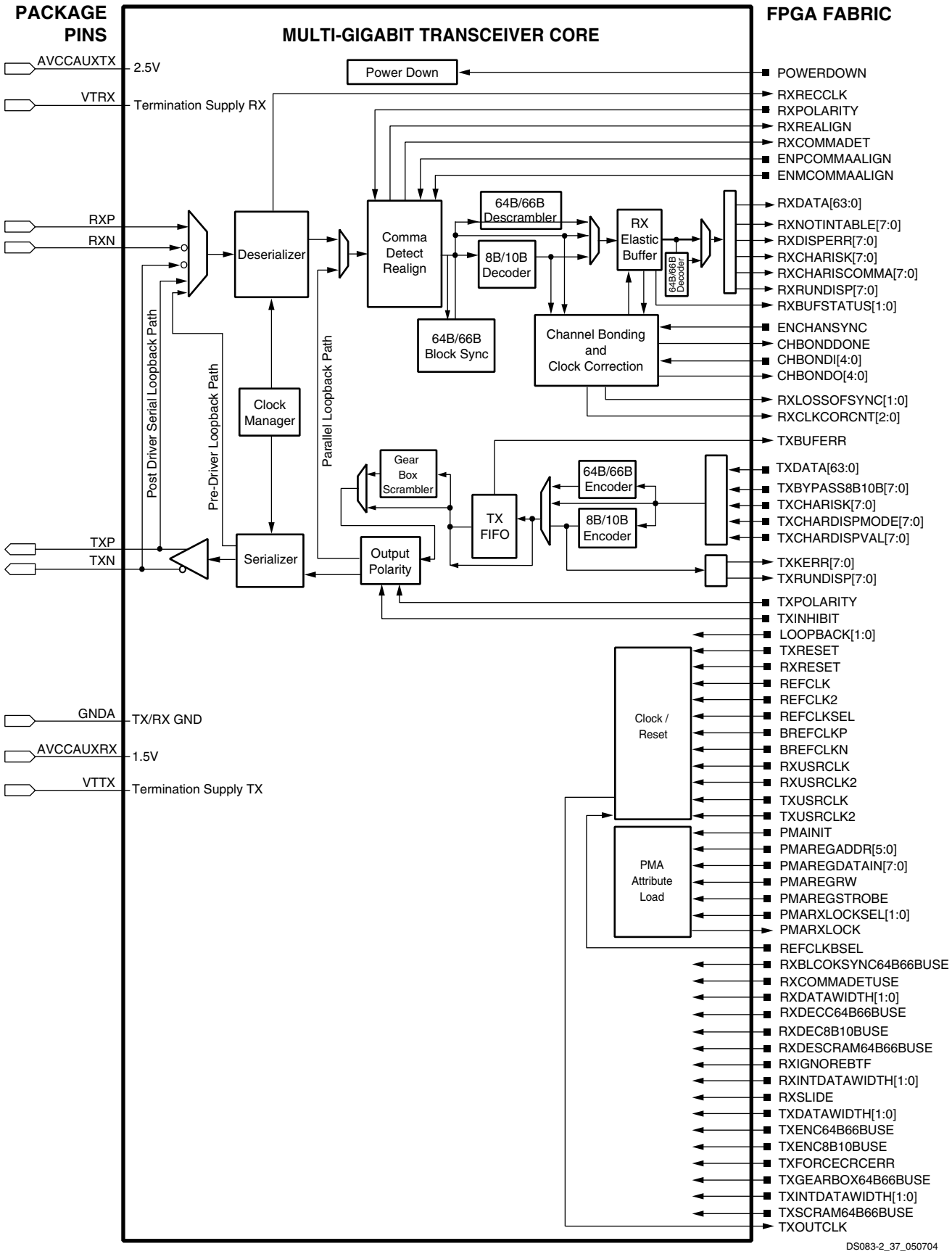


Figure 4: **RocketIO X Transceiver Block Diagram**

Functional Description: RocketIO Multi-Gigabit Transceiver (MGT)

This section summarizes the features of the RocketIO multi-gigabit transceiver. For an in-depth discussion of the RocketIO MGT, including digital and analog design considerations, refer to the ***RocketIO Transceiver User Guide***.

RocketIO Overview

Up to twenty RocketIO MGTs are available. The MGT is designed to operate at any baud rate in the range of 622 Mb/s to 3.125 Gb/s per channel. This includes specific baud rates used by various standards as listed in Table 4.

The RocketIO MGT consists of the *Physical Media Attachment* (PMA) and *Physical Coding Sublayer* (PCS). The PMA contains the 3.125 Gb/s serializer/deserializer (SERDES), TX/RX buffers, clock generator, and clock recovery circuitry. The PCS contains the bypassable 8B/10B encoder/ decoder, elastic buffers, and Cyclic Redundancy Check (CRC) units. The encoder and decoder handle the 8B/10B coding scheme. The elastic buffers support the clock correction (rate matching) and channel bonding features. The CRC units perform CRC generation and checking.

See Table 7, page 17, for a summary of the differences between the RocketIO X PMA/PCS and the RocketIO PMA/PCS.

Figure 10, page 11 shows a high-level block diagram of the RocketIO transceiver and its FPGA interface signals.

Table 4: **Protocols Supported by RocketIO Transceiver**

Mode	Channels (Lanes)(1)	I/O Bit Rate (Gb/s)
Fibre Channel	1	1.06
		2.12
		3.1875 (2)
Gigabit Ethernet	1	1.25
10Gbit Ethernet	4	3.125
Infiniband	1, 4, 12	2.5
Aurora	1, 2, 3, 4, ...	0.622 – 3.125
Custom Protocol	1, 2, 3, 4, ...	up to 3.125

Notes:
1. One channel is considered to be one transceiver.
2. Virtex-II Pro MGT can support the 10G Fibre Channel data rates of 3.1875 Gb/s across 6" of standard FR-4 PCB and one connector (Molex 74441 or equivalent) with a bit error rate of 10^{-12} or better.

PMA

Transmitter Output

The RocketIO transceiver is implemented in *Current Mode Logic* (CML). A CML transmitter output consists of transistors configured as shown in Figure 8. CML uses a positive supply and offers easy interface requirements. In this configuration, both legs of the driver, VP and VN, sink current, with one leg always sinking more current than its complement. The CML output consists of a differential pair with 50Ω (or, optionally, 75Ω) source resistors. The signal swing is created by switching the current in a common-source differential pair.

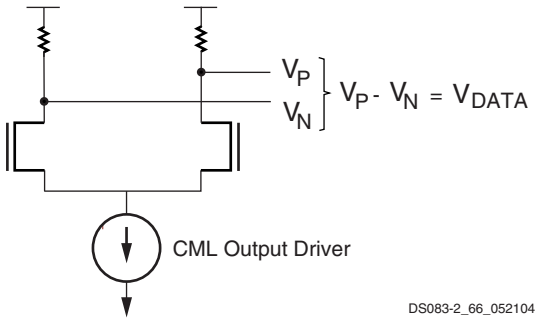


Figure 8: **CML Output Configuration**

Transmitter Termination

On-chip termination is provided at the transmitter, eliminating the need for external termination. The output driver and termination are powered by V_{TTX}. This configuration uses a CML approach with selectable 50Ω or 75Ω termination to TXP and TXN as shown in Figure 9.

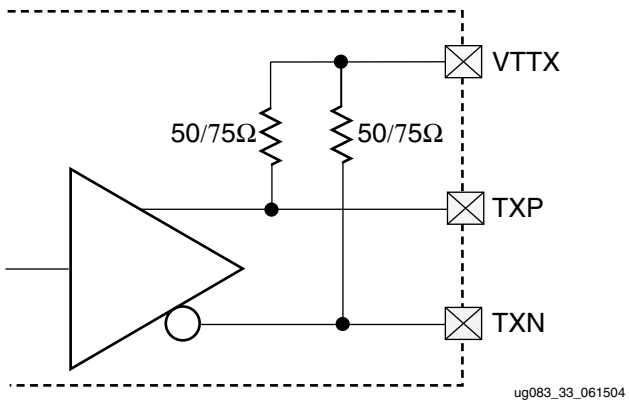
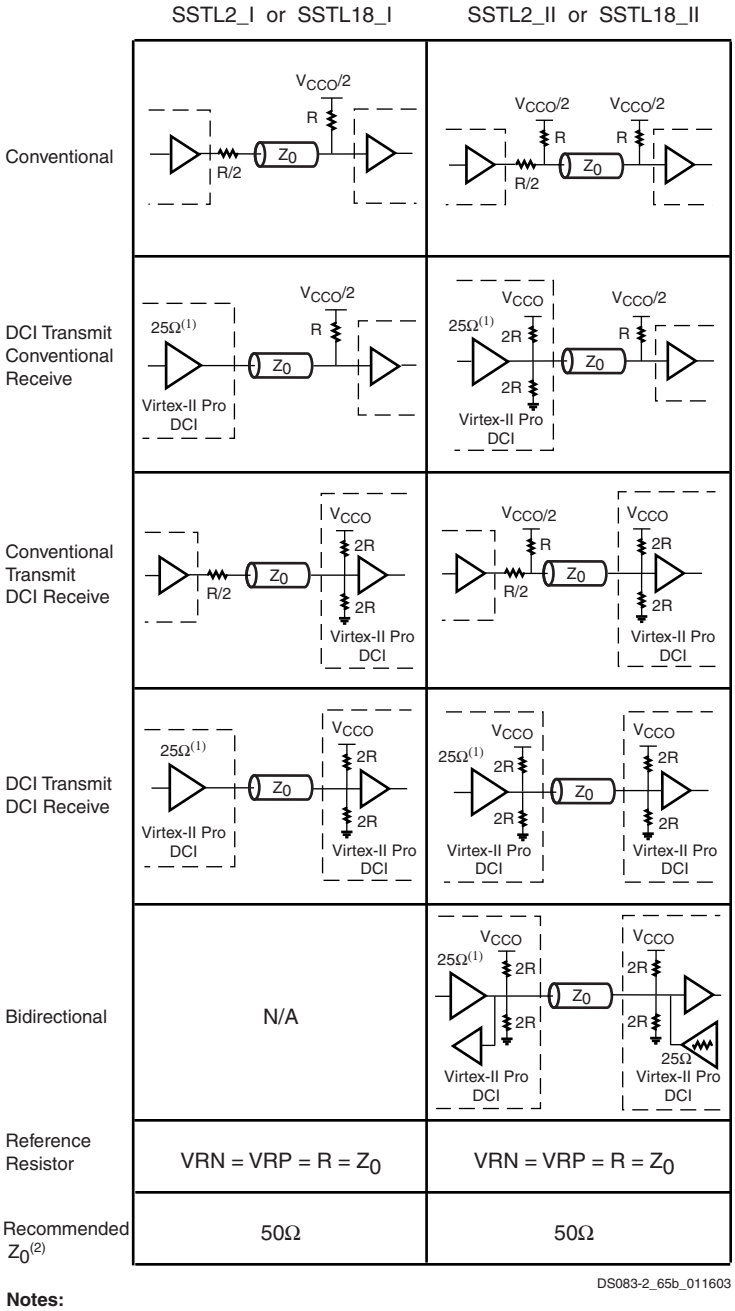


Figure 9: **RocketIO Transmit Termination**

Figure 29 provides examples illustrating the use of the SSTL2_I_DCI, SSTL2_II_DCI, SSTL18_I_DCI, and SSTL18_II_DCI I/O standards. For a complete list, see the ***Virtex-II Pro Platform FPGA User Guide***.



Notes:
1. The SSTL-compatible 25Ω series resistor is accounted for in the DCI buffer, and it is not DCI controlled.
2. Z_0 is the recommended PCB trace impedance.

Figure 29: **SSTL DCI Usage Examples**

Configurable Logic Blocks (CLBs)

The Virtex-II Pro configurable logic blocks (CLB) are organized in an array and are used to build combinatorial and synchronous logic designs. Each CLB element is tied to a switch matrix to access the general routing matrix, as shown in Figure 32. A CLB element comprises 4 similar slices, with fast local feedback within the CLB. The four slices are split in two columns of two slices with two independent carry logic chains and one common shift chain.

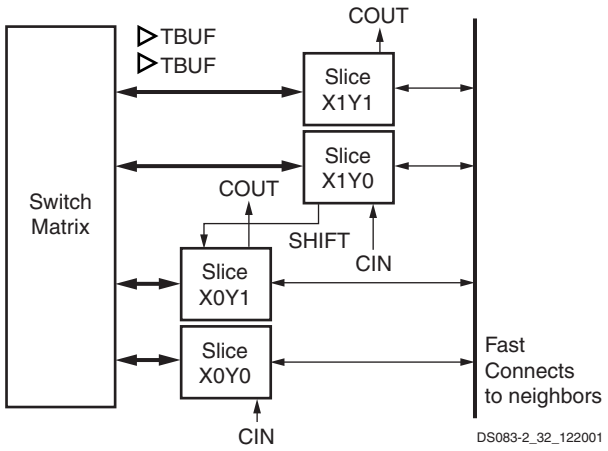


Figure 32: **Virtex-II Pro CLB Element**

Slice Description

Each slice includes two 4-input function generators, carry logic, arithmetic logic gates, wide function multiplexers and two storage elements. As shown in Figure 33, each 4-input function generator is programmable as a 4-input LUT, 16 bits of distributed SelectRAM+ memory, or a 16-bit variable-tap shift register element.

The output from the function generator in each slice drives both the slice output and the D input of the storage element. Figure 34 shows a more detailed view of a single slice.

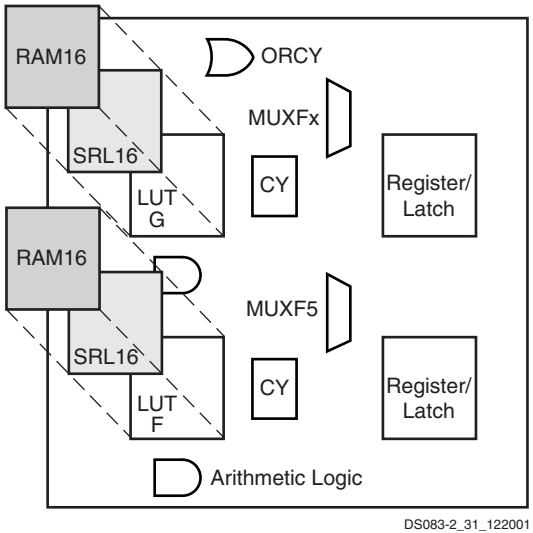


Figure 33: **Virtex-II Pro Slice Configuration**

Configurations

Look-Up Table

Virtex-II Pro function generators are implemented as 4-input look-up tables (LUTs). Four independent inputs are provided to each of the two function generators in a slice (F and G). These function generators are each capable of implementing any arbitrarily defined boolean function of four inputs. The propagation delay is therefore independent of the function implemented. Signals from the function generators can exit the slice (X or Y output), can input the XOR dedicated gate (see arithmetic logic), or input the carry-logic multiplexer (see fast look-ahead carry logic), or feed the D input of the storage element, or go to the MUXF5 (not shown in Figure 34).

In addition to the basic LUTs, the Virtex-II Pro slice contains logic (MUXF5 and MUXFX multiplexers) that combines function generators to provide any function of five, six, seven, or eight inputs. The MUXFX is either MUXF6, MUXF7, or MUXF8 according to the slice considered in the CLB. Selected functions up to nine inputs (MUXF5 multiplexer) can be implemented in one slice. The MUXFX can also be a MUXF6, MUXF7, or MUXF8 multiplexer to map any function of six, seven, or eight inputs and selected wide logic functions.

Register/Latch

The storage elements in a Virtex-II Pro slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D input can be directly driven by the X or Y output via the DX or DY input, or by the slice inputs bypassing the function generators via the BX or BY input. The clock enable signal (CE) is active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

In addition to clock (CK) and clock enable (CE) signals, each slice has set and reset signals (SR and BY slice inputs). SR forces the storage element into the state specified by the attribute SRHIGH or SRLOW. SRHIGH forces a logic 1 when SR is asserted. SRLOW forces a logic 0. When SR is used, an optional second input (BY) forces the storage element into the opposite state via the REV pin. The reset condition is predominant over the set condition. (See Figure 35.)

The initial state after configuration or global initial state is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1. For each slice, set and reset can be set to be synchronous or asynchronous. Virtex-II Pro devices also have the ability to set INIT0 and INIT1 independent of SRHIGH and SRLOW.

The control signals clock (CLK), clock enable (CE) and set/reset (SR) are common to both storage elements in one slice. All of the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

synchronously. The sequence can also be paused at any stage, until lock has been achieved on any or all DCMs, as well as DCI.

Readback

In this mode, configuration data from the Virtex-II Pro FPGA device can be read back. Readback is supported only in the SelectMAP (master and slave) and Boundary-Scan mode.

Along with the configuration data, it is possible to read back the contents of all registers, distributed SelectRAM+, and block RAM resources. This capability is used for real-time debugging. For more detailed configuration information, see the *Virtex-II Pro Platform FPGA User Guide.*

Bitstream Encryption

Virtex-II Pro devices have an on-chip decryptor using one or two sets of three keys for triple-key Data Encryption Standard (DES) operation. Xilinx software tools offer an optional encryption of the configuration data (bitstream) with a triple-key DES determined by the designer.

The keys are stored in the FPGA by JTAG instruction and retained by a battery connected to the V_{BATT} pin, when the device is not powered. Virtex-II Pro devices can be configured with the corresponding encrypted bitstream, using any of the configuration modes described previously.

A detailed description of how to use bitstream encryption is provided in the ***Virtex-II Pro Platform FPGA User Guide***. Your local FAE can also provide specific information on this feature.

Partial Reconfiguration

Partial reconfiguration of Virtex-II Pro devices can be accomplished in either Slave SelectMAP mode or Boundary-Scan mode. Instead of resetting the chip and doing a full configuration, new data is loaded into a specified area of the chip, while the rest of the chip remains in operation. Data is loaded on a column basis, with the smallest load unit being a configuration “frame” of the bitstream (device size dependent).

Partial reconfiguration is useful for applications that require different designs to be loaded into the same area of a chip, or that require the ability to change portions of a design without having to reset or reconfigure the entire chip.

For more information on Partial Reconfiguration in Virtex-II Pro devices, please refer to Xilinx Application Note **XAPP290**, *Two Flows for Partial Reconfiguration*.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/13/02	2.0	New Virtex-II Pro family members. New timing parameters per speedsfile **v1.62**.
09/03/02	2.1	• Revised Reset and Power sections. • Updated Table 8, which lists compatible input standards. [Table deleted in v2.6.] • Added Figure 28, Figure 29, and Figure 30, which provide examples illustrating the use of I/O standards.
09/27/02	2.2	• In section RocketIO Overview, corrected max number of MGTs from 16 to 24. • In section Input/Output Blocks (IOBs), added references to XAPP653 regarding implementation of 3.3V I/O standards.
11/20/02	2.3	• Table 8: Added rows for LVTTL, LVCMOS33, and PCI-X. • Table 8: Added LVTTL and LVCMOS33 to compatible 3.3V cells. [Table deleted in v2.6.] • Table 33: Correct bitstream lengths.
12/03/02	2.4	• Added mention of LVTTL and PCI with respect to SelectIO-Ultra configurations. See section Input/Output Individual Options and Figure 22.
01/20/03	2.5	• Added qualification to features vs. Virtex-II (open-drain output pin TDO does not have internal pull-up resistor) • Table 7: Added HSTL18 (I, II, III, & IV) and HSTL18_DCI (I,II, III & IV) to 1.8V VCCO row. [Table deleted in v2.6.] • Table 8: Numerous revisions. [Table deleted in v2.6.]

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The V_{CCINT} power supply must ramp on, monotonically, no faster than 200 µs and no slower than 50 ms. Ramp-on is defined as: 0 V_{DC} to minimum supply voltages (see Table 2).

V_{CCAUX} and V_{CCO} can power on at any ramp rate. Power supplies can be turned on in any sequence.

Table 5 shows the minimum current required by Virtex-II Pro devices for proper power-on and configuration.

If the current minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

Once initialized and configured, use the power calculator to estimate current drain on these supplies.

For more information on V_{CCAUX}, V_{CCO}, and configuration mode, refer to Chapter 3 in the *Virtex-II Pro Platform FPGA User Guide*.

Table 5: **Power-On Current for Virtex-II Pro Devices**

Symbol	Device											Units
	XC2VP2	XC2VP4	XC2VP7	XC2VP20	XC2VPX20	XC2VP30	XC2VP40	XC2VP50	XC2VP70	XC2VPX70	XC2VP100	
$I_{CCINTMIN}$	500	500	500	600	600	800	1050	1250	1700	1700	2200	mA
$I_{CCAUXMIN}$	250	250	250	250	250	250	250	250	250	250	250	mA
I_{CCOMIN}	100	100	100	100	100	100	100	100	100	100	100	mA

Notes:
1. Power-on current parameter values are specified for Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.5.
2. I_{CCOMIN} values listed here apply to the entire device (all banks).

General Power Supply Requirements

Proper decoupling of all FPGA power supplies is essential. Consult Xilinx Application Note **XAPP623** for detailed information on power distribution system design.

V_{CCAUX} powers critical resources in the FPGA. Therefore, this supply voltage is especially susceptible to power supply noise. V_{CCAUX} can share a power plane with V_{CCO}, but only if V_{CCO} does not have excessive noise. Staying within simultaneously switching output (SSO) limits is essential for keeping power supply noise to a minimum. Refer to **XAPP689**, "Managing Ground Bounce in Large FPGAs," to determine the number of simultaneously switching outputs allowed per bank at the package level.

Changes in V_{CCAUX} voltage beyond 200 mV peak-to-peak should take place at a rate no faster than 10 mV per millisecond.

Recommended practices that can help reduce jitter and period distortion are described in Xilinx Answer Record 13756.

Table 38: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
HSTL, Class II	HSTL_II	T_{OHSTL_II}	0.30	0.35	0.38	ns
HSTL, Class III	HSTL_III	T_{OHSTL_IIII}	0.31	0.35	0.39	ns
HSTL, Class IV	HSTL_IV	T_{OHSTL_IV}	0.15	0.17	0.19	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{OHSTL\_I\_18}$	0.56	0.64	0.70	ns
HSTL, Class II, 1.8V	HSTL_II_18	$T_{OHSTL\_II\_18}$	0.30	0.35	0.38	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{OHSTL\_IIII\_18}$	0.36	0.41	0.45	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{OHSTL\_IV\_18}$	0.19	0.22	0.24	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{OSSTL18\_I}$	0.80	0.92	1.01	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{OSSTL18\_II}$	0.45	0.51	0.56	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{OSSTL2_I}	0.63	0.72	0.79	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{OSSTL2_II}	0.22	0.25	0.27	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{OLVDCI_33}	0.72	0.83	0.91	ns
LVDCI, 2.5V	LVDCI_25	T_{OLVDCI_25}	0.56	0.64	0.71	ns
LVDCI, 1.8V	LVDCI_18	T_{OLVDCI_18}	0.65	0.75	0.82	ns
LVDCI, 1.5V	LVDCI_15	T_{OLVDCI_15}	1.00	1.15	1.26	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{OLVDCI\_DV2\_25}$	0.06	0.07	0.08	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{OLVDCI\_DV2\_18}$	0.30	0.34	0.38	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{OLVDCI\_DV2\_15}$	0.60	0.69	0.76	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{OHSLVDCI\_15}$	1.00	1.15	1.26	ns
HSLVDCI, 1.8V	HSLVDCI_18	$T_{OHSLVDCI\_18}$	0.65	0.75	0.82	ns
HSLVDCI, 2.5V	HSLVDCI_25	$T_{OHSLVDCI\_25}$	0.56	0.64	0.71	ns
HSLVDCI, 3.3V	HSLVDCI_33	$T_{OHSLVDCI\_33}$	0.72	0.83	0.91	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T_{OGTL_DCI}	1.21	1.39	1.53	ns
GTL Plus with DCI	GTLP_DCI	T_{OGTLP_DCI}	0.05	0.06	0.07	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	$T_{OHSTL\_I\_DCI}$	0.55	0.63	0.69	ns
HSTL, Class II, with DCI	HSTL_II_DCI	$T_{OHSTL\_II\_DCI}$	0.47	0.54	0.60	ns
HSTL, Class III, with DCI	HSTL_III_DCI	$T_{OHSTL\_III\_DCI}$	0.31	0.36	0.40	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	$T_{OHSTL\_IV\_DCI}$	1.81	2.08	2.29	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	$T_{OHSTL\_I\_DCI\_18}$	0.55	0.63	0.70	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	$T_{OHSTL\_II\_DCI\_18}$	0.24	0.28	0.31	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	$T_{OHSTL\_III\_DCI\_18}$	0.35	0.40	0.44	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	$T_{OHSTL\_IV\_DCI\_18}$	1.48	1.70	1.87	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	$T_{OSSTL18\_I\_DCI}$	0.54	0.62	0.68	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	$T_{OSSTL18\_II\_DCI}$	0.24	0.28	0.31	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	$T_{OSSTL2\_I\_DCI}$	0.48	0.56	0.61	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	$T_{OSSTL2\_II\_DCI}$	0.48	0.56	0.61	ns

Master/Slave Serial Mode Parameters

Clock timing for Slave Serial configuration programming is shown in Figure 8, with Master Serial clock timing shown in Figure 9. Programming parameters for both Slave and Master modes are given in Table 50.

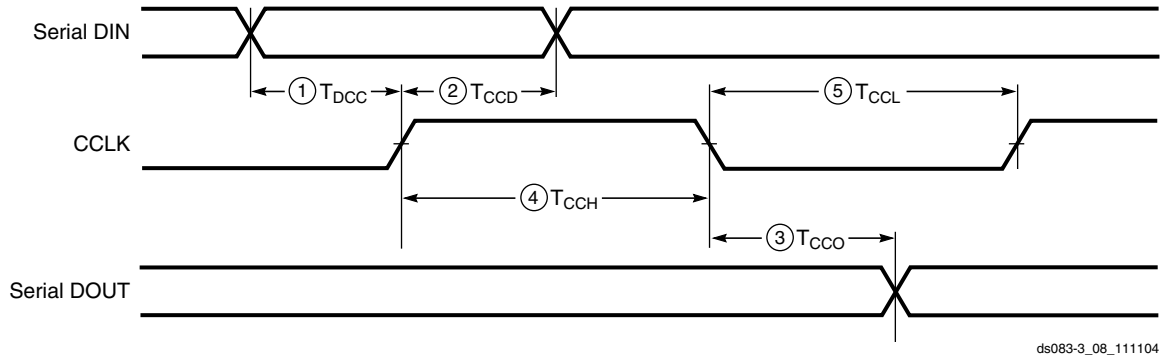


Figure 8: **Slave Serial Mode Timing Sequence**

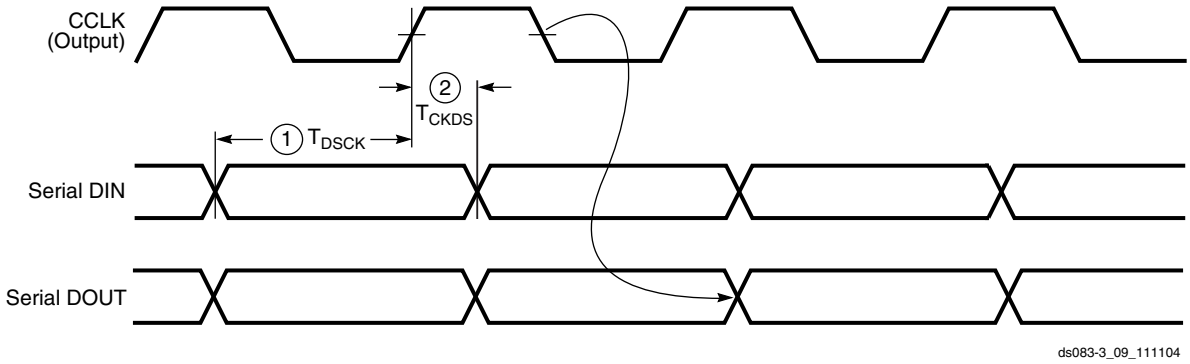


Figure 9: **Master Serial Mode Timing Sequence**

Table 50: **Master/Slave Serial Mode Timing Characteristics**

	Description	Figure References	Symbol	Value	Units
CCLK	DIN setup/hold, slave mode (Figure 8)	1/2	T_{DCC}/T_{CCD}	5.0/0.0	ns, min
	DIN setup/hold, master mode (Figure 9)	1/2	T_{DSCK}/T_{CKDS}	5.0/0.0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum start-up frequency		$F_{CC\_STARTUP}$	50	MHz, max
	Maximum frequency		F_{CC_SERIAL}	66(1)	MHz, max
	Frequency tolerance, master mode with respect to nominal			+45% –30%	

Notes:
1. If no provision is made in the design to adjust the frequency of CCLK, F_{CC_SERIAL} should not exceed $F_{CC\_STARTUP}$.

Virtex-II Pro Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM

Table 55: **Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1) For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25.						
No Delay Global Clock and IFF(2) with DCM	T_{PSDCM}/T_{PHDCM}	XC2VP2	1.54/–0.58	1.54/–0.57	1.54/–0.56	ns
		XC2VP4	1.59/–0.59	1.59/–0.58	1.59/–0.57	ns
		XC2VP7	1.66/–0.61	1.66/–0.59	1.66/–0.57	ns
		XC2VP20	1.68/–0.53	1.68/–0.53	1.68/–0.50	ns
		XC2VPX20	1.68/–0.53	1.68/–0.53	1.68/–0.50	ns
		XC2VP30	1.81/–0.74	1.81/–0.74	1.81/–0.71	ns
		XC2VP40	1.85/–0.65	1.85/–0.64	1.85/–0.60	ns
		XC2VP50	1.85/–0.57	1.85/–0.54	1.85/–0.50	ns
		XC2VP70	1.86/–0.45	1.86/–0.39	1.86/–0.30	ns
		XC2VPX70	1.86/–0.45	1.86/–0.39	1.86/–0.30	ns
		XC2VP100	N/A	1.86/–0.35	1.87/–0.28	ns

Notes:

1. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case duty-cycle distortion using CLK0 and CLK180, T_{DCD_CLK180}.
3. IFF = Input Flip-Flop or Latch

Table 65: **Package Skew**

Description	Symbol	Device/Package	Value	Units
Package Skew(1)	$T_{PKGSKEW}$	XC2VP2FF672	104	ps
		XC2VP4FF672	102	ps
		XC2VP7FF672	92	ps
		XC2VP7FF896	101	ps
		XC2VP20FF896	93	ps
		XC2VPX20FF896	93	ps
		XC2VP20FF1152	106	ps
		XC2VP30FF896	86	ps
		XC2VP30FF1152	112	ps
		XC2VP40FF1152	92	ps
		XC2VP40FF1148	100	ps
		XC2VP50FF1152	88	ps
		XC2VP50FF1148	101	ps
		XC2VP50FF1517	97	ps
		XC2VP70FF1517	95	ps
		XC2VP70FF1704	101	ps
		XC2VPX70FF1704	101	ps
		XC2VP100FF1704	86	ps
		XC2VP100FF1696	100	ps

Notes:
1. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball (7.1ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 66: **Sample Window**

Description	Symbol	Device	Speed Grade			Units
			–7	–6	–5	
Sampling Error at Receiver Pins(1)	T_{SAMP}	All	0.50	0.50	0.50	ns

Notes:
1. This parameter indicates the total sampling error of Virtex-II Pro DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation.
2. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case duty-cycle distortion, T_{DCD_CLK180}
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.

Table 67: **Example Pin-to-Pin Setup/Hold: Source-Synchronous Configuration**

Description	Symbol	Device	Speed Grade			Units
			–7	–6	–5	
Example Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin,(1) Using DCM and Global Clock Buffer. Values represent an 18-bit bus located in Banks 2, 3, 6, or 7 and grouped to one Horizontal Global Clock Line. TRACE must be used to determine the actual values for any given design. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25.						
No Delay Global Clock and IFF(2) with DCM	T_{PSDCM_0}/T_{PHDCM_0}	XC2VP2	0.23/0.39	0.21/0.42	0.21/0.42	ns
		XC2VP4	0.26/0.37	0.24/0.40	0.24/0.41	ns
		XC2VP7	0.18/ 0.36	0.18/ 0.40	0.18/ 0.41	ns
		XC2VP20	0.14/ 0.41	0.13/ 0.42	0.12/ 0.44	ns
		XC2VPX20	0.14/ 0.41	0.13/ 0.42	0.12/ 0.44	ns
		XC2VP30	0.29/ 0.25	0.31/ 0.24	0.31/ 0.24	ns
		XC2VP40	0.25/ 0.30	0.26/ 0.29	0.27/ 0.29	ns
		XC2VP50	0.18/ 0.36	0.18/ 0.38	0.17/ 0.39	ns
		XC2VP70	0.18/ 0.37	0.18/ 0.38	0.18/ 0.38	ns
		XC2VPX70	0.18/ 0.37	0.18/ 0.38	0.18/ 0.38	ns
		XC2VP100	N/A	0.18/ 0.33	0.19/ 0.37	ns

Notes:
1. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case duty-cycle distortion using CLK0 and CLK180, T_{DCD_CLK180}

   Package skew is not included in these measurements.
2. IFF = Input Flip-Flop

Source Synchronous Timing Budgets

This section describes how to use the parameters provided in the Source-Synchronous Switching Characteristics section to develop system-specific timing budgets. The following analysis provides information necessary for determining Virtex-II Pro contributions to an overall system timing analysis; no assumptions are made about the effects of Inter-Symbol Interference or PCB skew.

Virtex-II Pro Transmitter Data-Valid Window (T_X)

T_X is the minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

T_X = Data Period - [Jitter(1) + Duty Cycle Distortion(2) + TCKSKEW(3) + TPKGSKEW(4)]

Notes:
1. Jitter values and accumulation methodology to be provided in a future release of this document. The absolute period jitter values found in the DCM Timing Parameters section of the particular DCM output clock used to clock the IOB FF can be used for a best case analysis.
2. This value depends on the clocking methodology used. See Note1 for Table 64.
3. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	GND	H4			
N/A	GND	H23			
N/A	GND	K6			
N/A	GND	K21			
N/A	GND	L11			
N/A	GND	L12			
N/A	GND	L13			
N/A	GND	L14			
N/A	GND	L15			
N/A	GND	L16			
N/A	GND	M3			
N/A	GND	M11			
N/A	GND	M12			
N/A	GND	M13			
N/A	GND	M14			
N/A	GND	M15			
N/A	GND	M16			
N/A	GND	M24			
N/A	GND	N11			
N/A	GND	N12			
N/A	GND	N13			
N/A	GND	N14			
N/A	GND	N15			
N/A	GND	N16			
N/A	GND	P11			
N/A	GND	P12			
N/A	GND	P13			
N/A	GND	P14			
N/A	GND	P15			
N/A	GND	P16			
N/A	GND	R3			
N/A	GND	R11			
N/A	GND	R12			
N/A	GND	R13			
N/A	GND	R14			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
4	IO_L57P_4/VREF_4		AH13	NC		
4	IO_L67N_4		AB15			
4	IO_L67P_4		AC15			
4	IO_L68N_4		AD14			
4	IO_L68P_4		AE14			
4	IO_L69N_4		AF14			
4	IO_L69P_4/VREF_4		AG14			
4	IO_L73N_4		AD15			
4	IO_L73P_4		AE15			
4	IO_L74N_4/GCLK3S		AF15			
4	IO_L74P_4/GCLK2P		AG15			
4	IO_L75N_4/GCLK1S		AH15			
4	IO_L75P_4/GCLK0P		AJ15			
5	IO_L75N_5/GCLK7S	BREFCLKN	AJ16			
5	IO_L75P_5/GCLK6P	BREFCLKP	AH16			
5	IO_L74N_5/GCLK5S		AG16			
5	IO_L74P_5/GCLK4P		AF16			
5	IO_L73N_5		AE16			
5	IO_L73P_5		AD16			
5	IO_L69N_5/VREF_5		AG17			
5	IO_L69P_5		AF17			
5	IO_L68N_5		AE17			
5	IO_L68P_5		AD17			
5	IO_L67N_5		AC16			
5	IO_L67P_5		AB16			
5	IO_L57N_5/VREF_5		AH18	NC		
5	IO_L57P_5		AG18	NC		
5	IO_L56N_5		AF18	NC		
5	IO_L56P_5		AF19	NC		
5	IO_L54N_5		AK21	NC		
5	IO_L54P_5		AJ21	NC		
5	IO_L53_5/No_Pair		AG20	NC		
5	IO_L50_5/No_Pair		AF20	NC		
5	IO_L49N_5		AC17	NC		
5	IO_L49P_5		AB17	NC		

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
4	IO_L73P_4	AG17				
4	IO_L74N_4/GCLK3S	AH17				
4	IO_L74P_4/GCLK2P	AJ17				
4	IO_L75N_4/GCLK1S	AK17				
4	IO_L75P_4/GCLK0P	AL17				
5	IO_L75N_5/GCLK7S	AL18				
5	IO_L75P_5/GCLK6P	AK18				
5	IO_L74N_5/GCLK5S	AJ18				
5	IO_L74P_5/GCLK4P	AH18				
5	IO_L73N_5	AG18				
5	IO_L73P_5	AF18				
5	IO_L69N_5/VREF_5	AL19				
5	IO_L69P_5	AK19				
5	IO_L68N_5	AJ19				
5	IO_L68P_5	AH19				
5	IO_L67N_5	AE18				
5	IO_L67P_5	AD18				
5	IO_L57N_5/VREF_5	AL20				
5	IO_L57P_5	AL21				
5	IO_L56N_5	AJ20				
5	IO_L56P_5	AH20				
5	IO_L55N_5	AG19				
5	IO_L55P_5	AF19				
5	IO_L54N_5	AM22				
5	IO_L54P_5	AM21				
5	IO_L53_5/No_Pair	AK21				
5	IO_L50_5/No_Pair	AJ21				
5	IO_L49N_5	AE19				
5	IO_L49P_5	AD19				
5	IO_L48N_5	AL23				
5	IO_L48P_5	AL22				
5	IO_L47N_5	AH21				
5	IO_L47P_5	AG21				
5	IO_L46N_5	AF20				
5	IO_L46P_5	AE20				
5	IO_L45N_5/VREF_5	AM24				
5	IO_L45P_5	AL24				

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
5	IO_L19P_5		AV32		
5	IO_L09N_5/VREF_5		AP32		
5	IO_L09P_5		AR32		
5	IO_L08N_5		AW33		
5	IO_L08P_5		AV33		
5	IO_L07N_5/VREF_5		AT33		
5	IO_L07P_5		AU33		
5	IO_L06N_5/VRP_5		AP33		
5	IO_L06P_5/VRN_5		AR33		
5	IO_L05_5/No_Pair		AN32		
5	IO_L03N_5/D4		AW34		
5	IO_L03P_5/D5		AY34		
5	IO_L02N_5/D6		AV34		
5	IO_L02P_5/D7		AU34		
5	IO_L01N_5/RDWR_B		AR34		
5	IO_L01P_5/CS_B		AT34		
6	IO_L01P_6/VRN_6		AW37		
6	IO_L01N_6/VRP_6		AV37		
6	IO_L02P_6		AW36		
6	IO_L02N_6		AV36		
6	IO_L03P_6		AY37		
6	IO_L03N_6/VREF_6		AY38		
6	IO_L04P_6		AU36		
6	IO_L04N_6		AT37		
6	IO_L05P_6		AU35		
6	IO_L05N_6		AT35		
6	IO_L06P_6		AW41		
6	IO_L06N_6		AW42		
6	IO_L73P_6		AV41		
6	IO_L73N_6		AV42		
6	IO_L74P_6		AW40		
6	IO_L74N_6		AV40		
6	IO_L75P_6		AU39		
6	IO_L75N_6/VREF_6		AU40		
6	IO_L76P_6		AU41		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L52N_6		AE42		
6	IO_L53P_6		AE32		
6	IO_L53N_6		AE33		
6	IO_L54P_6		AD35		
6	IO_L54N_6		AD36		
6	IO_L55P_6		AD37		
6	IO_L55N_6		AD38		
6	IO_L56P_6		AD31		
6	IO_L56N_6		AD32		
6	IO_L57P_6		AD39		
6	IO_L57N_6/VREF_6		AD40		
6	IO_L58P_6		AD41		
6	IO_L58N_6		AD42		
6	IO_L59P_6		AD33		
6	IO_L59N_6		AD34		
6	IO_L60P_6		AC33		
6	IO_L60N_6		AC34		
6	IO_L85P_6		AC36		
6	IO_L85N_6		AC37		
6	IO_L86P_6		AC31		
6	IO_L86N_6		AC32		
6	IO_L87P_6		AC39		
6	IO_L87N_6/VREF_6		AC40		
6	IO_L88P_6		AB33		
6	IO_L88N_6		AB34		
6	IO_L89P_6		AB36		
6	IO_L89N_6		AB37		
6	IO_L90P_6		AB39		
6	IO_L90N_6		AB40		
7	IO_L90P_7		AA39		
7	IO_L90N_7		AA40		
7	IO_L89P_7		AB31		
7	IO_L89N_7		AA31		
7	IO_L88P_7		AA36		
7	IO_L88N_7/VREF_7		AA37		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
0	IO_L34P_0	C30	
0	IO_L35N_0	L29	
0	IO_L35P_0	M29	
0	IO_L36N_0	H28	
0	IO_L36P_0/VREF_0	G29	
0	IO_L76N_0	E29	
0	IO_L76P_0	F29	
0	IO_L77N_0	J29	
0	IO_L77P_0	K29	
0	IO_L78N_0	D28	
0	IO_L78P_0	C29	
0	IO_L79N_0	A29	
0	IO_L79P_0	B29	
0	IO_L80_0/No_Pair	L28	
0	IO_L83_0/No_Pair	M28	
0	IO_L84N_0	G27	
0	IO_L84P_0	G28	
0	IO_L85N_0	E28	
0	IO_L85P_0	F28	
0	IO_L86N_0	J28	
0	IO_L86P_0	K28	
0	IO_L87N_0	C27	
0	IO_L87P_0/VREF_0	C28	
0	IO_L37N_0	A28	
0	IO_L37P_0	B28	
0	IO_L38N_0	L27	
0	IO_L38P_0	M27	
0	IO_L39N_0	H26	
0	IO_L39P_0	H27	
0	IO_L43N_0	E27	
0	IO_L43P_0	F27	
0	IO_L44N_0	J27	
0	IO_L44P_0	K27	
0	IO_L45N_0	D26	
0	IO_L45P_0/VREF_0	D27	
0	IO_L10N_0	A27	NC
0	IO_L10P_0	B27	NC

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L67P_3	AU5	
3	IO_L66N_3	AU1	
3	IO_L66P_3	AU2	
3	IO_L65N_3	AJ9	
3	IO_L65P_3	AK8	
3	IO_L64N_3	AU8	
3	IO_L64P_3	AV8	
3	IO_L63N_3/VREF_3	AU7	
3	IO_L63P_3	AV7	
3	IO_L62N_3	AL8	
3	IO_L62P_3	AL9	
3	IO_L61N_3	AU3	
3	IO_L61P_3	AV2	
3	IO_L84N_3	AV6	
3	IO_L84P_3	AW5	
3	IO_L83N_3	AM8	
3	IO_L83P_3	AM9	
3	IO_L82N_3	AV4	
3	IO_L82P_3	AW4	
3	IO_L81N_3/VREF_3	AV3	
3	IO_L81P_3	AW3	
3	IO_L80N_3	AN9	
3	IO_L80P_3	AP8	
3	IO_L79N_3	AW1	
3	IO_L79P_3	AW2	
3	IO_L78N_3	AY7	
3	IO_L78P_3	AY8	
3	IO_L77N_3	AR8	
3	IO_L77P_3	AR9	
3	IO_L76N_3	AW7	
3	IO_L76P_3	AY6	
3	IO_L75N_3/VREF_3	AY3	
3	IO_L75P_3	AY4	
3	IO_L74N_3	AT9	
3	IO_L74P_3	AU9	
3	IO_L73N_3	AY5	
3	IO_L73P_3	BA5	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD22	
N/A	GND	AC22	
N/A	GND	AB22	
N/A	GND	AA22	
N/A	GND	Y22	
N/A	GND	W22	
N/A	GND	V22	
N/A	GND	U22	
N/A	GND	AF21	
N/A	GND	AE21	
N/A	GND	AD21	
N/A	GND	AC21	
N/A	GND	AB21	
N/A	GND	AA21	
N/A	GND	Y21	
N/A	GND	W21	
N/A	GND	V21	
N/A	GND	U21	
N/A	GND	BB20	
N/A	GND	AV20	
N/A	GND	AP20	
N/A	GND	AF20	
N/A	GND	AE20	
N/A	GND	AD20	
N/A	GND	AC20	
N/A	GND	AB20	
N/A	GND	AA20	
N/A	GND	Y20	
N/A	GND	W20	
N/A	GND	V20	
N/A	GND	U20	
N/A	GND	J20	
N/A	GND	E20	
N/A	GND	A20	
N/A	GND	AL19	
N/A	GND	AF19	
N/A	GND	AE19	

Date	Version	Revision
11/17/04	4.1	• Table 4: Added requirement to V_{BATT} to connect pin to V_{CCAUX} or GND if battery is not used.
03/01/05	4.2	• Table 3: Corrected number of Differential I/O Pairs for XC2VP30-FF1152 from 340 to 316. • Table 4: Changed Direction for User I/O pins (IO_LXXY_#) from “Input/Output” to “Input/Output/Bidirectional”.
06/20/05	4.3	*No changes in Module 4 for this revision.*
09/15/05	4.4	*No changes in Module 4 for this revision.*
10/10/05	4.5	*No changes in Module 4 for this revision.*
03/05/07	4.6	• Figure 2, page 29: Corrected NOTE 3. • Figure 7, page 161: Updated with drawing showing correct heat sink profile and detail.
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner. Updated Figure 3, page 50, with the newest FG676/FGG676 mechanical drawing.

Notice of Disclaimer

Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)