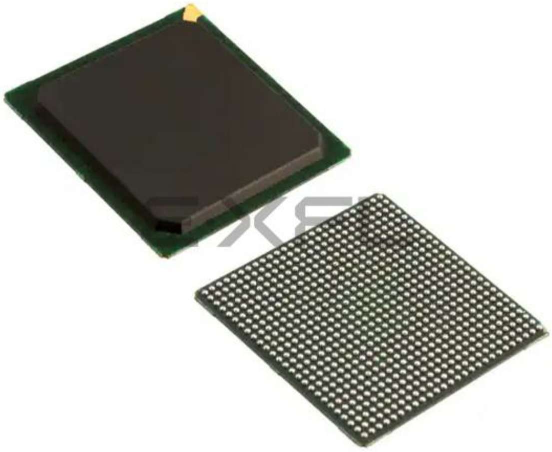

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2320
Number of Logic Elements/Cells	20880
Total RAM Bits	1622016
Number of I/O	404
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp20-7fgg676c

Serializer

The serializer multiplies the reference frequency provided on REFCLK by 20. The multiplication of the clock is achieved by using an embedded PLL.

Data is converted from parallel to serial format and transmitted on the TXP and TXN differential outputs. The electrical connection of TXP and TXN can be interchanged through configuration. This option can be controlled by an input (TXPOLARITY) at the FPGA transmitter interface.

Deserializer

The serial transceiver input is locked to the input data stream through Clock and Data Recovery (CDR), a built-in feature of the RocketIO transceiver. CDR keys off the rising and falling edges of incoming data and derives a clock that is representative of the incoming data rate.

The derived clock, RXRECCLK, is generated and locked to as long as it remains within the specified component range. This clock is presented to the FPGA fabric at $^1/_{20}$ the incoming data rate.

A sufficient number of transitions must be present in the data stream for CDR to work properly. CDR requires approximately 5,000 transitions upon power-up to guarantee locking to the incoming data rate. Once lock is achieved, up to 75 missing transitions can be tolerated before lock to the incoming data stream is lost. The CDR circuit is guaranteed to work with 8B/10B encoding.

Another feature of CDR is its ability to accept an external precision reference clock, REFCLK, which either acts to clock incoming data or to assist in synchronizing the derived RXRECCLK.

For further clarity, the TXUSRCLK is used to clock data from the FPGA fabric to the TX FIFO. The FIFO depth accounts for the slight phase difference between these two clocks. If the clocks are locked in frequency, then the FIFO acts much like a pass-through buffer.

The receiver can be configured to reverse the RXP and RXN inputs. This can be useful in the event that printed circuit board traces have been reversed.

Receiver Termination

On-chip termination is provided at the receiver, eliminating the need for external termination. The receiver includes programmable on-chip termination circuitry for 50Ω (default) or 75Ω impedance, as shown in Figure 11.

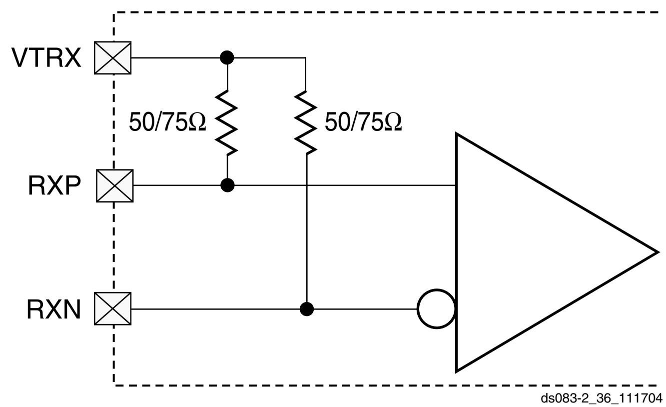

Figure 11: **RocketIO Receive Termination**

PCS

Fabric Data Interface

Internally, the PCS operates in 2-byte mode (16/20 bits). The FPGA fabric interface can either be 1, 2, or 4 bytes wide. When accompanied by the predefined modes of the PMA, the user thus has a large combination of protocols and data rates from which to choose.

USRCLK2 clocks data on the fabric side, while USRCLK clocks data on the PCS side. This creates distinct USRCLK/USRCLK2 frequency ratios for different combinations of fabric and internal data widths. Table 5 summarizes the USRCLK2 to USRCLK ratios for the three fabric data widths.

No fixed phase relationship is assumed between REFCLK, RXRECCLK, and/or any other clock that is not tied to either of these clocks. When RXUSRCLK and RXUSRCLK2 have different frequencies, each edge of the slower clock is aligned to a falling edge of the faster clock. The same relationships apply to TXUSRCLK and TXUSRCLK2.

Functional Description: FPGA

Input/Output Blocks (IOBs)

Virtex-II Pro I/O blocks (IOBs) are provided in groups of two or four on the perimeter of each device. Each IOB can be used as input and/or output for single-ended I/Os. Two IOBs can be used as a differential pair. A differential pair is always connected to the same switch matrix, as shown in Figure 18.

IOB blocks are designed for high-performance I/O, supporting 22 single-ended standards, as well as differential signaling with LVDS, LDT, bus LVDS, and LVPECL.

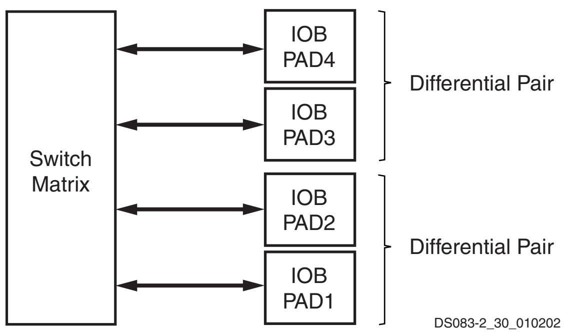

Figure 18: **Virtex-II Pro Input/Output Tile**

Note: Differential I/Os must use the same clock.

Supported I/O Standards

Virtex-II Pro IOB blocks feature SelectIO-Ultra inputs and outputs that support a wide variety of I/O signaling standards. In addition to the internal supply voltage (V_{CCINT} = 1.5V), output driver supply voltage (V_{CCO}) is dependent on the I/O standard (see Table 8 and Table 9). An auxiliary supply voltage (V_{CCAUX} = 2.5V) is required, regardless of the I/O standard used. For exact supply voltage absolute maximum ratings, see Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics.

All of the user IOBs have fixed-clamp diodes to V_{CCO} and to ground. The IOBs are not compatible or compliant with 5V I/O standards (not 5V-tolerant).

Table 10 lists supported I/O standards with Digitally Controlled Impedance. See Digitally Controlled Impedance (DCI), page 31.

Table 8: **Supported Single-Ended I/O Standards**

IOSTANDARD Attribute	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL(1)	3.3	3.3	N/R	N/R
LVCMOS33(1)	3.3	3.3	N/R	N/R
LVCMOS25	2.5	2.5	N/R	N/R
LVCMOS18	1.8	1.8	N/R	N/R
LVCMOS15	1.5	1.5	N/R	N/R
PCI33_3	Note (2)	Note (2)	N/R	N/R
PCI66_3	Note (2)	Note (2)	N/R	N/R
PCIX	Note (2)	Note (2)	N/R	N/R
GTL	Note (3)	Note (3)	0.8	1.2
GTLP	Note (3)	Note (3)	1.0	1.5
HSTL_I	1.5	N/R	0.75	0.75
HSTL_II	1.5	N/R	0.75	0.75
HSTL_III	1.5	N/R	0.9	1.5
HSTL_IV	1.5	N/R	0.9	1.5
HSTL_I_18	1.8	N/R	0.9	0.9
HSTL_II_18	1.8	N/R	0.9	0.9
HSTL_III _18	1.8	N/R	1.1	1.8
HSTL_IV_18	1.8	N/R	1.1	1.8
SSTL2_I	2.5	N/R	1.25	1.25
SSTL2_II	2.5	N/R	1.25	1.25
SSTL18_I (4)	1.8	N/R	0.9	0.9
SSTL18_II	1.8	N/R	0.9	0.9

Notes:
1. Refer to **XAPP659** for more details on interfacing to these 3.3V standards.
2. For PCI and PCI-X standards, refer to **XAPP653**.
3. V_{CCO} of GTL or GTLP should not be lower than the termination voltage or the voltage seen at the I/O pad. *Example:* If the pin High level is 1.5V, connect V_{CCO} to 1.5V.
4. SSTL18_I is not a JEDEC-supported standard.
5. N/R = no requirement.

Sum of Products

Each Virtex-II Pro slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice, as shown in Figure 43.

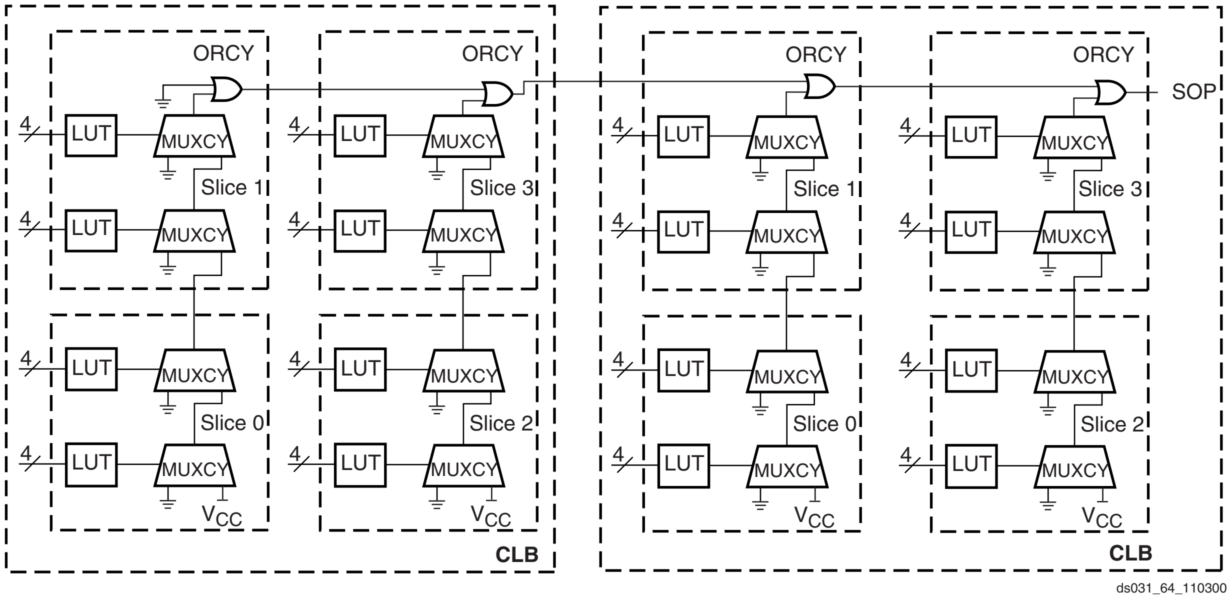

Figure 43: **Horizontal Cascade Chain**

LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 44 illustrates LUT and MUXCY resources configured as a 16-input AND gate.

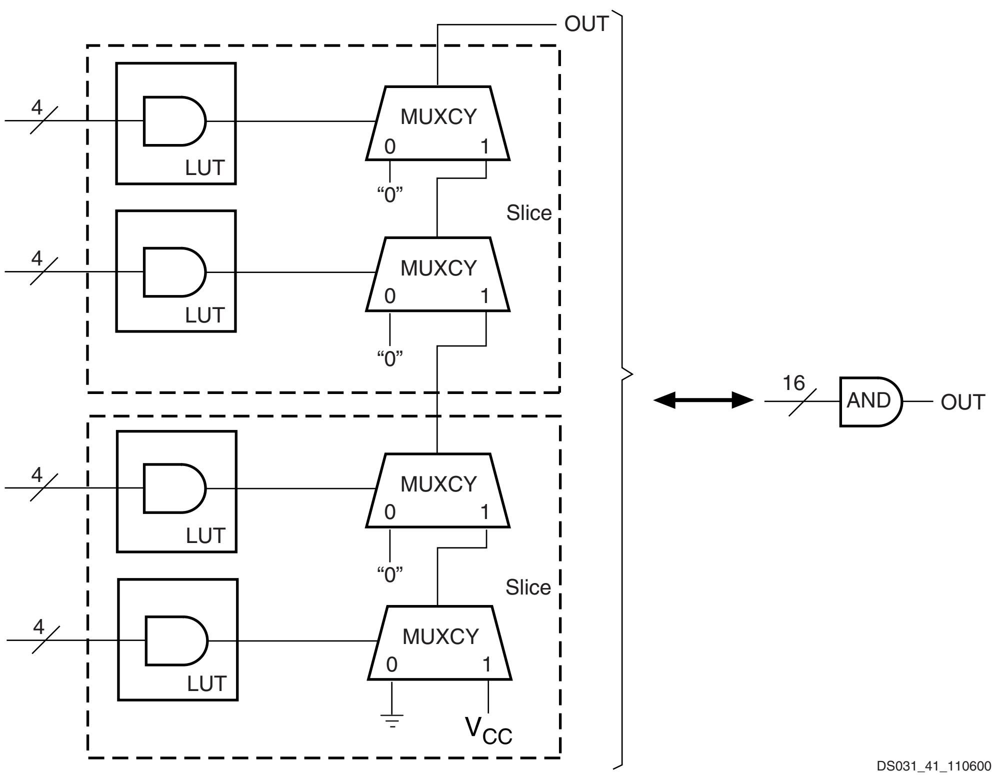

Figure 44: **Wide-Input AND Gate (16 Inputs)**

CLB/Slice Configurations

Table 19 summarizes the logic resources in one CLB. All of the CLBs are identical and each CLB or slice can be implemented in one of the configurations listed. Table 20 shows the available resources in all CLBs.

Table 19: **Logic Resources in One CLB**

Slices	LUTs	Flip-Flops	MULT_ANDs	Arithmetic & Carry-Chains	SOP Chains	Distributed SelectRAM+	Shift Registers	TBUF
4	8	8	8	2	2	128 bits	128 bits	2

Table 20: **Virtex-II Pro Logic Resources Available in All CLBs**

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry-Chains(1)	Number of SOP Chains(1)
XC2VP2	16 x 22	1,408	2,816	45,056	2,816	44	32
XC2VP4	40 x 22	3,008	6,016	96,256	6,016	44	80
XC2VP7	40 x 34	4,928	9,856	157,696	9,856	68	80
XC2VP20	56 x 46	9,280	18,560	296,960	18,560	92	112
XC2VPX20	56 x 46	9,792	19,584	313,334	18,560	92	112
XC2VP30	80 x 46	13,696	27,392	438,272	27,392	92	160
XC2VP40	88 x 58	19,392	38,784	620,544	38,784	116	176
XC2VP50	88 x 70	23,616	47,232	755,712	47,232	140	176
XC2VP70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VPX70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VP100	120 x 94	44,096	88,192	1,411,072	88,192	188	240

Notes:
1. The carry-chains and SOP chains can be split or cascaded.

18 Kb Block SelectRAM+ Resources

Introduction

Virtex-II Pro devices incorporate large amounts of 18 Kb block SelectRAM+ resources. These complement the distributed SelectRAM+ resources that provide shallow RAM structures implemented in CLBs. Each Virtex-II Pro block SelectRAM+ resource is an 18 Kb true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical. CLK, EN, WE, and SSR polarities are defined through configuration.

Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for write) and Data/parity data outputs (for read).

Operation is synchronous; the block SelectRAM+ behaves like a register. Control, address and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, a configuration option) clock edge. Data outputs change as a result of the same clock edge.

Configuration

Virtex-II Pro block SelectRAM+ supports various configurations, including single- and dual-port RAM and various data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 21.

Table 21: **Dual- and Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

Single-Port Configuration

As a single-port RAM, the block SelectRAM+ has access to the 18 Kb memory locations in any of the 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations and to 16 Kb memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of the 9-bit, 18-bit and 36-bit widths is the ability to store a parity bit for each eight bits. Parity bits must be generated or checked exter-

Virtex-II Pro Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II Pro devices. The numbers reported here are fully characterized worst-case values. Note that these values are subject to the same guidelines as Virtex-II Pro Switching Characteristics (speed files).

Table 13 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

Table 13: **Pin-to-Pin Performance**

Description	Device Used & Speed Grade	Pin-to-Pin Performance (with I/O Delays)	Units
Basic Functions:			
16-bit Address Decoder	XC2VP20FF1152-6	7.20	ns
32-bit Address Decoder	XC2VP20FF1152-6	8.08	ns
64-bit Address Decoder	XC2VP20FF1152-6	8.15	ns
4:1 MUX	XC2VP20FF1152-6	3.85	ns
8:1 MUX	XC2VP20FF1152-6	7.24	ns
16:1 MUX	XC2VP20FF1152-6	7.30	ns
32:1 MUX	XC2VP20FF1152-6	7.64	ns
Combinatorial (pad to LUT to pad)	XC2VP20FF1152-6	3.26	ns
Memory:			
Block RAM			
Pad to setup	XC2VP20FF1152-6	1.72	ns
Clock to Pad	XC2VP20FF1152-6	6.63	ns
Distributed RAM			
Pad to setup	XC2VP20FF1152-6	1.78	ns
Clock to Pad	XC2VP20FF1152-6	4.12	ns

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVCMOS25 with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments.

Table 37: **IOB Output Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}	1.58	1.68	1.85	ns, max
O input to Pad via transparent latch	T_{IOOLP}	1.65	1.82	1.99	ns, max
3-State Delays					
T input to Pad high-impedance(2)	T_{IOTHZ}	1.23	1.35	1.51	ns, max
T input to valid data on Pad	T_{IOTP}	1.51	1.63	1.78	ns, max
T input to Pad high-impedance via transparent latch(2)	$T_{IOTLPHZ}$	1.08	1.22	1.36	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	1.56	1.69	1.85	ns, max
GTS to Pad high-impedance(2)	T_{GTS}	4.11	4.73	5.20	ns, max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}	1.59	1.76	1.93	ns, max
Clock CLK to Pad high-impedance (synchronous)(2)	T_{IOCKHZ}	1.39	1.55	1.73	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	1.67	1.82	2.00	ns, max
Setup and Hold Times Before/After Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}	0.23/ 0.12	0.26/ 0.14	0.29/ 0.15	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.39/ 0.01	0.44/ 0.01	0.49/ 0.01	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.52/ 0.00	0.57/ 0.00	0.75/ 0.00	ns, min
3–State Setup Times, T input	T_{IOTCK}/T_{IOCKT}	0.23/ 0.12	0.26/ 0.14	0.29/ 0.15	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.39/ 0.01	0.44/ 0.01	0.49/ 0.01	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.52/ 0.00	0.57/ 0.00	0.75/ 0.00	ns, min
Set/Reset Delays					
Minimum Pulse Width, SR inputs (asynchronous)	T_{RPW}	0.37	0.40	0.45	ns, min
SR input to Pad (asynchronous)	T_{IOSRP}	2.33	2.56	2.83	ns, max
SR input to Pad high-impedance (asynchronous)(2)	T_{IOSRHZ}	1.97	2.16	2.41	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	2.24	2.44	2.69	ns, max
GSR to Pad	T_{IOGSRQ}	5.87	6.75	7.43	ns, max

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. The 3-state turn-off delays should not be adjusted.

Virtex-II Pro Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM

Table 55: **Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM**

Description	Symbol	Device	Speed Grade -7	Speed Grade -6	Speed Grade -5	Units
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1) For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25.						
No Delay Global Clock and IFF(2) with DCM	T_{PSDCM}/T_{PHDCM}	XC2VP2	1.54/–0.58	1.54/–0.57	1.54/–0.56	ns
		XC2VP4	1.59/–0.59	1.59/–0.58	1.59/–0.57	ns
		XC2VP7	1.66/–0.61	1.66/–0.59	1.66/–0.57	ns
		XC2VP20	1.68/–0.53	1.68/–0.53	1.68/–0.50	ns
		XC2VPX20	1.68/–0.53	1.68/–0.53	1.68/–0.50	ns
		XC2VP30	1.81/–0.74	1.81/–0.74	1.81/–0.71	ns
		XC2VP40	1.85/–0.65	1.85/–0.64	1.85/–0.60	ns
		XC2VP50	1.85/–0.57	1.85/–0.54	1.85/–0.50	ns
		XC2VP70	1.86/–0.45	1.86/–0.39	1.86/–0.30	ns
		XC2VPX70	1.86/–0.45	1.86/–0.39	1.86/–0.30	ns
		XC2VP100	N/A	1.86/–0.35	1.87/–0.28	ns

Notes:
1. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case duty-cycle distortion using CLK0 and CLK180, T_{DCD_CLK180}.
3. IFF = Input Flip-Flop or Latch

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
N/A	AVCCAUXRX7	B13
N/A	AVCCAUXRX18	R13
N/A	VTRXPAD18	R12
N/A	RXNPAD18	T13
N/A	RXPPAD18	T12
N/A	GNDA18	P11
N/A	TXPPAD18	T11
N/A	TXNPAD18	T10
N/A	VTTXPAD18	R10
N/A	AVCCAUXTX18	R11
N/A	AVCCAUXRX19	R7
N/A	VTRXPAD19	R6
N/A	RXNPAD19	T7
N/A	RXPPAD19	T6
N/A	GNDA19	P6
N/A	TXPPAD19	T5
N/A	TXNPAD19	T4
N/A	VTTXPAD19	R4
N/A	AVCCAUXTX19	R5
N/A	VCCINT	N4
N/A	VCCINT	N13
N/A	VCCINT	M5
N/A	VCCINT	M12
N/A	VCCINT	E5
N/A	VCCINT	E12
N/A	VCCINT	D4
N/A	VCCINT	D13
N/A	VCCAUX	R16
N/A	VCCAUX	R1
N/A	VCCAUX	B16
N/A	VCCAUX	B1
N/A	GND	T16
N/A	GND	T1
N/A	GND	R2

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
1	IO_L45N_1/VREF_1	C18			
1	IO_L45P_1	D18			
1	IO_L43N_1	E18			
1	IO_L43P_1	F18			
1	IO_L39N_1	G18			
1	IO_L39P_1	H18			
1	IO_L37N_1	A19			
1	IO_L37P_1	B19			
1	IO_L09N_1/VREF_1	E19			
1	IO_L09P_1	F19			
1	IO_L07N_1	G19			
1	IO_L07P_1	H19			
1	IO_L06N_1	C20			
1	IO_L06P_1	D20			
1	IO_L05_1/No_Pair	E20			
1	IO_L03N_1/VREF_1	F20			
1	IO_L03P_1	G20			
1	IO_L02N_1	D21			
1	IO_L02P_1	E21			
1	IO_L01N_1/VRP_1	D22			
1	IO_L01P_1/VRN_1	E22			
2	IO_L01N_2/VRP_2	C25			
2	IO_L01P_2/VRN_2	C26			
2	IO_L02N_2	D25			
2	IO_L02P_2	D26			
2	IO_L03N_2	E23			
2	IO_L03P_2	F22			
2	IO_L04N_2/VREF_2	E25			
2	IO_L04P_2	E26			
2	IO_L06N_2	F21			
2	IO_L06P_2	G21			
2	IO_L24N_2	F23	NC		
2	IO_L24P_2	F24	NC		
2	IO_L31N_2	F25			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	VCCINT	U10			
N/A	VCCINT	U11			
N/A	VCCINT	U16			
N/A	VCCINT	U17			
N/A	VCCINT	U20			
N/A	VCCINT	V9			
N/A	VCCINT	V18			
N/A	VCCINT	Y10			
N/A	VCCINT	Y13			
N/A	VCCINT	Y14			
N/A	VCCINT	Y17			
N/A	VCCAUX	A2			
N/A	VCCAUX	A13			
N/A	VCCAUX	A14			
N/A	VCCAUX	A25			
N/A	VCCAUX	N1			
N/A	VCCAUX	N26			
N/A	VCCAUX	P1			
N/A	VCCAUX	P26			
N/A	VCCAUX	AF2			
N/A	VCCAUX	AF13			
N/A	VCCAUX	AF14			
N/A	VCCAUX	AF25			
N/A	GND	A1			
N/A	GND	A26			
N/A	GND	B2			
N/A	GND	B25			
N/A	GND	C3			
N/A	GND	C24			
N/A	GND	D4			
N/A	GND	D8			
N/A	GND	D19			
N/A	GND	D23			
N/A	GND	F10			
N/A	GND	F17			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
2	VCCO_2	K2			
2	VCCO_2	K8			
2	VCCO_2	L9			
2	VCCO_2	M9			
2	VCCO_2	N9			
3	VCCO_3	P9			
3	VCCO_3	R9			
3	VCCO_3	T9			
3	VCCO_3	U2			
3	VCCO_3	U8			
3	VCCO_3	V8			
3	VCCO_3	Y2			
4	VCCO_4	W9			
4	VCCO_4	AD7			
4	VCCO_4	V11			
4	VCCO_4	V12			
4	VCCO_4	V13			
4	VCCO_4	W10			
4	VCCO_4	AD10			
5	VCCO_5	V14			
5	VCCO_5	V15			
5	VCCO_5	V16			
5	VCCO_5	W17			
5	VCCO_5	W18			
5	VCCO_5	AD17			
5	VCCO_5	AD20			
6	VCCO_6	P18			
6	VCCO_6	R18			
6	VCCO_6	T18			
6	VCCO_6	U19			
6	VCCO_6	U25			
6	VCCO_6	V19			
6	VCCO_6	Y25			
7	VCCO_7	G25			
7	VCCO_7	J19			
7	VCCO_7	K19			
7	VCCO_7	K25			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L38N_2	N10				
2	IO_L38P_2	N9				
2	IO_L39N_2	M7				
2	IO_L39P_2	M6				
2	IO_L40N_2/VREF_2	L2				
2	IO_L40P_2	M2				
2	IO_L41N_2	N8				
2	IO_L41P_2	N7				
2	IO_L42N_2	L4				
2	IO_L42P_2	L3				
2	IO_L43N_2	M4				
2	IO_L43P_2	M3				
2	IO_L44N_2	P10				
2	IO_L44P_2	P9				
2	IO_L45N_2	N6				
2	IO_L45P_2	N5				
2	IO_L46N_2/VREF_2	M1				
2	IO_L46P_2	N1				
2	IO_L47N_2	P8				
2	IO_L47P_2	P7				
2	IO_L48N_2	N4				
2	IO_L48P_2	N3				
2	IO_L49N_2	N2				
2	IO_L49P_2	P2				
2	IO_L50N_2	R10				
2	IO_L50P_2	R9				
2	IO_L51N_2	P6				
2	IO_L51P_2	P5				
2	IO_L52N_2/VREF_2	P4				
2	IO_L52P_2	P3				
2	IO_L53N_2	T11				
2	IO_L53P_2	U11				
2	IO_L54N_2	R7				
2	IO_L54P_2	R6				
2	IO_L55N_2	P1				
2	IO_L55P_2	R1				
2	IO_L56N_2	T10				
2	IO_L56P_2	T9				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
3	IO_L58P_3	W6				
3	IO_L57N_3/VREF_3	Y3				
3	IO_L57P_3	Y4				
3	IO_L56N_3	W7				
3	IO_L56P_3	W8				
3	IO_L55N_3	Y6				
3	IO_L55P_3	Y7				
3	IO_L54N_3	AA2				
3	IO_L54P_3	AB2				
3	IO_L53N_3	W9				
3	IO_L53P_3	W10				
3	IO_L52N_3	AA3				
3	IO_L52P_3	AA4				
3	IO_L51N_3/VREF_3	AB1				
3	IO_L51P_3	AC1				
3	IO_L50N_3	Y9				
3	IO_L50P_3	Y10				
3	IO_L49N_3	AA5				
3	IO_L49P_3	AA6				
3	IO_L48N_3	AB3				
3	IO_L48P_3	AB4				
3	IO_L47N_3	AA7				
3	IO_L47P_3	AA8				
3	IO_L46N_3	AB5				
3	IO_L46P_3	AB6				
3	IO_L45N_3/VREF_3	AC2				
3	IO_L45P_3	AD2				
3	IO_L44N_3	AA9				
3	IO_L44P_3	AA10				
3	IO_L43N_3	AC3				
3	IO_L43P_3	AC4				
3	IO_L42N_3	AD1				
3	IO_L42P_3	AE1				
3	IO_L41N_3	AB7				
3	IO_L41P_3	AB8				
3	IO_L40N_3	AC6				
3	IO_L40P_3	AC7				
3	IO_L39N_3/VREF_3	AD3				

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
0	IO_L59P_0	N21		
0	IO_L60N_0	E23		
0	IO_L60P_0	F22		
0	IO_L64N_0	D22		
0	IO_L64P_0	E22		
0	IO_L65N_0	H21		
0	IO_L65P_0	H20		
0	IO_L66N_0	G22		
0	IO_L66P_0/VREF_0	G21		
0	IO_L67N_0	D21		
0	IO_L67P_0	E21		
0	IO_L68N_0	J21		
0	IO_L68P_0	K21		
0	IO_L69N_0	C22		
0	IO_L69P_0/VREF_0	C21		
0	IO_L73N_0	F21		
0	IO_L73P_0	F20		
0	IO_L74N_0/GCLK7P	L21		
0	IO_L74P_0/GCLK6S	M21		
0	IO_L75N_0/GCLK5P	D20		
0	IO_L75P_0/GCLK4S	E20		
1	IO_L75N_1/GCLK3P	K20		
1	IO_L75P_1/GCLK2S	J20		
1	IO_L74N_1/GCLK1P	N20		
1	IO_L74P_1/GCLK0S	M20		
1	IO_L73N_1	E19		
1	IO_L73P_1	D19		
1	IO_L69N_1/VREF_1	G19		
1	IO_L69P_1	F19		
1	IO_L68N_1	L19		
1	IO_L68P_1	K19		
1	IO_L67N_1	J19		
1	IO_L67P_1	H19		
1	IO_L66N_1/VREF_1	C19		
1	IO_L66P_1	C18		
1	IO_L65N_1	N19		
1	IO_L65P_1	M19		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
4	IO_L03N_4/D2	AN10		
4	IO_L03P_4/D3	AM10		
4	IO_L05_4/No_Pair	AK10		
4	IO_L06N_4/VRP_4	AR10		
4	IO_L06P_4/VRN_4	AP10		
4	IO_L07N_4	AU10		
4	IO_L07P_4/VREF_4	AT10		
4	IO_L08N_4	AJ12		
4	IO_L08P_4	AJ13		
4	IO_L09N_4	AL10		
4	IO_L09P_4/VREF_4	AL11		
4	IO_L19N_4	AN11		
4	IO_L19P_4	AM11		
4	IO_L20N_4	AH13		
4	IO_L20P_4	AH14		
4	IO_L21N_4	AR11		
4	IO_L21P_4	AP11		
4	IO_L25N_4	AU11		
4	IO_L25P_4	AT11		
4	IO_L26N_4	AL14		
4	IO_L26P_4	AK14		
4	IO_L27N_4	AM12		
4	IO_L27P_4/VREF_4	AL12		
4	IO_L28N_4	AT12	NC	
4	IO_L28P_4	AR12	NC	
4	IO_L29N_4	AJ14	NC	
4	IO_L29P_4	AJ15	NC	
4	IO_L30N_4	AM13	NC	
4	IO_L30P_4	AL13	NC	
4	IO_L34N_4	AP12	NC	
4	IO_L34P_4	AN13	NC	
4	IO_L35N_4	AL15	NC	
4	IO_L35P_4	AK15	NC	
4	IO_L36N_4	AT13	NC	
4	IO_L36P_4/VREF_4	AR13	NC	
4	IO_L37N_4	AN14		
4	IO_L37P_4	AM14		
4	IO_L38N_4	AH15		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
5	IO_L29N_5	AK26	NC	
5	IO_L29P_5	AL26	NC	
5	IO_L28N_5	AL27	NC	
5	IO_L28P_5	AM27	NC	
5	IO_L27N_5/VREF_5	AR28		
5	IO_L27P_5	AT28		
5	IO_L26N_5	AH26		
5	IO_L26P_5	AH27		
5	IO_L25N_5	AL28		
5	IO_L25P_5	AM28		
5	IO_L21N_5	AT29		
5	IO_L21P_5	AU29		
5	IO_L20N_5	AJ27		
5	IO_L20P_5	AJ28		
5	IO_L19N_5	AP29		
5	IO_L19P_5	AR29		
5	IO_L09N_5/VREF_5	AM29		
5	IO_L09P_5	AN29		
5	IO_L08N_5	AK29		
5	IO_L08P_5	AL29		
5	IO_L07N_5/VREF_5	AT30		
5	IO_L07P_5	AU30		
5	IO_L06N_5/VRP_5	AP30		
5	IO_L06P_5/VRN_5	AR30		
5	IO_L05_5/No_Pair	AK28		
5	IO_L03N_5/D4	AM30		
5	IO_L03P_5/D5	AN30		
5	IO_L02N_5/D6	AL30		
5	IO_L02P_5/D7	AK30		
5	IO_L01N_5/RDWR_B	AR31		
5	IO_L01P_5/CS_B	AT31		
6	IO_L01P_6/VRN_6	AU33		
6	IO_L01N_6/VRP_6	AT33		
6	IO_L02P_6	AT32		
6	IO_L02N_6	AR32		
6	IO_L03P_6	AN31		
6	IO_L03N_6/VREF_6	AM31		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
6	IO_L04P_6	AR33		
6	IO_L04N_6	AP33		
6	IO_L05P_6	AM32		
6	IO_L05N_6	AL31		
6	IO_L06P_6	AT34		
6	IO_L06N_6	AR34		
6	IO_L73P_6	AU35	NC	
6	IO_L73N_6	AT35	NC	
6	IO_L75P_6	AT38	NC	
6	IO_L75N_6/VREF_6	AT39	NC	
6	IO_L76P_6	AR37	NC	
6	IO_L76N_6	AR38	NC	
6	IO_L78P_6	AP38	NC	
6	IO_L78N_6	AP39	NC	
6	IO_L79P_6	AP36	NC	
6	IO_L79N_6	AP37	NC	
6	IO_L81P_6	AP35	NC	
6	IO_L81N_6/VREF_6	AN35	NC	
6	IO_L82P_6	AN38	NC	
6	IO_L82N_6	AN39	NC	
6	IO_L84P_6	AN36	NC	
6	IO_L84N_6	AN37	NC	
6	IO_L07P_6	AN33		
6	IO_L07N_6	AN34		
6	IO_L08P_6	AK31		
6	IO_L08N_6	AK32		
6	IO_L09P_6	AM37		
6	IO_L09N_6/VREF_6	AM38		
6	IO_L10P_6	AM36		
6	IO_L10N_6	AL35		
6	IO_L11P_6	AJ31		
6	IO_L11N_6	AH30		
6	IO_L12P_6	AM33		
6	IO_L12N_6	AM34		
6	IO_L13P_6	AL38		
6	IO_L13N_6	AL39		
6	IO_L14P_6	AH29		
6	IO_L14N_6	AG29		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	VCCO_7	P27		
7	VCCO_7	W26		
7	VCCO_7	V26		
7	VCCO_7	U26		
7	VCCO_7	T26		
7	VCCO_7	R26		
6	VCCO_6	AR39		
6	VCCO_6	AC37		
6	VCCO_6	AR36		
6	VCCO_6	AL36		
6	VCCO_6	AG36		
6	VCCO_6	AC33		
6	VCCO_6	AP32		
6	VCCO_6	AL32		
6	VCCO_6	AG32		
6	VCCO_6	AC29		
6	VCCO_6	AG28		
6	VCCO_6	AF27		
6	VCCO_6	AE26		
6	VCCO_6	AD26		
6	VCCO_6	AC26		
6	VCCO_6	AB26		
6	VCCO_6	AA26		
6	VCCO_6	Y26		
5	VCCO_5	AP27		
5	VCCO_5	AK27		
5	VCCO_5	AG26		
5	VCCO_5	AG25		
5	VCCO_5	AF25		
5	VCCO_5	AG24		
5	VCCO_5	AF24		
5	VCCO_5	AP23		
5	VCCO_5	AK23		
5	VCCO_5	AF23		
5	VCCO_5	AF22		
5	VCCO_5	AF21		
4	VCCO_4	AF19		
4	VCCO_4	AF18		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
4	VCCO_4	AP17		
4	VCCO_4	AK17		
4	VCCO_4	AF17		
4	VCCO_4	AG16		
4	VCCO_4	AF16		
4	VCCO_4	AG15		
4	VCCO_4	AF15		
4	VCCO_4	AG14		
4	VCCO_4	AP13		
4	VCCO_4	AK13		
3	VCCO_3	AE14		
3	VCCO_3	AD14		
3	VCCO_3	AC14		
3	VCCO_3	AB14		
3	VCCO_3	AA14		
3	VCCO_3	Y14		
3	VCCO_3	AF13		
3	VCCO_3	AG12		
3	VCCO_3	AC11		
3	VCCO_3	AP8		
3	VCCO_3	AL8		
3	VCCO_3	AG8		
3	VCCO_3	AC7		
3	VCCO_3	AR4		
3	VCCO_3	AL4		
3	VCCO_3	AG4		
3	VCCO_3	AC3		
3	VCCO_3	AR1		
2	VCCO_2	W14		
2	VCCO_2	V14		
2	VCCO_2	U14		
2	VCCO_2	T14		
2	VCCO_2	R14		
2	VCCO_2	P13		
2	VCCO_2	N12		
2	VCCO_2	U11		
2	VCCO_2	N8		
2	VCCO_2	J8		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L44P_2		U10		
2	IO_L45N_2		U3		
2	IO_L45P_2		U4		
2	IO_L46N_2/VREF_2		U1		
2	IO_L46P_2		U2		
2	IO_L47N_2		T12		
2	IO_L47P_2		U12		
2	IO_L48N_2		V10		
2	IO_L48P_2		V11		
2	IO_L49N_2		V7		
2	IO_L49P_2		V8		
2	IO_L50N_2		U11		
2	IO_L50P_2		V12		
2	IO_L51N_2		V4		
2	IO_L51P_2		V5		
2	IO_L52N_2/VREF_2		V1		
2	IO_L52P_2		V2		
2	IO_L53N_2		W9		
2	IO_L53P_2		W10		
2	IO_L54N_2		W7		
2	IO_L54P_2		W8		
2	IO_L55N_2		W5		
2	IO_L55P_2		W6		
2	IO_L56N_2		W11		
2	IO_L56P_2		W12		
2	IO_L57N_2		W3		
2	IO_L57P_2		W4		
2	IO_L58N_2/VREF_2		W1		
2	IO_L58P_2		W2		
2	IO_L59N_2		Y9		
2	IO_L59P_2		Y10		
2	IO_L60N_2		Y6		
2	IO_L60P_2		Y7		
2	IO_L85N_2		Y3		
2	IO_L85P_2		Y4		
2	IO_L86N_2		Y11		