



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	3424
Number of Logic Elements/Cells	30816
Total RAM Bits	2506752
Number of I/O	644
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp30-5ff1152c



Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview

DS083 (v5.0) June 21, 2011

Product Specification

Summary of Virtex-II Pro™ / Virtex-II Pro X Features

- High-Performance Platform FPGA Solution, Including
 - Up to twenty RocketIO™ or RocketIO X embedded Multi-Gigabit Transceivers (MGTS)
 - Up to two IBM PowerPC™ RISC processor blocks
- Based on Virtex-II™ Platform FPGA Technology
 - Flexible logic resources
 - SRAM-based in-system configuration
 - Active Interconnect technology
- SelectRAM™+ memory hierarchy
- Dedicated 18-bit x 18-bit multiplier blocks
- High-performance clock management circuitry
- SelectIO™-Ultra technology
- XCITE Digitally Controlled Impedance (DCI) I/O

Virtex-II Pro / Virtex-II Pro X family members and resources are shown in [Table 1](#).

Table 1: Virtex-II Pro / Virtex-II Pro X FPGA Family Members

Device ⁽¹⁾	RocketIO Transceiver Blocks	PowerPC Processor Blocks	Logic Cells ⁽²⁾	CLB (1 = 4 slices = max 128 bits)		18 X 18 Bit Multiplier Blocks	Block SelectRAM+		DCMs	Maximum User I/O Pads
				Slices	Max Distr RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)		
XC2VP2	4	0	3,168	1,408	44	12	12	216	4	204
XC2VP4	4	1	6,768	3,008	94	28	28	504	4	348
XC2VP7	8	1	11,088	4,928	154	44	44	792	4	396
XC2VP20	8	2	20,880	9,280	290	88	88	1,584	8	564
XC2VPX20	8 ⁽⁴⁾	1	22,032	9,792	306	88	88	1,584	8	552
XC2VP30	8	2	30,816	13,696	428	136	136	2,448	8	644
XC2VP40	0 ⁽³⁾ , 8, or 12	2	43,632	19,392	606	192	192	3,456	8	804
XC2VP50	0 ⁽³⁾ or 16	2	53,136	23,616	738	232	232	4,176	8	852
XC2VP70	16 or 20	2	74,448	33,088	1,034	328	328	5,904	8	996
XC2VPX70	20 ⁽⁴⁾	2	74,448	33,088	1,034	308	308	5,544	8	992
XC2VP100	0 ⁽³⁾ or 20	2	99,216	44,096	1,378	444	444	7,992	12	1,164

Notes:

- 7 speed grade devices are not available in Industrial grade.
- Logic Cell ≈ (1) 4-input LUT + (1)FF + Carry Logic
- These devices can be ordered in a configuration without RocketIO transceivers. See [Table 3](#) for package configurations.
- Virtex-II Pro X devices equipped with RocketIO X transceiver cores.

RocketIO X Transceiver Features (XC2VPX20 and XC2VPX70 Only)

- Variable-Speed Full-Duplex Transceiver (XC2VPX20) Allowing 2.488 Gb/s to 6.25 Gb/s Baud Transfer Rates.
 - Includes specific baud rates used by various standards, as listed in [Table 4, Module 2](#).
- Fixed-Speed Full-Duplex Transceiver (XC2VPX70) Operating at 4.25 Gb/s Baud Transfer Rate.
- Eight or Twenty Transceiver Modules on an FPGA, Depending upon Device
- Monolithic Clock Synthesis and Clock Recovery
 - Eliminates the need for external components
- Automatic Lock-to-Reference Function
- Programmable Serial Output Differential Swing
 - 200 mV to 1600 mV, peak-peak
 - Allows compatibility with other serial system voltage levels
- Programmable Pre-emphasis Levels 0 to 500%
- Telecom/Datacom Support Modes
 - "x8" and "x10" clocking/data paths
 - 64B/66B clocking support



Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description

DS083 (v5.0) June 21, 2011

Product Specification

Virtex-II Pro⁽¹⁾ Array Functional Description

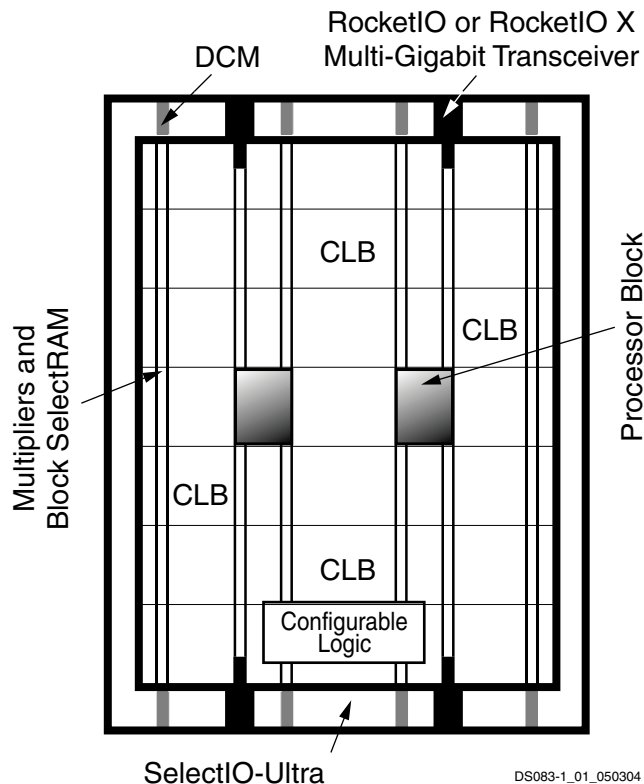


Figure 1: Virtex-II Pro Generic Architecture Overview

This module describes the following Virtex™-II Pro functional components, as shown in **Figure 1**:

- Embedded RocketIO™ (up to 3.125 Gb/s) or RocketIO X (up to 6.25 Gb/s) Multi-Gigabit Transceivers (MGTs)
- Processor blocks with embedded IBM PowerPC™ 405 RISC CPU core (PPC405) and integration circuitry.
- FPGA fabric based on Virtex-II architecture.

Virtex-II Pro User Guides

Virtex-II Pro User Guides cover theory of operation in more detail, and include implementation details, primitives and attributes, command/instruction sets, and many HDL code examples where appropriate. All parameter specifications are given only in **Module 3** of this Data Sheet.

These User Guides are available:

- For detailed descriptions of PPC405 embedded core programming models and internal core operations, see [PowerPC Processor Reference Guide](#) and [PowerPC 405 Processor Block Reference Guide](#).
- For detailed RocketIO transceiver digital/analog design considerations, see [RocketIO Transceiver User Guide](#).
- For detailed RocketIO X transceiver digital/analog design considerations, see [RocketIO X Transceiver User Guide](#).
- For detailed descriptions of the FPGA fabric (CLB, IOB, DCM, etc.), see [Virtex-II Pro Platform FPGA User Guide](#).

All of the documents above, as well as a complete listing and description of Xilinx-developed Intellectual Property cores for Virtex-II Pro, are available on the Xilinx website.

Contents of This Module

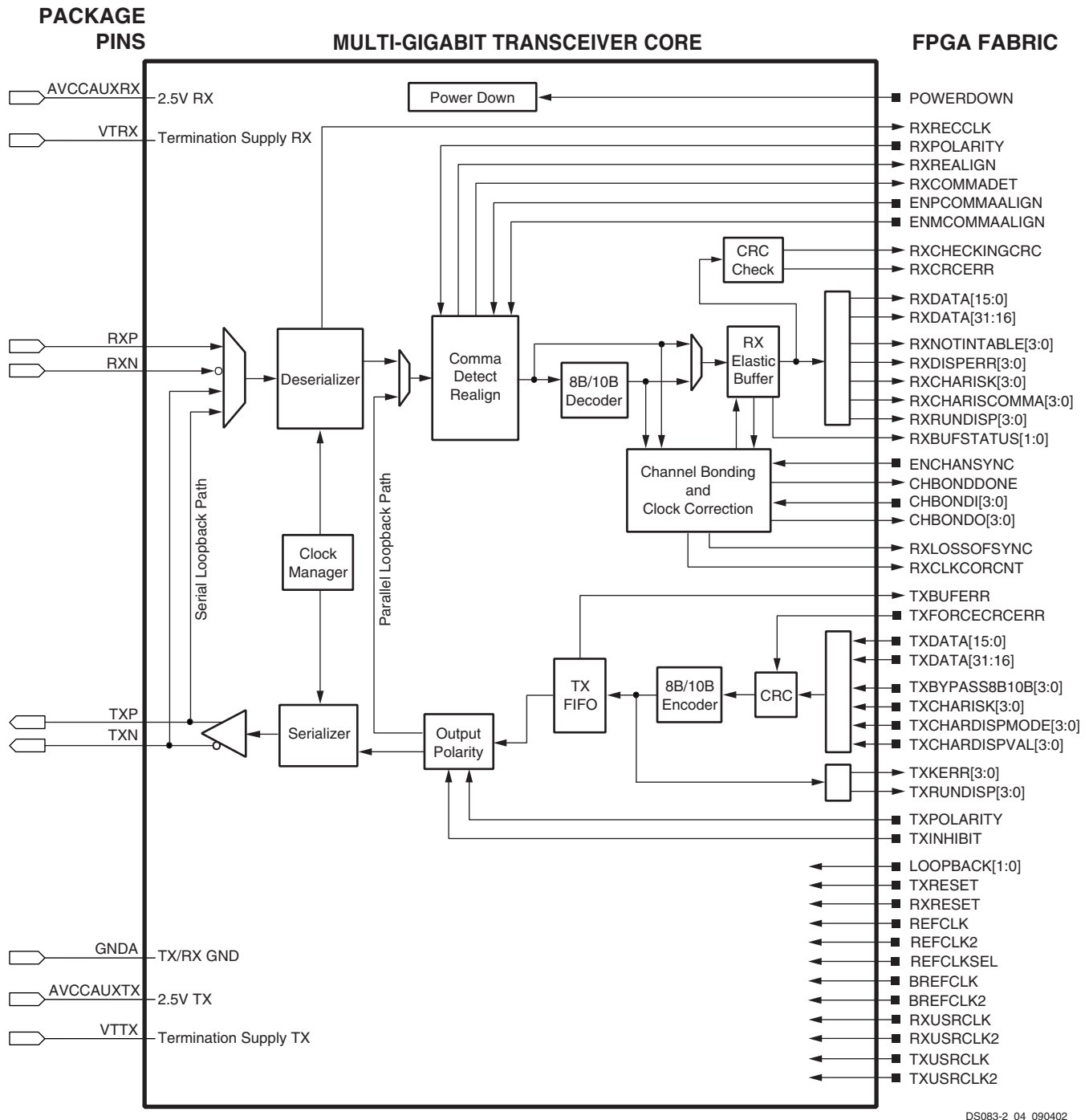
- [Functional Description: RocketIO X Multi-Gigabit Transceiver \(MGT\)](#)
- [Functional Description: RocketIO Multi-Gigabit Transceiver \(MGT\)](#)
- [Functional Description: Processor Block](#)
- [Functional Description: Embedded PowerPC 405 Core](#)
- [Functional Description: FPGA](#)
- [Revision History](#)

Virtex-II Pro Compared to Virtex-II Devices

Virtex-II Pro devices are built on the Virtex-II FPGA architecture. Most FPGA features are identical to Virtex-II devices. Major differences are described below:

- The Virtex-II Pro FPGA family is the first to incorporate embedded PPC405 and RocketIO/RocketIO X cores.
- V_{CCAUX} , the auxiliary supply voltage, is 2.5V instead of 3.3V as for Virtex-II devices. Advanced processing at 0.13 μ m has resulted in a smaller die, faster speed, and lower power consumption.
- Virtex-II Pro devices are neither bitstream-compatible nor pin-compatible with Virtex-II devices. However, Virtex-II designs can be compiled into Virtex-II Pro devices.
- On-chip input LVDS differential termination is available.
- SSTL3, AGP-2X/AGP, LVPECL_33, LVDS_33, and LVDSEXT_33 standards are not supported.
- The open-drain output pin TDO does not have an internal pull-up resistor.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.



DS083-2_04_090402

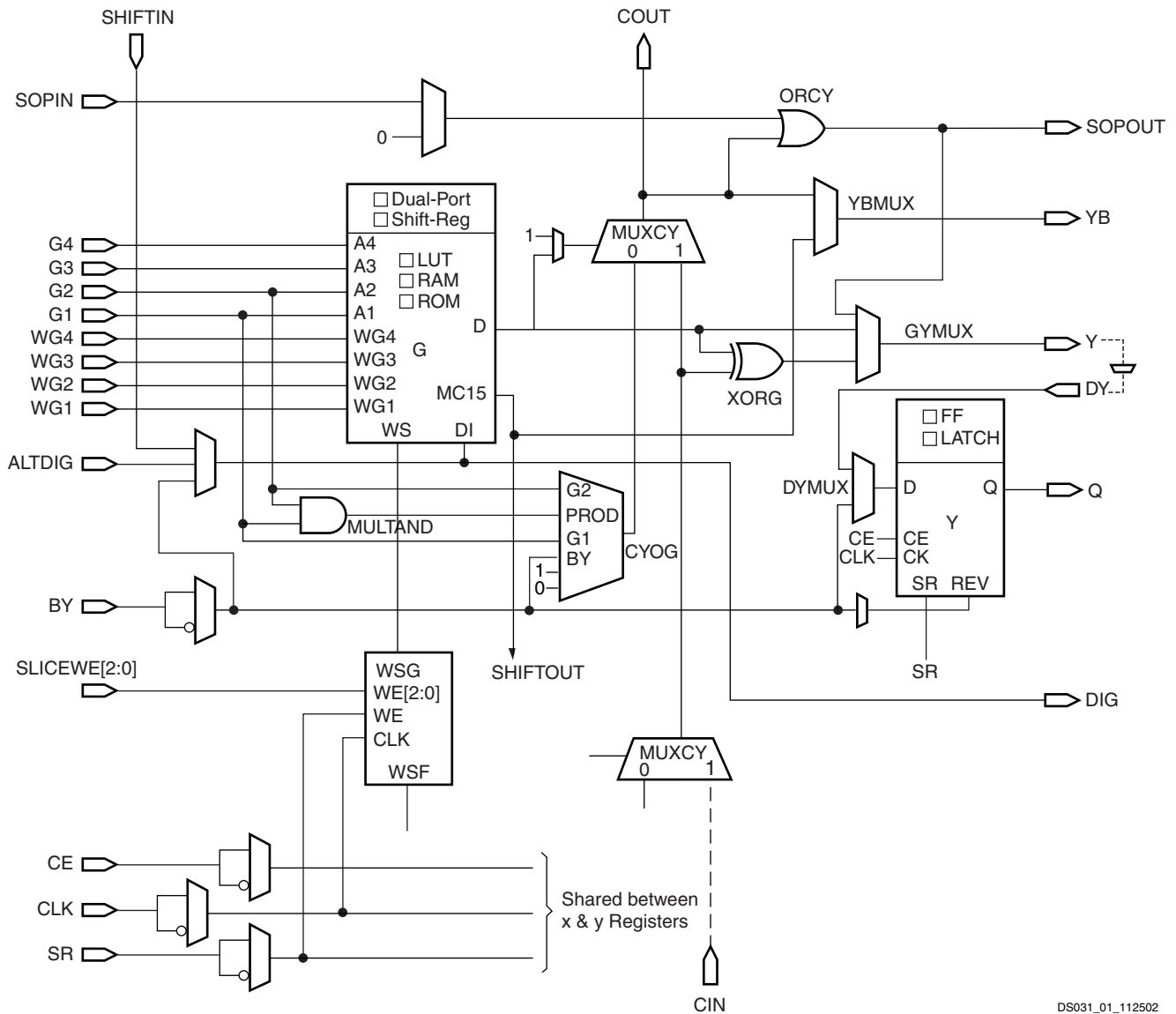
Figure 10: RocketIO Transceiver Block Diagram

Output Swing and Pre-emphasis

The output swing and pre-emphasis levels of the RocketIO MGTs are fully programmable. Each is controlled via attributes at configuration, but can be modified via partial reconfiguration.

The programmable output swing control can adjust the differential output level between 400 mV and 800 mV in four increments of 100 mV.

With pre-emphasis, the differential voltage swing is boosted to create a stronger rising waveform. This method compensates for high-frequency loss in the transmission media that would otherwise limit the magnitude of this waveform. Lossy transmission lines cause the dissipation of electrical energy. This pre-emphasis technique extends the distance that signals can be driven down lossy line media and increases the signal-to-noise ratio at the receiver.



DS031_01_112502

Figure 34: Virtex-II Pro Slice (Top Half)

Multiplier Switching Characteristics

Table 45: Multiplier Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Propagation Delay to Output Pin					
Input to Pin35	T _{MULT_P35}	4.08	4.64	5.19	ns, max
Input to Pin34	T _{MULT_P34}	3.99	4.55	5.09	ns, max
Input to Pin33	T _{MULT_P33}	3.90	4.45	4.99	ns, max
Input to Pin32	T _{MULT_P32}	3.80	4.36	4.88	ns, max
Input to Pin31	T _{MULT_P31}	3.71	4.27	4.78	ns, max
Input to Pin30	T _{MULT_P30}	3.62	4.17	4.67	ns, max
Input to Pin29	T _{MULT_P29}	3.53	4.08	4.57	ns, max
Input to Pin28	T _{MULT_P28}	3.43	3.99	4.46	ns, max
Input to Pin27	T _{MULT_P27}	3.34	3.89	4.36	ns, max
Input to Pin26	T _{MULT_P26}	3.25	3.80	4.26	ns, max
Input to Pin25	T _{MULT_P25}	3.16	3.71	4.15	ns, max
Input to Pin24	T _{MULT_P24}	3.06	3.61	4.05	ns, max
Input to Pin23	T _{MULT_P23}	2.97	3.52	3.94	ns, max
Input to Pin22	T _{MULT_P22}	2.88	3.43	3.84	ns, max
Input to Pin21	T _{MULT_P21}	2.79	3.34	3.73	ns, max
Input to Pin20	T _{MULT_P20}	2.70	3.24	3.63	ns, max
Input to Pin19	T _{MULT_P19}	2.60	3.15	3.53	ns, max
Input to Pin18	T _{MULT_P18}	2.51	3.06	3.42	ns, max
Input to Pin17	T _{MULT_P17}	2.42	2.96	3.32	ns, max
Input to Pin16	T _{MULT_P16}	2.34	2.86	3.21	ns, max
Input to Pin15	T _{MULT_P15}	2.27	2.76	3.09	ns, max
Input to Pin14	T _{MULT_P14}	2.19	2.67	2.98	ns, max
Input to Pin13	T _{MULT_P13}	2.12	2.57	2.87	ns, max
Input to Pin12	T _{MULT_P12}	2.04	2.47	2.76	ns, max
Input to Pin11	T _{MULT_P11}	1.96	2.37	2.65	ns, max
Input to Pin10	T _{MULT_P10}	1.89	2.27	2.54	ns, max
Input to Pin9	T _{MULT_P9}	1.81	2.17	2.43	ns, max
Input to Pin8	T _{MULT_P8}	1.74	2.07	2.32	ns, max
Input to Pin7	T _{MULT_P7}	1.66	1.97	2.21	ns, max
Input to Pin6	T _{MULT_P6}	1.59	1.87	2.09	ns, max
Input to Pin5	T _{MULT_P5}	1.51	1.77	1.98	ns, max
Input to Pin4	T _{MULT_P4}	1.44	1.67	1.87	ns, max
Input to Pin3	T _{MULT_P3}	1.36	1.57	1.76	ns, max
Input to Pin2	T _{MULT_P2}	1.28	1.47	1.65	ns, max
Input to Pin1	T _{MULT_P1}	1.21	1.37	1.54	ns, max
Input to Pin0	T _{MULT_P0}	1.13	1.27	1.43	ns, max

Block SelectRAM+ Switching Characteristics

Table 47: Block SelectRAM+ Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Sequential Delays					
Clock CLK to DOUT output	T_{BCKO}	1.41	1.50	1.68	ns, max
Setup and Hold Times Before Clock CLK					
ADDR inputs	T_{BACK}/T_{BCKA}	0.27/ 0.22	0.31/ 0.25	0.35/ 0.28	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}	0.20/ 0.22	0.23/ 0.25	0.26/ 0.28	ns, min
EN input	T_{BECK}/T_{BCKE}	0.28/ 0.00	0.32/ 0.00	0.35/ 0.00	ns, min
RST input	T_{BRCK}/T_{BCKR}	0.28/ 0.00	0.32/ 0.00	0.35/ 0.00	ns, min
WEN input	T_{BWCK}/T_{BCKW}	0.33/ 0.00	0.35/ 0.00	0.39/ 0.00	ns, min
Clock CLK					
CLKA to CLKB setup time for different ports	T_{BCCS}	1.0	1.0	1.0	ns, min
Minimum Pulse Width, High	T_{BPWH}	1.17	1.30	1.50	ns, min
Minimum Pulse Width, Low	T_{BPWL}	1.17	1.30	1.50	ns, min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

TBUF Switching Characteristics

Table 48: TBUF Switching Characteristics

		Speed Grade			
Description	Symbol	-7	-6	-5	Units
Combinatorial Delays					
IN input to OUT output	T_{IO}	0.88	1.01	1.12	ns, max
TRI input to OUT output high-impedance	T_{OFF}	0.48	0.55	0.61	ns, max
TRI input to valid data on OUT output	T_{ON}	0.48	0.55	0.61	ns, max

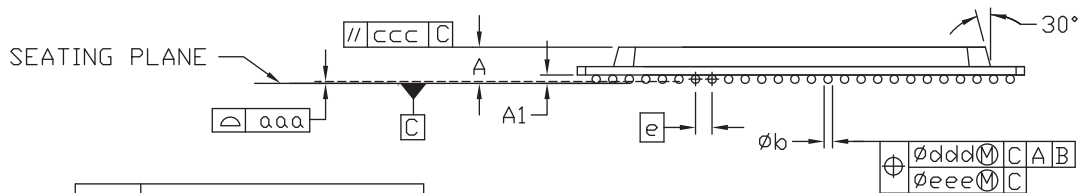
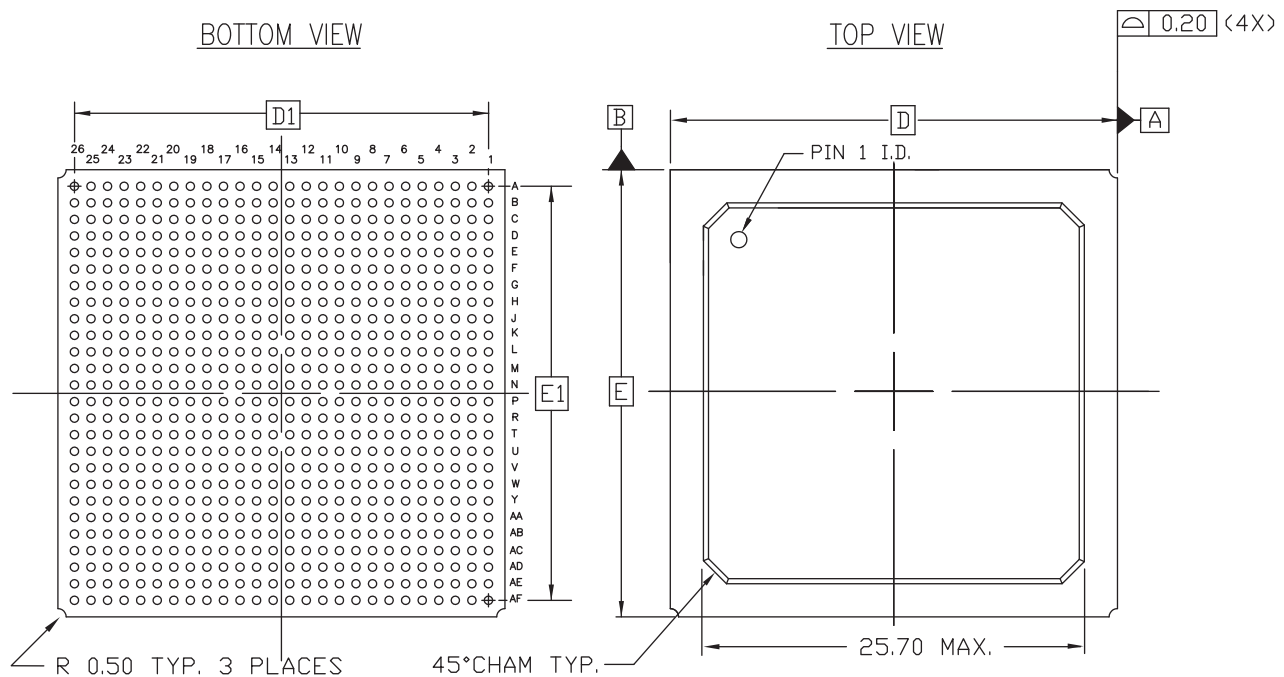
Table 7: FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
5	IO_L46N_5	W11			
5	IO_L46P_5	W10			
5	IO_L45N_5/VREF_5	AD9			
5	IO_L45P_5	AC9			
5	IO_L43N_5	AB9			
5	IO_L43P_5	AA9			
5	IO_L39N_5	Y9			
5	IO_L39P_5	W9			
5	IO_L37N_5	AF8			
5	IO_L37P_5	AE8			
5	IO_L09N_5/VREF_5	AB8			
5	IO_L09P_5	AA8			
5	IO_L07N_5/VREF_5	Y8			
5	IO_L07P_5	W8			
5	IO_L06N_5/VRP_5	AD7			
5	IO_L06P_5/VRN_5	AC7			
5	IO_L05_5/No_Pair	AB7			
5	IO_L03N_5/D4	AA7			
5	IO_L03P_5/D5	Y7			
5	IO_L02N_5/D6	AC6			
5	IO_L02P_5/D7	AB6			
5	IO_L01N_5/RDWR_B	AC5			
5	IO_L01P_5/CS_B	AB5			
6	IO_L01P_6/VRN_6	AE1			
6	IO_L01N_6/VRP_6	AD1			
6	IO_L02P_6	AD2			
6	IO_L02N_6	AC3			
6	IO_L03P_6	AC2			
6	IO_L03N_6/VREF_6	AC1			
6	IO_L05P_6	AB4			
6	IO_L05N_6	AA5			
6	IO_L06P_6	AB2			
6	IO_L06N_6	AB1			
6	IO_L23P_6	AA6	NC		

Table 7: FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	AVCCAUXRX21	AE7			
N/A	VTRXPAD21	AE6			
N/A	RXNPAD21	AF7			
N/A	RXPPAD21	AF6			
N/A	GNDA21	AD6			
N/A	TXPPAD21	AF5			
N/A	TXNPAD21	AF4			
N/A	VTTXPAD21	AE4			
N/A	AVCCAUXTX21	AE5			
N/A	M2	AD4			
N/A	M0	AF3			
N/A	M1	AE3			
N/A	TDI	D3			
N/A	VCCINT	G10			
N/A	VCCINT	G13			
N/A	VCCINT	G14			
N/A	VCCINT	G17			
N/A	VCCINT	J9			
N/A	VCCINT	J18			
N/A	VCCINT	K7			
N/A	VCCINT	K10			
N/A	VCCINT	K11			
N/A	VCCINT	K16			
N/A	VCCINT	K17			
N/A	VCCINT	K20			
N/A	VCCINT	L10			
N/A	VCCINT	L17			
N/A	VCCINT	N7			
N/A	VCCINT	N20			
N/A	VCCINT	P7			
N/A	VCCINT	P20			
N/A	VCCINT	T10			
N/A	VCCINT	T17			
N/A	VCCINT	U7			

FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)



FG676 - 63/37 (Sn/Pb) Solder Balls
FGG676 - Sn/Ag/Cu Solder Balls

SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.02	2.23	2.44
A ₁	0.40	0.50	0.60
D/E	27.00 BSC		
D ₁ /E ₁	25.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa	$\sim$	$\sim$	0.20
ccc	$\sim$	$\sim$	0.35
ddd	$\sim$	$\sim$	0.30
eee	$\sim$	$\sim$	0.10
M	26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

ds083_4_03_053111

Figure 3: FG676/FGG676 Fine-Pitch BGA Package Specifications

FF672 Flip-Chip Fine-Pitch BGA Package

As shown in [Table 8](#), XC2VP2, XC2VP4, and XC2VP7 Virtex-II Pro devices are available in the FF672 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for differences shown in the "No Connects" column. Following this table are the [FF672 Flip-Chip Fine-Pitch BGA Package Specifications \(1.00mm pitch\)](#).

Table 8: FF672 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L01N_0/VRP_0	B24			
0	IO_L01P_0/VRN_0	A24			
0	IO_L02N_0	D21			
0	IO_L02P_0	C21			
0	IO_L03N_0	E20			
0	IO_L03P_0/VREF_0	D20			
0	IO_L05_0/No_Pair	F19			
0	IO_L06N_0	E19			
0	IO_L06P_0	E18			
0	IO_L07N_0	D19			
0	IO_L07P_0	C19			
0	IO_L08N_0	B19			
0	IO_L08P_0	A19			
0	IO_L09N_0	G18			
0	IO_L09P_0/VREF_0	F18			
0	IO_L37N_0	D18	NC	NC	
0	IO_L37P_0	C18	NC	NC	
0	IO_L38N_0	G17	NC	NC	
0	IO_L38P_0	H16	NC	NC	
0	IO_L39N_0	F17	NC	NC	
0	IO_L39P_0	F16	NC	NC	
0	IO_L43N_0	E17	NC	NC	
0	IO_L43P_0	D17	NC	NC	
0	IO_L44N_0	G16	NC	NC	
0	IO_L44P_0	G15	NC	NC	
0	IO_L45N_0	E16	NC	NC	
0	IO_L45P_0/VREF_0	D16	NC	NC	
0	IO_L67N_0	F15			
0	IO_L67P_0	E15			
0	IO_L68N_0	D15			
0	IO_L68P_0	C15			
0	IO_L69N_0	H15			
0	IO_L69P_0/VREF_0	H14			

FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)

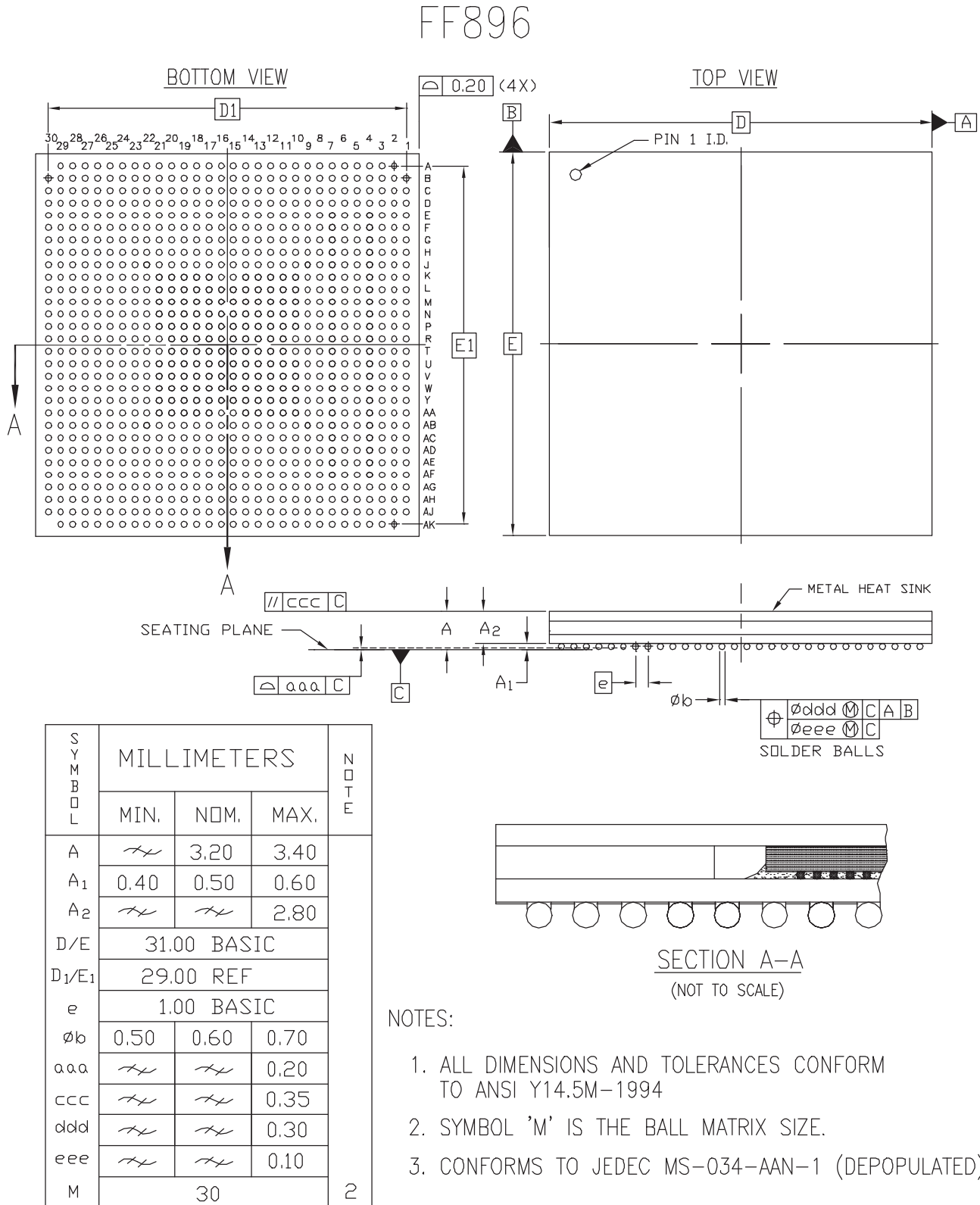


Figure 5: FF896 Flip-Chip Fine-Pitch BGA Package Specifications

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		V6		
N/A	GND		U25		
N/A	GND		U24		
N/A	GND		U23		
N/A	GND		U22		
N/A	GND		U21		
N/A	GND		U20		
N/A	GND		U19		
N/A	GND		U18		
N/A	GND		T42		
N/A	GND		T1		
N/A	GND		R39		
N/A	GND		R36		
N/A	GND		R7		
N/A	GND		R4		
N/A	GND		M42		
N/A	GND		M1		
N/A	GND		L22		
N/A	GND		L21		
N/A	GND		K39		
N/A	GND		K4		
N/A	GND		J34		
N/A	GND		J9		
N/A	GND		H42		
N/A	GND		H35		
N/A	GND		H22		
N/A	GND		H21		
N/A	GND		H8		
N/A	GND		H1		
N/A	GND		G36		
N/A	GND		G7		
N/A	GND		F37		
N/A	GND		F25		
N/A	GND		F18		
N/A	GND		F6		
N/A	GND		E38		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		E22		
N/A	GND		E21		
N/A	GND		E5		
N/A	GND		D39		
N/A	GND		D32		
N/A	GND		D28		
N/A	GND		D15		
N/A	GND		D11		
N/A	GND		D4		
N/A	GND		C42		
N/A	GND		C41		
N/A	GND		C40		
N/A	GND		C3		
N/A	GND		C2		
N/A	GND		C1		
N/A	GND		B42		
N/A	GND		B1		
N/A	GND		N14		
N/A	GND		N29		
N/A	GND		AK14		
N/A	GND		AK29		
N/A	GND		P13		
N/A	GND		P30		
N/A	GND		AJ13		
N/A	GND		AJ30		

Notes:

1. See [Table 4](#) for an explanation of the signals available on this pin.

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L75N_2	C5	
2	IO_L75P_2	B5	
2	IO_L76N_2/VREF_2	D7	
2	IO_L76P_2	C6	
2	IO_L77N_2	H8	
2	IO_L77P_2	H9	
2	IO_L78N_2	C3	
2	IO_L78P_2	C4	
2	IO_L79N_2	D1	
2	IO_L79P_2	D2	
2	IO_L80N_2	J8	
2	IO_L80P_2	K9	
2	IO_L81N_2	E6	
2	IO_L81P_2	D5	
2	IO_L82N_2/VREF_2	E4	
2	IO_L82P_2	D4	
2	IO_L83N_2	L8	
2	IO_L83P_2	L9	
2	IO_L84N_2	E3	
2	IO_L84P_2	D3	
2	IO_L61N_2	F8	
2	IO_L61P_2	E8	
2	IO_L62N_2	M8	
2	IO_L62P_2	M9	
2	IO_L63N_2	F7	
2	IO_L63P_2	E7	
2	IO_L64N_2/VREF_2	F3	
2	IO_L64P_2	E2	
2	IO_L65N_2	N12	
2	IO_L65P_2	P12	
2	IO_L66N_2	F1	
2	IO_L66P_2	F2	
2	IO_L67N_2	G7	
2	IO_L67P_2	G8	
2	IO_L68N_2	N10	
2	IO_L68P_2	N11	
2	IO_L69N_2	G6	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L67P_3	AU5	
3	IO_L66N_3	AU1	
3	IO_L66P_3	AU2	
3	IO_L65N_3	AJ9	
3	IO_L65P_3	AK8	
3	IO_L64N_3	AU8	
3	IO_L64P_3	AV8	
3	IO_L63N_3/VREF_3	AU7	
3	IO_L63P_3	AV7	
3	IO_L62N_3	AL8	
3	IO_L62P_3	AL9	
3	IO_L61N_3	AU3	
3	IO_L61P_3	AV2	
3	IO_L84N_3	AV6	
3	IO_L84P_3	AW5	
3	IO_L83N_3	AM8	
3	IO_L83P_3	AM9	
3	IO_L82N_3	AV4	
3	IO_L82P_3	AW4	
3	IO_L81N_3/VREF_3	AV3	
3	IO_L81P_3	AW3	
3	IO_L80N_3	AN9	
3	IO_L80P_3	AP8	
3	IO_L79N_3	AW1	
3	IO_L79P_3	AW2	
3	IO_L78N_3	AY7	
3	IO_L78P_3	AY8	
3	IO_L77N_3	AR8	
3	IO_L77P_3	AR9	
3	IO_L76N_3	AW7	
3	IO_L76P_3	AY6	
3	IO_L75N_3/VREF_3	AY3	
3	IO_L75P_3	AY4	
3	IO_L74N_3	AT9	
3	IO_L74P_3	AU9	
3	IO_L73N_3	AY5	
3	IO_L73P_3	BA5	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
5	IO_L10N_5	AW27	NC
5	IO_L10P_5	AW26	NC
5	IO_L45N_5/VREF_5	AN27	
5	IO_L45P_5	AP27	
5	IO_L44N_5	AU27	
5	IO_L44P_5	AV27	
5	IO_L43N_5	AR27	
5	IO_L43P_5	AR26	
5	IO_L39N_5	AL27	
5	IO_L39P_5	AM27	
5	IO_L38N_5	BA28	
5	IO_L38P_5	BB28	
5	IO_L37N_5	AY28	
5	IO_L37P_5	AY27	
5	IO_L87N_5/VREF_5	AN28	
5	IO_L87P_5	AP28	
5	IO_L86N_5	AU28	
5	IO_L86P_5	AV28	
5	IO_L85N_5	AT28	
5	IO_L85P_5	AT27	
5	IO_L84N_5	AL28	
5	IO_L84P_5	AM28	
5	IO_L83_5/No_Pair	BA29	
5	IO_L80_5/No_Pair	BB29	
5	IO_L79N_5	AY29	
5	IO_L79P_5	AW28	
5	IO_L78N_5	AN29	
5	IO_L78P_5	AP29	
5	IO_L77N_5	AU29	
5	IO_L77P_5	AV29	
5	IO_L76N_5	AT29	
5	IO_L76P_5	AR28	
5	IO_L36N_5/VREF_5	AL29	
5	IO_L36P_5	AM29	
5	IO_L35N_5	AY30	
5	IO_L35P_5	BA30	
5	IO_L34N_5	AT30	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
5	IO_L34P_5	AU30	
5	IO_L30N_5	AM30	
5	IO_L30P_5	AN30	
5	IO_L29N_5	AY31	
5	IO_L29P_5	BA31	
5	IO_L28N_5	AW31	
5	IO_L28P_5	AW30	
5	IO_L27N_5/VREF_5	AP31	
5	IO_L27P_5	AR31	
5	IO_L26N_5	AU31	
5	IO_L26P_5	AV31	
5	IO_L25N_5	AT31	
5	IO_L25P_5	AR30	
5	IO_L21N_5	AM31	
5	IO_L21P_5	AN31	
5	IO_L20N_5	BA32	
5	IO_L20P_5	BB32	
5	IO_L19N_5	AV32	
5	IO_L19P_5	AW32	
5	IO_L09N_5/VREF_5	AP32	
5	IO_L09P_5	AR32	
5	IO_L08N_5	AT32	
5	IO_L08P_5	AU32	
5	IO_L07N_5/VREF_5	BA33	
5	IO_L07P_5	BB33	
5	IO_L06N_5/VRP_5	AY33	
5	IO_L06P_5/VRN_5	AY32	
5	IO_L05_5/No_Pair	AT33	
5	IO_L03N_5/D4	AM32	
5	IO_L03P_5/D5	AN32	
5	IO_L02N_5/D6	AU33	
5	IO_L02P_5/D7	AV33	
5	IO_L01N_5/RDWR_B	AL31	
5	IO_L01P_5/CS_B	AL32	
6	IO_L01P_6/VRN_6	BB39	
6	IO_L01N_6/VRP_6	BA39	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L26P_7	V31	
7	IO_L26N_7	U31	
7	IO_L25P_7	L41	
7	IO_L25N_7	L42	
7	IO_L24P_7	K40	
7	IO_L24N_7	L40	
7	IO_L23P_7	T34	
7	IO_L23N_7	T35	
7	IO_L22P_7	L38	
7	IO_L22N_7/VREF_7	L39	
7	IO_L21P_7	K36	
7	IO_L21N_7	L36	
7	IO_L20P_7	T32	
7	IO_L20N_7	T33	
7	IO_L19P_7	K41	
7	IO_L19N_7	K42	
7	IO_L18P_7	K37	
7	IO_L18N_7	K38	
7	IO_L17P_7	R34	
7	IO_L17N_7	R35	
7	IO_L16P_7	H42	
7	IO_L16N_7/VREF_7	J41	
7	IO_L15P_7	J39	
7	IO_L15N_7	J40	
7	IO_L14P_7	R32	
7	IO_L14N_7	R33	
7	IO_L13P_7	J36	
7	IO_L13N_7	J37	
7	IO_L12P_7	H40	
7	IO_L12N_7	H41	
7	IO_L11P_7	T31	
7	IO_L11N_7	R31	
7	IO_L10P_7	H38	
7	IO_L10N_7/VREF_7	H39	
7	IO_L09P_7	H36	
7	IO_L09N_7	H37	
7	IO_L08P_7	P34	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
5	VCCO_5	AL30	
5	VCCO_5	AW29	
5	VCCO_5	AR29	
5	VCCO_5	AJ26	
5	VCCO_5	AW25	
5	VCCO_5	AR25	
5	VCCO_5	AJ25	
5	VCCO_5	AH25	
5	VCCO_5	AJ24	
5	VCCO_5	AH24	
5	VCCO_5	AJ23	
5	VCCO_5	AH23	
5	VCCO_5	AJ22	
5	VCCO_5	AH22	
4	VCCO_4	AJ21	
4	VCCO_4	AH21	
4	VCCO_4	AJ20	
4	VCCO_4	AH20	
4	VCCO_4	AJ19	
4	VCCO_4	AH19	
4	VCCO_4	AW18	
4	VCCO_4	AR18	
4	VCCO_4	AJ18	
4	VCCO_4	AH18	
4	VCCO_4	AJ17	
4	VCCO_4	AW14	
4	VCCO_4	AR14	
4	VCCO_4	AL13	
4	VCCO_4	AW10	
3	VCCO_3	AG15	
3	VCCO_3	AF15	
3	VCCO_3	AE15	
3	VCCO_3	AD15	
3	VCCO_3	AC15	
3	VCCO_3	AB15	
3	VCCO_3	AH14	
3	VCCO_3	AG14	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	VCCO_3	AF14	
3	VCCO_3	AE14	
3	VCCO_3	AD14	
3	VCCO_3	AC14	
3	VCCO_3	AB14	
3	VCCO_3	AR10	
3	VCCO_3	AL10	
3	VCCO_3	AN8	
3	VCCO_3	AJ8	
3	VCCO_3	AD8	
3	VCCO_3	AW6	
3	VCCO_3	AU4	
3	VCCO_3	AN4	
3	VCCO_3	AJ4	
3	VCCO_3	AD4	
2	VCCO_2	AA15	
2	VCCO_2	Y15	
2	VCCO_2	W15	
2	VCCO_2	V15	
2	VCCO_2	U15	
2	VCCO_2	T15	
2	VCCO_2	AA14	
2	VCCO_2	Y14	
2	VCCO_2	W14	
2	VCCO_2	V14	
2	VCCO_2	U14	
2	VCCO_2	T14	
2	VCCO_2	R14	
2	VCCO_2	M10	
2	VCCO_2	H10	
2	VCCO_2	W8	
2	VCCO_2	P8	
2	VCCO_2	K8	
2	VCCO_2	D6	
2	VCCO_2	W4	
2	VCCO_2	P4	
2	VCCO_2	K4	