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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3424
Number of Logic Elements/Cells	30816
Total RAM Bits	2506752
Number of I/O	556
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp30-5ff896c

- Programmable Receiver Equalization
- Internal AC Coupling
- On-Chip 50Ω Termination
  - Eliminates the need for external termination resistors
- Pre- and Post-Driver Serial and Parallel TX-to-RX Internal Loopback Modes for Testing Operability
- Programmable Comma Detection
  - Allows for any protocol
  - Allows for detection of any 10-bit character
- 8B/10B and 64B/66B Encoding Blocks

RocketIO Transceiver Features (All Except XC2VPX20 and XC2VPX70)

- Full-Duplex Serial Transceiver (SERDES) Capable of Baud Rates from 600 Mb/s to 3.125 Gb/s
- 100 Gb/s Duplex Data Rate (20 Channels)
- Monolithic Clock Synthesis and Clock Recovery (CDR)
- Fibre Channel, 10G Fibre Channel, Gigabit Ethernet, 10 Gb Attachment Unit Interface (XAUI), and Infiniband-Compliant Transceivers
- 8-, 16-, or 32-bit Selectable Internal FPGA Interface
- 8B/10B Encoder and Decoder (optional)
- 50Ω/75Ω on-chip Selectable Transmit and Receive Terminations
- Programmable Comma Detection
- Channel Bonding Support (from 2 to 20 Channels)
- Rate Matching via Insertion/Deletion Characters
- Four Levels of Selectable Pre-Emphasis
- Five Levels of Output Differential Voltage
- Per-Channel Internal Loopback Modes
- 2.5V Transceiver Supply Voltage

PowerPC RISC Processor Block Features (All Except XC2VP2)

- Embedded 300+ MHz Harvard Architecture Block
- Low Power Consumption: 0.9 mW/MHz
- Five-Stage Data Path Pipeline
- Hardware Multiply/Divide Unit
- Thirty-Two 32-bit General Purpose Registers
- 16 KB Two-Way Set-Associative Instruction Cache
- 16 KB Two-Way Set-Associative Data Cache
- Memory Management Unit (MMU)
  - 64-entry unified Translation Look-aside Buffers (TLB)
  - Variable page sizes (1 KB to 16 MB)
- Dedicated On-Chip Memory (OCM) Interface
- Supports IBM CoreConnect™ Bus Architecture
- Debug and Trace Support
- Timer Facilities

Virtex-II Pro Platform FPGA Technology (All Devices)

- SelectRAM+ Memory Hierarchy
  - Up to 8 Mb of True Dual-Port RAM in 18 Kb block SelectRAM+ resources
  - Up to 1,378 Kb of distributed SelectRAM+ resources
  - High-performance interfaces to external memory
- Arithmetic Functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible Logic Resources
  - Up to 88,192 internal registers/latches with Clock Enable
  - Up to 88,192 look-up tables (LUTs) or cascadable variable (1 to 16 bits) shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and Sum-of-Products support
  - Internal 3-state busing
- High-Performance Clock Management Circuitry
  - Up to twelve Digital Clock Manager (DCM) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers in all parts
- Active Interconnect Technology
  - Fourth-generation segmented routing structure
  - Fast, predictable routing delay, independent of fanout
  - Deep sub-micron noise immunity benefits
- SelectIO™-Ultra Technology
  - Up to 1,164 user I/Os
  - Twenty-two single-ended standards and ten differential standards
  - Programmable LVCMOS sink/source current (2 mA to 24 mA) per I/O
  - XCITE Digitally Controlled Impedance (DCI) I/O
  - PCI/PCI-X support (1)
  - Differential signaling
    - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
    - On-chip differential termination
    - Bus LVDS I/O

1. Refer to XAPP653 for more information.

Figure 30 provides examples illustrating the use of the LVDS_25_DCI and LVDSEXT_25_DCI I/O standards. For a complete list, see the ***Virtex-II Pro Platform FPGA User Guide***.

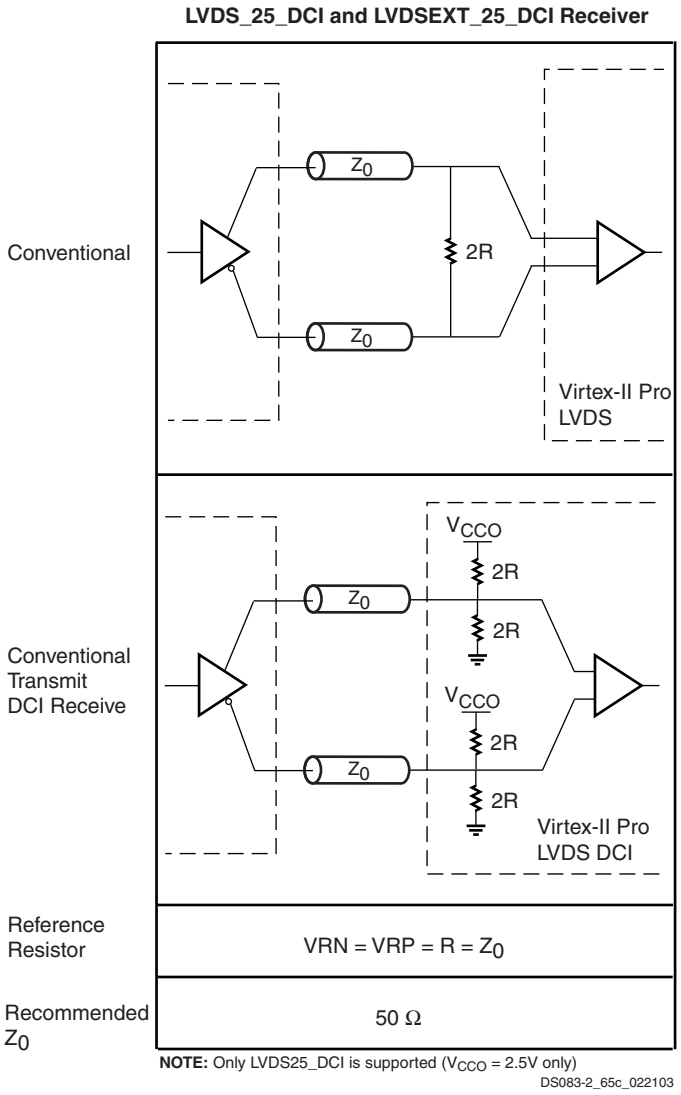

Figure 30: **LVDS DCI Usage Examples**

On-Chip Differential Termination

Virtex-II Pro provides a true 100Ω differential termination (DT) across the input differential receiver terminals. The LVDS_25_DT, LVDSEXT_25_DT, LDT_25_DT, and ULVDS_25_DT standards support on-chip differential termination.

The on-chip input differential termination in Virtex-II Pro provides major advantages over the external resistor or the DCI termination solution:

- Eliminates the stub at the receiver completely and therefore greatly improve signal integrity
- Consumes less power than DCI termination
- Supports LDT (not supported by DCI termination)
- Frees up VRP/VRN pins

Figure 31 provides examples illustrating the use of the LVDS_25_DT, LVDSEXT_25_DT, LDT_25_DT, and ULVDS_25_DT I/O standards. For further details, refer to **Solution Record 17244**. Also see the ***Virtex-II Pro Platform FPGA User Guide*** for more design information.

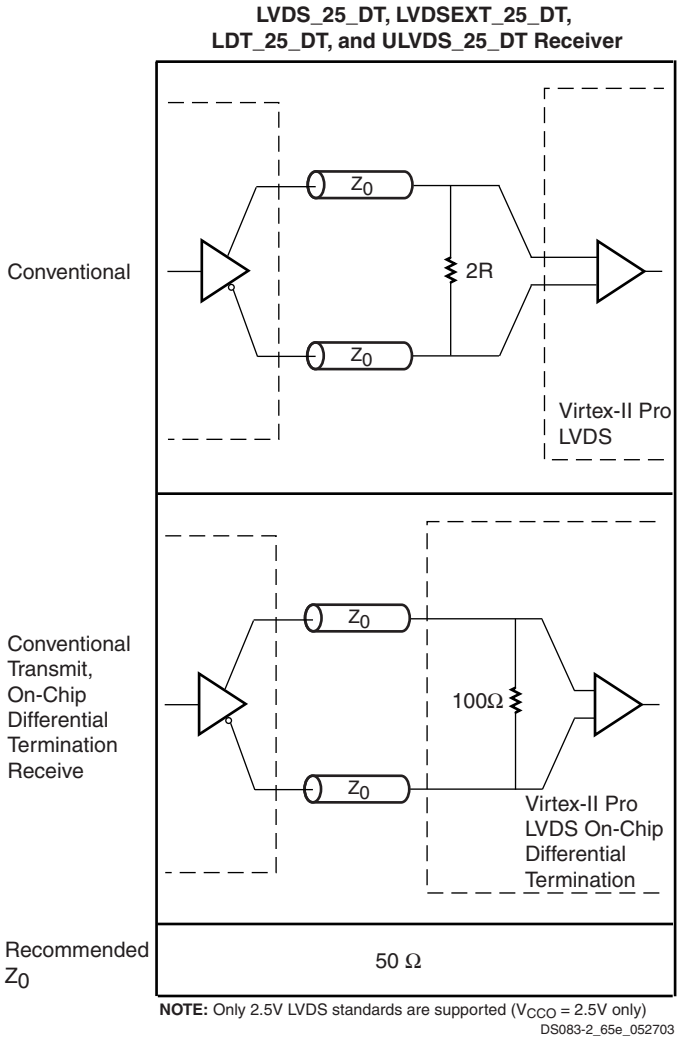

Figure 31: **LVDS Differential Termination Usage Examples**

nally in user logic. In such cases, the width is viewed as 8 + 1, 16 + 2, or 32 + 4. These extra parity bits are stored and behave exactly as the other bits, including the timing parameters. Video applications can use the 9-bit ratio of Virtex-II Pro block SelectRAM+ memory to advantage.

Each block SelectRAM+ cell is a fully synchronous memory as illustrated in Figure 47. Input data bus and output data bus widths are identical.

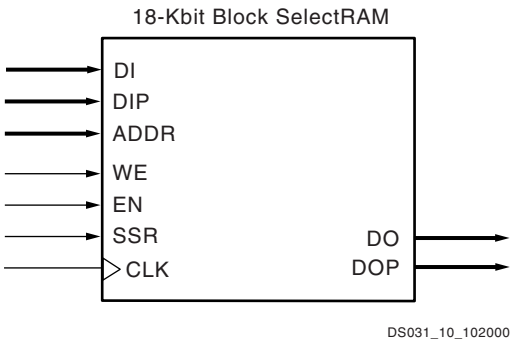

Figure 47: **18 Kb Block SelectRAM+ Memory in Single-Port Mode**

Dual-Port Configuration

As a dual-port RAM, each port of block SelectRAM+ has access to a common 18 Kb memory resource. These are fully synchronous ports with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

Table 22 illustrates the different configurations available on ports A and B.

If both ports are configured in either 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations, the 18 Kb block is accessible from port A or B. If both ports are configured in either 16K x 1-bit, 8K x 2-bit. or 4K x 4-bit configurations, the 16 K-bit block is accessible from Port A or Port B. All other configurations result in one port having access to an 18 Kb memory block and the other port having access to a 16 K-bit subset of the memory block equal to 16 Kbs.

Table 22: **Dual-Port Mode Configurations**

Port A	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1
Port B	16K x 1	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36
Port A	8K x 2	8K x 2	8K x 2	8K x 2	8K x 2	
Port B	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36	
Port A	4K x 4	4K x 4	4K x 4	4K x 4		
Port B	4K x 4	2K x 9	1K x 18	512 x 36		
Port A	2K x 9	2K x 9	2K x 9			
Port B	2K x 9	1K x 18	512 x 36			
Port A	1K x 18	1K x 18				
Port B	1K x 18	512 x 36				
Port A	512 x 36					
Port B	512 x 36					

Date	Version	Revision
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s.
03/05/07	4.6	*No changes in Module 2 for this revision.*
11/05/07	4.7	• Updated copyright notice and legal disclaimer. • Debug Interface, page 19, and Boundary-Scan (JTAG, IEEE 1532) Mode, page 57: Updated IEEE 1149.1 compliance statement.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner.

Notice of Disclaimer

Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)

SelectIO-Ultra DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: **DC Input and Output Levels**

IOSTANDARD Attribute	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, max	V, min	mA	mA
LVTTL	–0.2	0.8	2.0	3.45	0.4	2.4	24	–24
LVCMOS33	–0.2	0.8	2.0	3.45	0.4	V_{CCO} – 0.4	24	–24
LVCMOS25	–0.2	0.7	1.7	V_{CCO} + 0.4	0.4	V_{CCO} – 0.4	24	–24
LVCMOS18	–0.2	30% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.4	0.4	V_{CCO} – 0.45	16	–16
LVCMOS15	–0.2	30% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.4	0.4	V_{CCO} – 0.45	16	–16
PCI33_3	–0.2	30% V_{CCO}	50% V_{CCO}	3.6	10% V_{CCO}	90% V_{CCO}		
PCI66_3	–0.2	30% V_{CCO}	50% V_{CCO}	3.6	10% V_{CCO}	90% V_{CCO}		
PCIX	–0.2	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)
GTLP	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.6	n/a	36	n/a
GTL	–0.2	V_{REF} – 0.05	V_{REF} + 0.05	V_{CCO} + 0.4	0.4	n/a	40	n/a
HSTL_I	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	8(2)	–8(2)
HSTL_II	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	16(2)	–16(2)
HSTL_III	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	24(2)	–8(2)
HSTL_IV	–0.2	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(2)	V_{CCO} – 0.4	48(2)	–8(2)
SSTL2_I	–0.2	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2_II	–0.2	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL18_I	–0.2	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	6.7	–6.7
SSTL18_II	–0.2	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	13.4	–13.4

Notes:
1. Tested according to relevant specifications.
2. This applies to 1.5V and 1.8V HSTL.

LDT DC Specifications (LDT_25)

Table 7: **LDT DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Differential Output Voltage	V_{OD}	R_T = 100 ohm across Q and $\overline{Q}$ signals	495	600	715	mV
Change in V_{OD} Magnitude	ΔV_{OD}		–15		15	mV
Output Common Mode Voltage	V_{OCM}	R_T = 100 ohm across Q and $\overline{Q}$ signals	495	600	715	mV
Change in V_{OS} Magnitude	ΔV_{OCM}		–15		15	mV
Input Differential Voltage	V_{ID}		200	600	1000	mV
Change in V_{ID} Magnitude	ΔV_{ID}		–15		15	mV
Input Common Mode Voltage	V_{ICM}		440	600	780	mV
Change in V_{ICM} Magnitude	ΔV_{ICM}		–15		15	mV

Table 17: **Processor Block Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (CPMC405CLOCK)					
Device Control Register Bus control inputs	$T_{PCCK\_}DCR/T_{PCKC\_}DCR$	0.38/–0.18	0.44/–0.20	0.48/–0.23	ns, min
Device Control Register Bus data inputs	$T_{PDCK\_}DCR/T_{PCKD\_}DCR$	0.65/–0.01	0.75/–0.01	0.82/–0.02	ns, min
Clock and Power Management control inputs	$T_{PCCK\_}CPM/T_{PCKC\_}CPM$	0.16/ 0.03	0.19/ 0.03	0.20/ 0.03	ns, min
Reset control inputs	$T_{PCCK\_}RST/T_{PCKC\_}RST$	0.16/ 0.03	0.19/ 0.03	0.20/ 0.03	ns, min
Debug control inputs	$T_{PCCK\_}DBG/T_{PCKC\_}DBG$	0.27/ 0.30	0.31/ 0.35	0.34/ 0.38	ns, min
Trace control inputs	$T_{PCCK\_}TRC/T_{PCKC\_}TRC$	1.37/–0.41	1.57/–0.48	1.73/–0.52	ns, min
External Interrupt Controller control inputs	$T_{PCCK\_}EIC/T_{PCKC\_}EIC$	0.57/–0.22	0.66/–0.25	0.72/–0.27	ns, min
Clock to Out					
Device Control Register Bus control outputs	$T_{PCKCO\_}DCR$	1.32	1.52	1.67	ns, max
Device Control Register Bus address outputs	$T_{PCKAO\_}DCR$	1.72	1.98	2.17	ns, max
Device Control Register Bus data outputs	$T_{PCKDO\_}DCR$	1.76	2.02	2.22	ns, max
Clock and Power Management control outputs	$T_{PCKCO\_}CPM$	1.26	1.45	1.59	ns, max
Reset control outputs	$T_{PCKCO\_}RST$	1.32	1.51	1.66	ns, max
Debug control outputs	$T_{PCKCO\_}DBG$	1.94	2.22	2.44	ns, max
Trace control outputs	$T_{PCKCO\_}TRC$	1.35	1.56	1.71	ns, max
Clock					
CPMC405CLOCK minimum pulse width, high	T_{CPWH}	1.25	1.42	1.66	ns, min
CPMC405CLOCK minimum pulse width, low	T_{CPWL}	1.25	1.42	1.66	ns, min

Table 18: **Processor Block PLB Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (PLBCLK)					
Processor Local Bus(ICU/DCU) control inputs	$T_{PCCK\_}PLB/T_{PCKC\_}PLB$	0.98/ 0.18	1.12/ 0.21	1.23/ 0.23	ns, min
Processor Local Bus (ICU/DCU) data inputs	$T_{PDCK\_}PLB/T_{PCKD\_}PLB$	0.62/ 0.16	0.71/ 0.18	0.78/ 0.20	ns, min
Clock to Out					
Processor Local Bus(ICU/DCU) control outputs	$T_{PCKCO\_}PLB$	1.34	1.54	1.69	ns, max
Processor Local Bus(ICU/DCU) address bus outputs	$T_{PCKAO\_}PLB$	1.16	1.34	1.47	ns, max
Processor Local Bus(ICU/DCU) data bus outputs	$T_{PCKDO\_}PLB$	1.44	1.65	1.81	ns, max

Table 35: **IOB Input Switching Characteristics *(Continued)***

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All	0.84/–0.61	0.86/–0.63	0.90/–0.67	ns, min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$	XC2VP2	2.28/–1.89	2.60/–2.15	2.95/–2.43	ns, max
		XC2VP4	2.55/–2.10	2.87/–2.36	3.21/–2.65	ns, max
		XC2VP7	2.48/–2.05	2.82/–2.32	3.15/–2.60	ns, max
		XC2VP20	2.63/–2.05	3.02/–2.35	3.40/–2.66	ns, max
		XC2VPX20	2.63/–2.05	3.02/–2.35	3.40/–2.66	ns, max
		XC2VP30	2.67/–2.07	3.09/–2.42	3.49/–2.73	ns, max
		XC2VP40	3.28/–2.56	3.61/–2.83	4.01/–3.15	ns, max
		XC2VP50	3.84/–3.02	4.08/–3.21	4.42/–3.48	ns, max
		XC2VP70	3.98/–3.13	4.23/–3.33	4.55/–3.58	ns, max
		XC2VPX70	3.98/–3.13	4.23/–3.33	4.55/–3.58	ns, max
		XC2VP100	N/A	6.48/–5.13	7.04/–5.57	ns, max
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All	0.39/ 0.01	0.44/ 0.01	0.49/ 0.01	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.52	0.57	0.75	ns, min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	1.13	1.27	1.42	ns, max
GSR to output IQ	T_{GSRQ}	All	5.87	6.75	7.43	ns, max

Notes:
1. Input timing for LVCMOS25 is measured at 1.25V. For other I/O standards, see Table 39.

Table 65: **Package Skew**

Description	Symbol	Device/Package	Value	Units
Package Skew(1)	$T_{PKGSKEW}$	XC2VP2FF672	104	ps
		XC2VP4FF672	102	ps
		XC2VP7FF672	92	ps
		XC2VP7FF896	101	ps
		XC2VP20FF896	93	ps
		XC2VPX20FF896	93	ps
		XC2VP20FF1152	106	ps
		XC2VP30FF896	86	ps
		XC2VP30FF1152	112	ps
		XC2VP40FF1152	92	ps
		XC2VP40FF1148	100	ps
		XC2VP50FF1152	88	ps
		XC2VP50FF1148	101	ps
		XC2VP50FF1517	97	ps
		XC2VP70FF1517	95	ps
		XC2VP70FF1704	101	ps
		XC2VPX70FF1704	101	ps
		XC2VP100FF1704	86	ps
		XC2VP100FF1696	100	ps

Notes:
1. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball (7.1ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 66: **Sample Window**

Description	Symbol	Device	Speed Grade			Units
			–7	–6	–5	
Sampling Error at Receiver Pins(1)	T_{SAMP}	All	0.50	0.50	0.50	ns

Notes:
1. This parameter indicates the total sampling error of Virtex-II Pro DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation.
2. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case duty-cycle distortion, T_{DCD_CLK180}
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
3	VCCO_3	AB24			
4	VCCO_4	U14			
4	VCCO_4	U15			
4	VCCO_4	V16			
4	VCCO_4	V17			
4	VCCO_4	AC16			
4	VCCO_4	AD19			
4	VCCO_4	AD22			
5	VCCO_5	U12			
5	VCCO_5	U13			
5	VCCO_5	V10			
5	VCCO_5	V11			
5	VCCO_5	AC11			
5	VCCO_5	AD5			
5	VCCO_5	AD8			
6	VCCO_6	P10			
6	VCCO_6	R10			
6	VCCO_6	T4			
6	VCCO_6	T9			
6	VCCO_6	U9			
6	VCCO_6	W3			
6	VCCO_6	AB3			
7	VCCO_7	E3			
7	VCCO_7	H3			
7	VCCO_7	K9			
7	VCCO_7	L4			
7	VCCO_7	L9			
7	VCCO_7	M10			
7	VCCO_7	N10			
N/A	PROG_B	B1			
N/A	HSWAP_EN	B3			
N/A	DXP	A3			
N/A	DXN	C4			
N/A	AVCCAUXTX4	B5			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	IO_L44P_7	G24	NC		
7	IO_L44N_7	G23	NC		
7	IO_L43P_7	G22	NC		
7	IO_L43N_7	G21	NC		
7	IO_L42P_7	F25	NC	NC	NC
7	IO_L42N_7	F24	NC	NC	NC
7	IO_L40P_7	F23	NC	NC	NC
7	IO_L40N_7/VREF_7	F22	NC	NC	NC
7	IO_L06P_7	E26			
7	IO_L06N_7	E25			
7	IO_L05P_7	E24			
7	IO_L05N_7	E23			
7	IO_L04P_7	D26			
7	IO_L04N_7/VREF_7	D25			
7	IO_L03P_7	C26			
7	IO_L03N_7	C25			
7	IO_L02P_7	B26			
7	IO_L02N_7	A25			
7	IO_L01P_7/VRN_7	D24			
7	IO_L01N_7/VRP_7	C23			
0	VCCO_0	C17			
0	VCCO_0	C20			
0	VCCO_0	H17			
0	VCCO_0	H18			
0	VCCO_0	J14			
0	VCCO_0	J15			
0	VCCO_0	J16			
1	VCCO_1	C7			
1	VCCO_1	H9			
1	VCCO_1	C10			
1	VCCO_1	H10			
1	VCCO_1	J11			
1	VCCO_1	J12			
1	VCCO_1	J13			
2	VCCO_2	G2			
2	VCCO_2	J8			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
4	IO_L57P_4/VREF_4		AH13	NC		
4	IO_L67N_4		AB15			
4	IO_L67P_4		AC15			
4	IO_L68N_4		AD14			
4	IO_L68P_4		AE14			
4	IO_L69N_4		AF14			
4	IO_L69P_4/VREF_4		AG14			
4	IO_L73N_4		AD15			
4	IO_L73P_4		AE15			
4	IO_L74N_4/GCLK3S		AF15			
4	IO_L74P_4/GCLK2P		AG15			
4	IO_L75N_4/GCLK1S		AH15			
4	IO_L75P_4/GCLK0P		AJ15			
5	IO_L75N_5/GCLK7S	BREFCLKN	AJ16			
5	IO_L75P_5/GCLK6P	BREFCLKP	AH16			
5	IO_L74N_5/GCLK5S		AG16			
5	IO_L74P_5/GCLK4P		AF16			
5	IO_L73N_5		AE16			
5	IO_L73P_5		AD16			
5	IO_L69N_5/VREF_5		AG17			
5	IO_L69P_5		AF17			
5	IO_L68N_5		AE17			
5	IO_L68P_5		AD17			
5	IO_L67N_5		AC16			
5	IO_L67P_5		AB16			
5	IO_L57N_5/VREF_5		AH18	NC		
5	IO_L57P_5		AG18	NC		
5	IO_L56N_5		AF18	NC		
5	IO_L56P_5		AF19	NC		
5	IO_L54N_5		AK21	NC		
5	IO_L54P_5		AJ21	NC		
5	IO_L53_5/No_Pair		AG20	NC		
5	IO_L50_5/No_Pair		AF20	NC		
5	IO_L49N_5		AC17	NC		
5	IO_L49P_5		AB17	NC		

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
7	IO_L36N_7		F27	NC		
7	IO_L35P_7		K24	NC		
7	IO_L35N_7		K23	NC		
7	IO_L34P_7		E30	NC		
7	IO_L34N_7/VREF_7		E29	NC		
7	IO_L33P_7		E28	NC		
7	IO_L33N_7		E27	NC		
7	IO_L32P_7		H26	NC		
7	IO_L32N_7		H25	NC		
7	IO_L31P_7		D30	NC		
7	IO_L31N_7		D29	NC		
7	IO_L06P_7		D28			
7	IO_L06N_7		C27			
7	IO_L05P_7		J24			
7	IO_L05N_7		J23			
7	IO_L04P_7		C30			
7	IO_L04N_7/VREF_7		C29			
7	IO_L03P_7		D26			
7	IO_L03N_7		C26			
7	IO_L02P_7		G26			
7	IO_L02N_7		G25			
7	IO_L01P_7/VRN_7		B28			
7	IO_L01N_7/VRP_7		A28			
0	VCCO_0		K21			
0	VCCO_0		K20			
0	VCCO_0		K19			
0	VCCO_0		K18			
0	VCCO_0		K17			
0	VCCO_0		K16			
0	VCCO_0		J21			
0	VCCO_0		J20			
0	VCCO_0		J19			
0	VCCO_0		J18			
1	VCCO_1		K15			
1	VCCO_1		K14			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L05N_2	J8				
2	IO_L05P_2	J7				
2	IO_L06N_2	F5				
2	IO_L06P_2	F4				
2	IO_L15N_2	G4	NC			
2	IO_L15P_2	G3	NC			
2	IO_L16N_2/VREF_2	G6	NC			
2	IO_L16P_2	G5	NC			
2	IO_L17N_2	F2	NC			
2	IO_L17P_2	F1	NC			
2	IO_L18N_2	L10	NC			
2	IO_L18P_2	L9	NC			
2	IO_L19N_2	H6	NC			
2	IO_L19P_2	H5	NC			
2	IO_L20N_2	G2	NC			
2	IO_L20P_2	G1	NC			
2	IO_L21N_2	J6	NC			
2	IO_L21P_2	J5	NC			
2	IO_L22N_2/VREF_2	J4	NC			
2	IO_L22P_2	J3	NC			
2	IO_L23N_2	K8	NC			
2	IO_L23P_2	K7	NC			
2	IO_L24N_2	H4	NC			
2	IO_L24P_2	H3	NC			
2	IO_L31N_2	H2				
2	IO_L31P_2	H1				
2	IO_L32N_2	M10				
2	IO_L32P_2	M9				
2	IO_L33N_2	K5				
2	IO_L33P_2	K4				
2	IO_L34N_2/VREF_2	J2				
2	IO_L34P_2	K2				
2	IO_L35N_2	L8				
2	IO_L35P_2	L7				
2	IO_L36N_2	L6				
2	IO_L36P_2	L5				
2	IO_L37N_2	K1				
2	IO_L37P_2	L1				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
3	IO_L39P_3	AD4				
3	IO_L38N_3	AB9				
3	IO_L38P_3	AB10				
3	IO_L37N_3	AD5				
3	IO_L37P_3	AD6				
3	IO_L36N_3	AE2				
3	IO_L36P_3	AF2				
3	IO_L35N_3	AD7				
3	IO_L35P_3	AD8				
3	IO_L34N_3	AE4				
3	IO_L34P_3	AE5				
3	IO_L33N_3/VREF_3	AG1				
3	IO_L33P_3	AG2				
3	IO_L32N_3	AC9				
3	IO_L32P_3	AC10				
3	IO_L31N_3	AF3				
3	IO_L31P_3	AF4				
3	IO_L24N_3	AH1	NC			
3	IO_L24P_3	AH2	NC			
3	IO_L23N_3	AE7	NC			
3	IO_L23P_3	AE8	NC			
3	IO_L22N_3	AF5	NC			
3	IO_L22P_3	AF6	NC			
3	IO_L21N_3/VREF_3	AG3	NC			
3	IO_L21P_3	AG4	NC			
3	IO_L20N_3	AD9	NC			
3	IO_L20P_3	AD10	NC			
3	IO_L19N_3	AH3	NC			
3	IO_L19P_3	AH4	NC			
3	IO_L18N_3	AJ1	NC			
3	IO_L18P_3	AJ2	NC			
3	IO_L17N_3	AF7	NC			
3	IO_L17P_3	AF8	NC			
3	IO_L16N_3	AK1	NC			
3	IO_L16P_3	AK2	NC			
3	IO_L15N_3/VREF_3	AG5	NC			
3	IO_L15P_3	AG6	NC			
3	IO_L06N_3	AL1				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
3	IO_L06P_3	AL2				
3	IO_L05N_3	AG7				
3	IO_L05P_3	AH8				
3	IO_L04N_3	AH5				
3	IO_L04P_3	AH6				
3	IO_L03N_3/VREF_3	AK3				
3	IO_L03P_3	AK4				
3	IO_L02N_3	AJ7				
3	IO_L02P_3	AJ8				
3	IO_L01N_3/VRP_3	AJ4				
3	IO_L01P_3/VRN_3	AJ5				
4	IO_L01N_4/BUSY/DOUT(1)	AL5				
4	IO_L01P_4/INIT_B	AL6				
4	IO_L02N_4/D0/DIN(1)	AG9				
4	IO_L02P_4/D1	AH9				
4	IO_L03N_4/D2	AK6				
4	IO_L03P_4/D3	AK7				
4	IO_L05_4/No_Pair	AF10				
4	IO_L06N_4/VRP_4	AL7				
4	IO_L06P_4/VRN_4	AM7				
4	IO_L07N_4	AE11				
4	IO_L07P_4/VREF_4	AF11				
4	IO_L08N_4	AG10				
4	IO_L08P_4	AH10				
4	IO_L09N_4	AK8				
4	IO_L09P_4/VREF_4	AL8				
4	IO_L19N_4	AE12	NC	NC		
4	IO_L19P_4	AF12	NC	NC		
4	IO_L20N_4	AJ9	NC	NC		
4	IO_L20P_4	AK9	NC	NC		
4	IO_L21N_4	AL9	NC	NC		
4	IO_L21P_4	AM9	NC	NC		
4	IO_L25N_4	AG11	NC	NC		
4	IO_L25P_4	AH11	NC	NC		
4	IO_L26N_4	AH12	NC	NC		
4	IO_L26P_4	AJ12	NC	NC		
4	IO_L27N_4	AK10	NC	NC		

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	P17				
N/A	GND	P18				
N/A	GND	P19				
N/A	GND	P20				
N/A	GND	P21				
N/A	GND	R8				
N/A	GND	R14				
N/A	GND	R15				
N/A	GND	R16				
N/A	GND	R17				
N/A	GND	R18				
N/A	GND	R19				
N/A	GND	R20				
N/A	GND	R21				
N/A	GND	R27				
N/A	GND	T1				
N/A	GND	T14				
N/A	GND	T15				
N/A	GND	T16				
N/A	GND	T17				
N/A	GND	T18				
N/A	GND	T19				
N/A	GND	T20				
N/A	GND	T21				
N/A	GND	T34				
N/A	GND	U14				
N/A	GND	U15				
N/A	GND	U16				
N/A	GND	U17				
N/A	GND	U18				
N/A	GND	U19				
N/A	GND	U20				
N/A	GND	U21				
N/A	GND	V14				
N/A	GND	V15				
N/A	GND	V16				
N/A	GND	V17				
N/A	GND	V18				

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
5	IO_L29N_5	AK26	NC	
5	IO_L29P_5	AL26	NC	
5	IO_L28N_5	AL27	NC	
5	IO_L28P_5	AM27	NC	
5	IO_L27N_5/VREF_5	AR28		
5	IO_L27P_5	AT28		
5	IO_L26N_5	AH26		
5	IO_L26P_5	AH27		
5	IO_L25N_5	AL28		
5	IO_L25P_5	AM28		
5	IO_L21N_5	AT29		
5	IO_L21P_5	AU29		
5	IO_L20N_5	AJ27		
5	IO_L20P_5	AJ28		
5	IO_L19N_5	AP29		
5	IO_L19P_5	AR29		
5	IO_L09N_5/VREF_5	AM29		
5	IO_L09P_5	AN29		
5	IO_L08N_5	AK29		
5	IO_L08P_5	AL29		
5	IO_L07N_5/VREF_5	AT30		
5	IO_L07P_5	AU30		
5	IO_L06N_5/VRP_5	AP30		
5	IO_L06P_5/VRN_5	AR30		
5	IO_L05_5/No_Pair	AK28		
5	IO_L03N_5/D4	AM30		
5	IO_L03P_5/D5	AN30		
5	IO_L02N_5/D6	AL30		
5	IO_L02P_5/D7	AK30		
5	IO_L01N_5/RDWR_B	AR31		
5	IO_L01P_5/CS_B	AT31		
6	IO_L01P_6/VRN_6	AU33		
6	IO_L01N_6/VRP_6	AT33		
6	IO_L02P_6	AT32		
6	IO_L02N_6	AR32		
6	IO_L03P_6	AN31		
6	IO_L03N_6/VREF_6	AM31		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	TXPPAD7		A20		
N/A	GNDA7		C21		
N/A	RXPPAD7		A19		
N/A	RXNPAD7		A18		
N/A	VTRXPAD7		B19		
N/A	AVCCAUXRX7		B18		
N/A	AVCCAUXTX8		B16		
N/A	VTTXPAD8		B17		
N/A	TXNPAD8		A17		
N/A	TXPPAD8		A16		
N/A	GNDA8		C16		
N/A	RXPPAD8		A15		
N/A	RXNPAD8		A14		
N/A	VTRXPAD8		B15		
N/A	AVCCAUXRX8		B14		
N/A	AVCCAUXTX9		B12		
N/A	VTTXPAD9		B13		
N/A	TXNPAD9		A13		
N/A	TXPPAD9		A12		
N/A	GNDA9		C12		
N/A	RXPPAD9		A11		
N/A	RXNPAD9		A10		
N/A	VTRXPAD9		B11		
N/A	AVCCAUXRX9		B10		
N/A	AVCCAUXTX10		B8		
N/A	VTTXPAD10		B9		
N/A	TXNPAD10		A9		
N/A	TXPPAD10		A8		
N/A	GNDA10		C8		
N/A	RXPPAD10		A7		
N/A	RXNPAD10		A6		
N/A	VTRXPAD10		B7		
N/A	AVCCAUXRX10		B6		
N/A	AVCCAUXTX11		B4		
N/A	VTTXPAD11		B5		
N/A	TXNPAD11		A5		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
5	VCCO_5	AL30	
5	VCCO_5	AW29	
5	VCCO_5	AR29	
5	VCCO_5	AJ26	
5	VCCO_5	AW25	
5	VCCO_5	AR25	
5	VCCO_5	AJ25	
5	VCCO_5	AH25	
5	VCCO_5	AJ24	
5	VCCO_5	AH24	
5	VCCO_5	AJ23	
5	VCCO_5	AH23	
5	VCCO_5	AJ22	
5	VCCO_5	AH22	
4	VCCO_4	AJ21	
4	VCCO_4	AH21	
4	VCCO_4	AJ20	
4	VCCO_4	AH20	
4	VCCO_4	AJ19	
4	VCCO_4	AH19	
4	VCCO_4	AW18	
4	VCCO_4	AR18	
4	VCCO_4	AJ18	
4	VCCO_4	AH18	
4	VCCO_4	AJ17	
4	VCCO_4	AW14	
4	VCCO_4	AR14	
4	VCCO_4	AL13	
4	VCCO_4	AW10	
3	VCCO_3	AG15	
3	VCCO_3	AF15	
3	VCCO_3	AE15	
3	VCCO_3	AD15	
3	VCCO_3	AC15	
3	VCCO_3	AB15	
3	VCCO_3	AH14	
3	VCCO_3	AG14	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	VCCAUX	A2	
N/A	VCCAUX	BA1	
N/A	VCCAUX	AY1	
N/A	VCCAUX	AL1	
N/A	VCCAUX	AB1	
N/A	VCCAUX	AA1	
N/A	VCCAUX	M1	
N/A	VCCAUX	C1	
N/A	VCCAUX	B1	
N/A	GND	AV42	
N/A	GND	AP42	
N/A	GND	AK42	
N/A	GND	AF42	
N/A	GND	AC42	
N/A	GND	Y42	
N/A	GND	U42	
N/A	GND	N42	
N/A	GND	J42	
N/A	GND	E42	
N/A	GND	BA41	
N/A	GND	AY41	
N/A	GND	C41	
N/A	GND	B41	
N/A	GND	BA40	
N/A	GND	B40	
N/A	GND	BB38	
N/A	GND	AV38	
N/A	GND	AP38	
N/A	GND	AK38	
N/A	GND	AF38	
N/A	GND	AC38	
N/A	GND	Y38	
N/A	GND	U38	
N/A	GND	N38	
N/A	GND	J38	
N/A	GND	E38	
N/A	GND	A38	