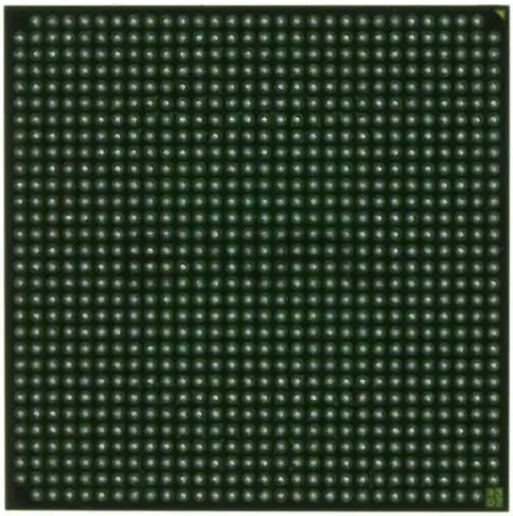


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3424
Number of Logic Elements/Cells	30816
Total RAM Bits	2506752
Number of I/O	556
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp30-5ffg896c

Digitally Controlled Impedance (DCI)

Today's chip output signals with fast edge rates require termination to prevent reflections and maintain signal integrity. High pin count packages (especially ball grid arrays) can not accommodate external termination resistors.

Virtex-II Pro XCITE DCI provides controlled impedance drivers and on-chip termination for single-ended and differential I/Os. This eliminates the need for external resistors and improves signal integrity. The DCI feature can be used on any IOB by selecting one of the DCI I/O standards.

When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination.

DCI operates independently on each I/O bank. When a DCI I/O standard is used in a particular I/O bank, external reference resistors must be connected to two dual-function pins on the bank. These resistors, voltage reference of N transistor (VRN) and the voltage reference of P transistor (VRP) are shown in Figure 26.

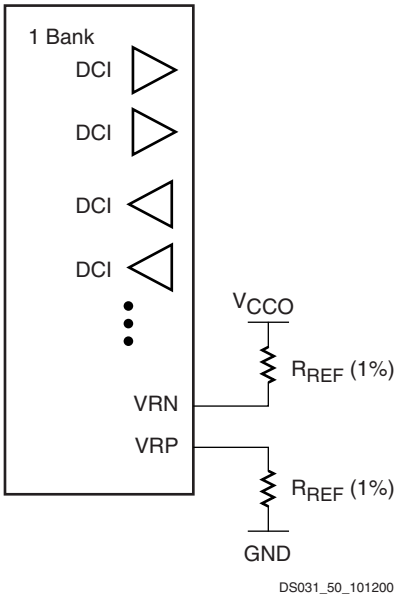


Figure 26: **DCI in a Virtex-II Pro Bank**

When used with a terminated I/O standard, the value of the resistors are specified by the standard (typically 50Ω). When used with a controlled impedance driver, the resistors set the output impedance of the driver within the specified range (20Ω to 100Ω). For all series and parallel terminations listed in Table 13 and Table 14, the reference resistors must have the same value for any given bank. One percent resistors are recommended.

The DCI system adjusts the I/O impedance to match the two external reference resistors, or half of the reference resistors, and compensates for impedance changes due to voltage and/or temperature fluctuations. The adjustment is done by turning parallel transistors in the IOB on or off.

Controlled Impedance Drivers (Series Termination)

DCI can be used to provide a buffer with a controlled output impedance. It is desirable for this output impedance to match the transmission line impedance (Z_0). Virtex-II Pro input buffers also support LVDCI and LVDCI_DV2.

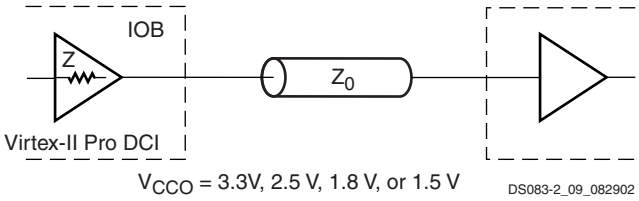


Figure 27: **Internal Series Termination**

Table 13: **SelectIO-Ultra Controlled Impedance Buffers**

V_{CCO}	DCI	DCI Half Impedance
3.3V	LVDCI_33	N/A
2.5V	LVDCI_25	LVDCI_DV2_25
1.8V	LVDCI_18	LVDCI_DV2_18
1.5V	LVDCI_15	LVDCI_DV2_15

Controlled Impedance Terminations (Parallel)

DCI also provides on-chip termination for SSTL2, SSTL18, HSTL (Class I, II, III, or IV), LVDS_25, LVDSEXT_25, and GTL/GTLP receivers or transmitters on bidirectional lines. Table 14 and Table 15 list the on-chip parallel terminations available in Virtex-II Pro devices. V_{CCO} must be set according to Table 10. There is a V_{CCO} requirement for GTL_DCI and GTLP_DCI, due to the on-chip termination resistor.

Table 14: **SelectIO-Ultra Buffers With On-Chip Parallel Termination**

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
SSTL Class I, 2.5V	SSTL2_I	SSTL2_I_DCI(1)
SSTL Class II, 2.5V	SSTL2_II	SSTL2_II_DCI(1)
SSTL Class I, 1.8V	SSTL18_I	SSTL18_I_DCI
SSTL Class II, 1.8V	SSTL18_II	SSTL18_II_DCI
HSTL Class I	HSTL_I	HSTL_I_DCI
HSTL Class I, 1.8V	HSTL_I_18	HSTL_I_DCI_18
HSTL Class II	HSTL_II	HSTL_II_DCI
HSTL Class II, 1.8V	HSTL_II_18	HSTL_II_DCI_18
HSTL Class III	HSTL_III	HSTL_III_DCI
HSTL Class III, 1.8V	HSTL_III_18	HSTL_III_DCI_18
HSTL Class IV	HSTL_IV	HSTL_IV_DCI
HSTL Class IV, 1.8V	HSTL_IV_18	HSTL_IV_DCI_18
GTL	GTL	GTL_DCI
GTL Plus	GTLP	GTLP_DCI

Notes:
1. SSTL compatible.

Table 19: **Processor Block JTAG Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (JTAGC405TCK)					
JTAG control inputs	$T_{PCCK_}$JTAG/ $T_{PCKC_}$JTAG	0.80/ 0.70	0.80/ 0.70	0.88/ 0.77	ns, min
JTAG reset input	$T_{PCCK_}$JTAGRST/ $T_{PCKC_}$JTAGRST	0.80/ 0.70	0.80/ 0.70	0.88/ 0.77	ns, min
Clock to Out					
JTAG control outputs	$T_{PCKCO_}$JTAG	1.34	1.54	1.69	ns, max

Table 20: **PowerPC 405 Data-Side On-Chip Memory Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (BRAMDSOCMCLK)					
Data-Side On-Chip Memory data bus inputs	$T_{PDCK_}$DSOCM/ $T_{PCKD_}$DSOCM	0.73/ 0.83	0.84/ 0.95	0.92/ 1.05	ns, min
Clock to Out					
Data-Side On-Chip Memory control outputs	$T_{PCKCO_}$DSOCM	1.58	1.82	1.99	ns, max
Data-Side On-Chip Memory address bus outputs	$T_{PCKAO_}$DSOCM	1.46	1.68	1.84	ns, max
Data-Side On-Chip Memory data bus outputs	$T_{PCKDO_}$DSOCM	0.90	1.03	1.13	ns, max

Table 21: **PowerPC 405 Instruction-Side On-Chip Memory Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-7**	**-6**	**-5**	**Units**
Setup and Hold Relative to Clock (BRAMISOCMCLK)					
Instruction-Side On-Chip Memory data bus inputs	$T_{PDCK_}$ISOCM/ $T_{PCKD_}$ISOCM	0.81/ 0.68	0.93/ 0.78	1.02/ 0.86	ns, min
Clock to Out					
Instruction-Side On-Chip Memory control outputs	$T_{PCKCO_}$ISOCM	1.33	1.53	1.68	ns, max
Instruction-Side On-Chip Memory address bus outputs	$T_{PCKAO_}$ISOCM	1.52	1.75	1.92	ns, max
Instruction-Side On-Chip Memory data bus outputs	$T_{PCKDO_}$ISOCM	1.35	1.55	1.70	ns, max

Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
1	IO_L02N_1	C13
1	IO_L02P_1	B14
1	IO_L01N_1/VRP_1	C14
1	IO_L01P_1/VRN_1	C15
2	IO_L01N_2/VRP_2	E14
2	IO_L01P_2/VRN_2	E15
2	IO_L02N_2	E13
2	IO_L02P_2	F12
2	IO_L03N_2	F13
2	IO_L03P_2	F14
2	IO_L04N_2/VREF_2	F15
2	IO_L04P_2	F16
2	IO_L06N_2	G13
2	IO_L06P_2	G14
2	IO_L85N_2	G15
2	IO_L85P_2	G16
2	IO_L86N_2	G12
2	IO_L86P_2	H13
2	IO_L88N_2/VREF_2	H14
2	IO_L88P_2	H15
2	IO_L90N_2	H16
2	IO_L90P_2	J16
3	IO_L90N_3	J15
3	IO_L90P_3	J14
3	IO_L89N_3	J13
3	IO_L89P_3	K12
3	IO_L87N_3/VREF_3	K16
3	IO_L87P_3	K15
3	IO_L85N_3	K14
3	IO_L85P_3	K13
3	IO_L06N_3	L16
3	IO_L06P_3	L15
3	IO_L05N_3	L14

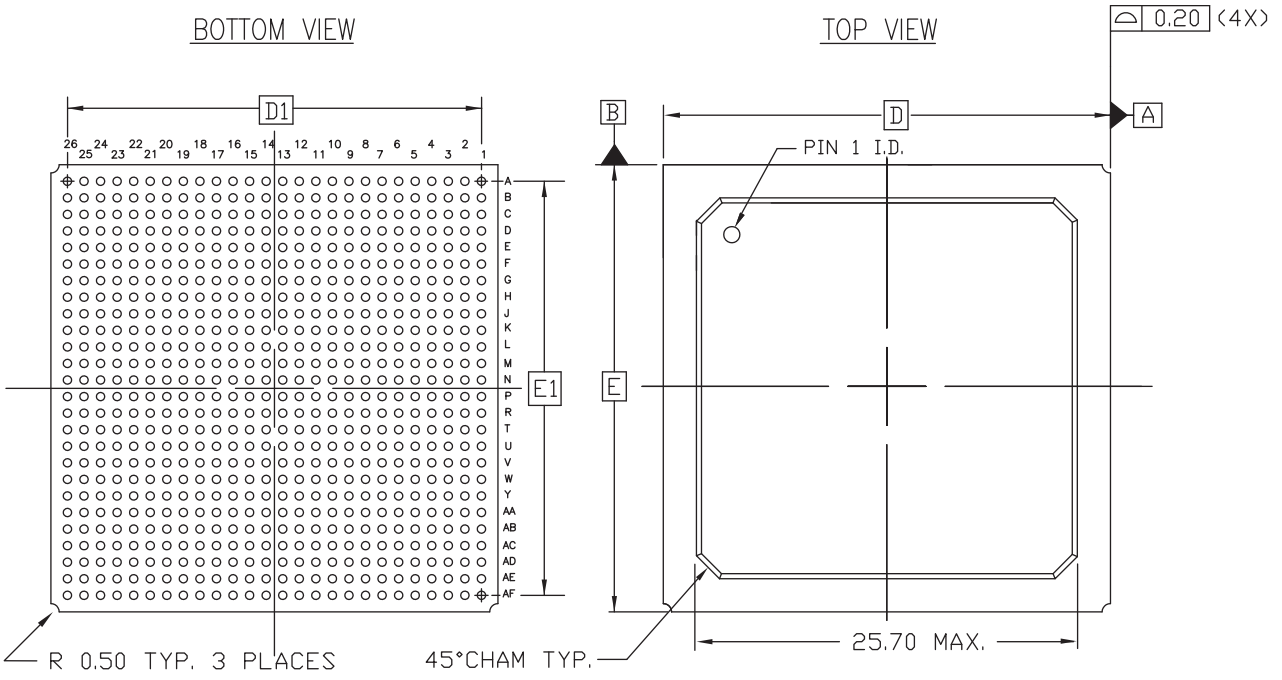
Table 5: **FG256/FGG256 — XC2VP2 and XC2VP4**

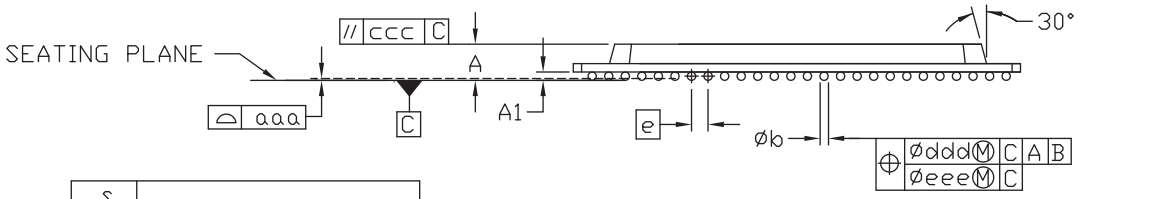
Bank	Pin Description	Pin Number
5	IO_L06N_5/VRP_5	P5
5	IO_L06P_5/VRN_5	N5
5	IO_L03N_5/D4	T3
5	IO_L03P_5/D5	T2
5	IO_L02N_5/D6	P4
5	IO_L02P_5/D7	R3
5	IO_L01N_5/RDWR_B	P3
5	IO_L01P_5/CS_B	P2
6	IO_L01P_6/VRN_6	M3
6	IO_L01N_6/VRP_6	M2
6	IO_L02P_6	N1
6	IO_L02N_6	M1
6	IO_L03P_6	M4
6	IO_L03N_6/VREF_6	L5
6	IO_L05P_6	L4
6	IO_L05N_6	L3
6	IO_L06P_6	L2
6	IO_L06N_6	L1
6	IO_L85P_6	K4
6	IO_L85N_6	K3
6	IO_L87P_6	K2
6	IO_L87N_6/VREF_6	K1
6	IO_L89P_6	K5
6	IO_L89N_6	J4
6	IO_L90P_6	J3
6	IO_L90N_6	J2
7	IO_L90P_7	J1
7	IO_L90N_7	H1
7	IO_L88P_7	H2
7	IO_L88N_7/VREF_7	H3
7	IO_L86P_7	H4
7	IO_L86N_7	G5
7	IO_L85P_7	G1

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
3	IO_L03P_3	AC25			
3	IO_L02N_3	AC24			
3	IO_L02P_3	AD25			
3	IO_L01N_3/VRP_3	AD26			
3	IO_L01P_3/VRN_3	AE26			
4	IO_L01N_4/BUSY/DOUT(1)	AB22			
4	IO_L01P_4/INIT_B	AC22			
4	IO_L02N_4/D0/DIN(1)	AB21			
4	IO_L02P_4/D1	AC21			
4	IO_L03N_4/D2	Y20			
4	IO_L03P_4/D3	AA20			
4	IO_L05_4/No_Pair	AB20			
4	IO_L06N_4/VRP_4	AC20			
4	IO_L06P_4/VRN_4	AD20			
4	IO_L07N_4	W19			
4	IO_L07P_4/VREF_4	Y19			
4	IO_L09N_4	AA19			
4	IO_L09P_4/VREF_4	AB19			
4	IO_L37N_4	AE19			
4	IO_L37P_4	AF19			
4	IO_L39N_4	W18			
4	IO_L39P_4	Y18			
4	IO_L43N_4	AA18			
4	IO_L43P_4	AB18			
4	IO_L45N_4	AC18			
4	IO_L45P_4/VREF_4	AD18			
4	IO_L46N_4	W17			
4	IO_L46P_4	W16			
4	IO_L48N_4	AB17			
4	IO_L48P_4	AB16			
4	IO_L49N_4	AC17			
4	IO_L49P_4	AD17			
4	IO_L50_4/No_Pair	Y16			
4	IO_L53_4/No_Pair	AA16			

FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)





FG676 - 63/37 (Sn/Pb) Solder Balls
FGG676 - Sn/Ag/Cu Solder Balls

SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.02	2.23	2.44
A_1	0.40	0.50	0.60
D/E	27.00 BSC		
D_1/E_1	25.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa	~	~	0.20
ccc	~	~	0.35
ddd	~	~	0.30
eee	~	~	0.10
M	26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

ds083_4_03_053111

Figure 3: **FG676/FGG676 Fine-Pitch BGA Package Specifications**

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	AVCCAUXRX19	AE15			
N/A	VTRXPAD19	AE16			
N/A	RXNPAD19	AF15			
N/A	RXPPAD19	AF16			
N/A	GNDA19	AD16			
N/A	TXPPAD19	AF17			
N/A	TXNPAD19	AF18			
N/A	VTTXPAD19	AE18			
N/A	AVCCAUXTX19	AE17			
N/A	AVCCAUXRX21	AE20	NC	NC	
N/A	VTRXPAD21	AE21	NC	NC	
N/A	RXNPAD21	AF20	NC	NC	
N/A	RXPPAD21	AF21	NC	NC	
N/A	GNDA21	AD22	NC	NC	
N/A	TXPPAD21	AF22	NC	NC	
N/A	TXNPAD21	AF23	NC	NC	
N/A	VTTXPAD21	AE23	NC	NC	
N/A	AVCCAUXTX21	AE22	NC	NC	
N/A	VCCINT	H8			
N/A	VCCINT	J9			
N/A	VCCINT	K9			
N/A	VCCINT	U9			
N/A	VCCINT	V9			
N/A	VCCINT	W8			
N/A	VCCINT	H19			
N/A	VCCINT	J10			
N/A	VCCINT	J17			
N/A	VCCINT	J18			
N/A	VCCINT	K11			
N/A	VCCINT	K16			
N/A	VCCINT	K18			
N/A	VCCINT	L10			
N/A	VCCINT	L17			
N/A	VCCINT	T10			
N/A	VCCINT	T17			
N/A	VCCINT	U11			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
1	IO_L02P_1		F7			
1	IO_L01N_1/VRP_1		E7			
1	IO_L01P_1/VRN_1		E6			
2	IO_L01N_2/VRP_2		A3			
2	IO_L01P_2/VRN_2		B3			
2	IO_L02N_2		G6			
2	IO_L02P_2		G5			
2	IO_L03N_2		C5			
2	IO_L03P_2		D5			
2	IO_L04N_2/VREF_2		C2			
2	IO_L04P_2		C1			
2	IO_L05N_2		J8			
2	IO_L05P_2		J7			
2	IO_L06N_2		C4			
2	IO_L06P_2		D3			
2	IO_L31N_2		D2	NC		
2	IO_L31P_2		D1	NC		
2	IO_L32N_2		H6	NC		
2	IO_L32P_2		H5	NC		
2	IO_L33N_2		E4	NC		
2	IO_L33P_2		E3	NC		
2	IO_L34N_2/VREF_2		E2	NC		
2	IO_L34P_2		E1	NC		
2	IO_L35N_2		K8	NC		
2	IO_L35P_2		K7	NC		
2	IO_L36N_2		F4	NC		
2	IO_L36P_2		F3	NC		
2	IO_L37N_2		F2	NC		
2	IO_L37P_2		F1	NC		
2	IO_L38N_2		J6	NC		
2	IO_L38P_2		J5	NC		
2	IO_L39N_2		G4	NC		
2	IO_L39P_2		G3	NC		
2	IO_L40N_2/VREF_2		G2	NC		
2	IO_L40P_2		G1	NC		

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
3	IO_L57P_3		Y1			
3	IO_L56N_3		U7			
3	IO_L56P_3		U8			
3	IO_L55N_3		V5			
3	IO_L55P_3		V6			
3	IO_L54N_3		Y2			
3	IO_L54P_3		AA2			
3	IO_L53N_3		V7			
3	IO_L53P_3		V8			
3	IO_L52N_3		W3			
3	IO_L52P_3		W4			
3	IO_L51N_3/VREF_3		AA1			
3	IO_L51P_3		AB1			
3	IO_L50N_3		W5			
3	IO_L50P_3		W6			
3	IO_L49N_3		Y4			
3	IO_L49P_3		Y5			
3	IO_L48N_3		AA3			
3	IO_L48P_3		AA4			
3	IO_L47N_3		W7			
3	IO_L47P_3		W8			
3	IO_L46N_3		AB3			
3	IO_L46P_3		AB4			
3	IO_L45N_3/VREF_3		AB2			
3	IO_L45P_3		AC2			
3	IO_L44N_3		AA5			
3	IO_L44P_3		AA6			
3	IO_L43N_3		AC3			
3	IO_L43P_3		AC4			
3	IO_L42N_3		AD1	NC		
3	IO_L42P_3		AD2	NC		
3	IO_L41N_3		Y7	NC		
3	IO_L41P_3		Y8	NC		
3	IO_L40N_3		AB5	NC		
3	IO_L40P_3		AB6	NC		
3	IO_L39N_3/VREF_3		AE1	NC		

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	GND		U18			
N/A	GND		U17			
N/A	GND		U16			
N/A	GND		U15			
N/A	GND		U14			
N/A	GND		U13			
N/A	GND		U12			
N/A	GND		U6			
N/A	GND		T19			
N/A	GND		T18			
N/A	GND		T17			
N/A	GND		T16			
N/A	GND		T15			
N/A	GND		T14			
N/A	GND		T13			
N/A	GND		T12			
N/A	GND		R19			
N/A	GND		R18			
N/A	GND		R17			
N/A	GND		R16			
N/A	GND		R15			
N/A	GND		R14			
N/A	GND		R13			
N/A	GND		R12			
N/A	GND		P25			
N/A	GND		P19			
N/A	GND		P18			
N/A	GND		P17			
N/A	GND		P16			
N/A	GND		P15			
N/A	GND		P14			
N/A	GND		P13			
N/A	GND		P12			
N/A	GND		P6			
N/A	GND		N19			
N/A	GND		N18			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L38N_2	N10				
2	IO_L38P_2	N9				
2	IO_L39N_2	M7				
2	IO_L39P_2	M6				
2	IO_L40N_2/VREF_2	L2				
2	IO_L40P_2	M2				
2	IO_L41N_2	N8				
2	IO_L41P_2	N7				
2	IO_L42N_2	L4				
2	IO_L42P_2	L3				
2	IO_L43N_2	M4				
2	IO_L43P_2	M3				
2	IO_L44N_2	P10				
2	IO_L44P_2	P9				
2	IO_L45N_2	N6				
2	IO_L45P_2	N5				
2	IO_L46N_2/VREF_2	M1				
2	IO_L46P_2	N1				
2	IO_L47N_2	P8				
2	IO_L47P_2	P7				
2	IO_L48N_2	N4				
2	IO_L48P_2	N3				
2	IO_L49N_2	N2				
2	IO_L49P_2	P2				
2	IO_L50N_2	R10				
2	IO_L50P_2	R9				
2	IO_L51N_2	P6				
2	IO_L51P_2	P5				
2	IO_L52N_2/VREF_2	P4				
2	IO_L52P_2	P3				
2	IO_L53N_2	T11				
2	IO_L53P_2	U11				
2	IO_L54N_2	R7				
2	IO_L54P_2	R6				
2	IO_L55N_2	P1				
2	IO_L55P_2	R1				
2	IO_L56N_2	T10				
2	IO_L56P_2	T9				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	AG8				
N/A	GND	AG12				
N/A	GND	AG15				
N/A	GND	AG20				
N/A	GND	AG23				
N/A	GND	AG27				
N/A	GND	J34				
N/A	GND	AH7				
N/A	GND	AH28				
N/A	GND	AJ6				
N/A	GND	AJ29				
N/A	GND	AK5				
N/A	GND	AK12				
N/A	GND	AK23				
N/A	GND	AK30				
N/A	GND	AL4				
N/A	GND	AL31				
N/A	GND	AM1				
N/A	GND	AM2				
N/A	GND	AM10				
N/A	GND	AM16				
N/A	GND	AM19				
N/A	GND	AM25				
N/A	GND	AM33				
N/A	GND	AM34				
N/A	GND	AN1				
N/A	GND	AN34				

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
1	IO_L75N_1/GCLK3P	C17		
1	IO_L75P_1/GCLK2S	B17		
1	IO_L74N_1/GCLK1P	L17		
1	IO_L74P_1/GCLK0S	K17		
1	IO_L73N_1	E17		
1	IO_L73P_1	D17		
1	IO_L69N_1/VREF_1	G17		
1	IO_L69P_1	F17		
1	IO_L68N_1	J17		
1	IO_L68P_1	H17		
1	IO_L67N_1	C16		
1	IO_L67P_1	B16		
1	IO_L66N_1/VREF_1	G16	NC	
1	IO_L66P_1	F16	NC	
1	IO_L57N_1/VREF_1	B15		
1	IO_L57P_1	A15		
1	IO_L56N_1	L16		
1	IO_L56P_1	K16		
1	IO_L55N_1	D16		
1	IO_L55P_1	C15		
1	IO_L54N_1	F15		
1	IO_L54P_1	E15		
1	IO_L53_1/No_Pair	H16		
1	IO_L50_1/No_Pair	G15		
1	IO_L49N_1	B14		
1	IO_L49P_1	A14		
1	IO_L48N_1	D14		
1	IO_L48P_1	C14		
1	IO_L47N_1	L15		
1	IO_L47P_1	K15		
1	IO_L46N_1	F14		
1	IO_L46P_1	E14		
1	IO_L45N_1/VREF_1	H14		
1	IO_L45P_1	G14		
1	IO_L44N_1	L14		
1	IO_L44P_1	K14		
1	IO_L43N_1	C13		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
5	IO_L69P_5	AJ18		
5	IO_L68N_5	AF18		
5	IO_L68P_5	AG18		
5	IO_L67N_5	AM19		
5	IO_L67P_5	AN19		
5	IO_L66N_5/VREF_5	AH19	NC	
5	IO_L66P_5	AJ19	NC	
5	IO_L57N_5/VREF_5	AN20		
5	IO_L57P_5	AP20		
5	IO_L56N_5	AD19		
5	IO_L56P_5	AE19		
5	IO_L55N_5	AL19		
5	IO_L55P_5	AM20		
5	IO_L54N_5	AJ20		
5	IO_L54P_5	AK20		
5	IO_L53_5/No_Pair	AG19		
5	IO_L50_5/No_Pair	AH20		
5	IO_L49N_5	AN21		
5	IO_L49P_5	AP21		
5	IO_L48N_5	AL21		
5	IO_L48P_5	AM21		
5	IO_L47N_5	AD20		
5	IO_L47P_5	AE20		
5	IO_L46N_5	AJ21		
5	IO_L46P_5	AK21		
5	IO_L45N_5/VREF_5	AG21		
5	IO_L45P_5	AH21		
5	IO_L44N_5	AD21		
5	IO_L44P_5	AE21		
5	IO_L43N_5	AM22		
5	IO_L43P_5	AN22		
5	IO_L39N_5	AH22		
5	IO_L39P_5	AJ22		
5	IO_L38N_5	AF20		
5	IO_L38P_5	AF21		
5	IO_L37N_5	AN23		
5	IO_L37P_5	AP23		
5	IO_L27N_5/VREF_5	AL22		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L76N_6		AU42		
6	IO_L77P_6		AT39		
6	IO_L77N_6		AT40		
6	IO_L78P_6		AT41		
6	IO_L78N_6		AT42		
6	IO_L79P_6		AR38		
6	IO_L79N_6		AR39		
6	IO_L80P_6		AR37		
6	IO_L80N_6		AT38		
6	IO_L81P_6		AR40		
6	IO_L81N_6/VREF_6		AR41		
6	IO_L82P_6		AP36		
6	IO_L82N_6		AP37		
6	IO_L83P_6		AP35		
6	IO_L83N_6		AR36		
6	IO_L84P_6		AP38		
6	IO_L84N_6		AP39		
6	IO_L07P_6		AP41		
6	IO_L07N_6		AP42		
6	IO_L08P_6		AN35		
6	IO_L08N_6		AN36		
6	IO_L09P_6		AN37		
6	IO_L09N_6/VREF_6		AN38		
6	IO_L10P_6		AN41		
6	IO_L10N_6		AN42		
6	IO_L11P_6		AM33		
6	IO_L11N_6		AN34		
6	IO_L12P_6		AM36		
6	IO_L12N_6		AM37		
6	IO_L13P_6		AM38		
6	IO_L13N_6		AM39		
6	IO_L14P_6		AM34		
6	IO_L14N_6		AM35		
6	IO_L15P_6		AN40		
6	IO_L15N_6/VREF_6		AM40		
6	IO_L16P_6		AM41		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
1	VCCO_1		D18		
2	VCCO_2		AA15		
2	VCCO_2		AA14		
2	VCCO_2		Y15		
2	VCCO_2		Y14		
2	VCCO_2		Y8		
2	VCCO_2		Y5		
2	VCCO_2		W15		
2	VCCO_2		W14		
2	VCCO_2		V15		
2	VCCO_2		V14		
2	VCCO_2		V3		
2	VCCO_2		U15		
2	VCCO_2		U14		
2	VCCO_2		T15		
2	VCCO_2		T14		
2	VCCO_2		R14		
2	VCCO_2		T9		
2	VCCO_2		P4		
2	VCCO_2		M6		
2	VCCO_2		J3		
2	VCCO_2		F5		
3	VCCO_3		AU5		
3	VCCO_3		AP3		
3	VCCO_3		AL6		
3	VCCO_3		AJ4		
3	VCCO_3		AH14		
3	VCCO_3		AG15		
3	VCCO_3		AG14		
3	VCCO_3		AG9		
3	VCCO_3		AF15		
3	VCCO_3		AF14		
3	VCCO_3		AE15		
3	VCCO_3		AE14		
3	VCCO_3		AE3		
3	VCCO_3		AD15		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		AB18		
N/A	GND		AB17		
N/A	GND		AB11		
N/A	GND		AB8		
N/A	GND		AB5		
N/A	GND		AC41		
N/A	GND		AC26		
N/A	GND		AC25		
N/A	GND		AC24		
N/A	GND		AC23		
N/A	GND		AC22		
N/A	GND		AC21		
N/A	GND		AC20		
N/A	GND		AC19		
N/A	GND		AC18		
N/A	GND		AC17		
N/A	GND		AC2		
N/A	GND		AD26		
N/A	GND		AD25		
N/A	GND		AD24		
N/A	GND		AD23		
N/A	GND		AD22		
N/A	GND		AD21		
N/A	GND		AD20		
N/A	GND		AD19		
N/A	GND		AD18		
N/A	GND		AD17		
N/A	GND		AE37		
N/A	GND		AE34		
N/A	GND		AE26		
N/A	GND		AE25		
N/A	GND		AE24		
N/A	GND		AE23		
N/A	GND		AE22		
N/A	GND		AE21		
N/A	GND		AE20		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
4	IO_L58P_4	AW19	
4	IO_L59N_4	AP19	
4	IO_L59P_4	AN19	
4	IO_L60N_4	BB19	
4	IO_L60P_4	BA19	
4	IO_L64N_4	AU20	
4	IO_L64P_4	AT20	
4	IO_L65N_4	AL21	
4	IO_L65P_4	AL20	
4	IO_L66N_4	BA20	
4	IO_L66P_4/VREF_4	AY20	
4	IO_L67N_4	AR21	
4	IO_L67P_4	AP21	
4	IO_L68N_4	AN20	
4	IO_L68P_4	AM20	
4	IO_L69N_4	AU21	
4	IO_L69P_4/VREF_4	AT21	
4	IO_L73N_4	AW21	
4	IO_L73P_4	AV21	
4	IO_L74N_4/GCLK3S	AN21	
4	IO_L74P_4/GCLK2P	AM21	
4	IO_L75N_4/GCLK1S	BA21	
4	IO_L75P_4/GCLK0P	AY21	
5	IO_L75N_5/GCLK7S	AY22	
5	IO_L75P_5/GCLK6P	BA22	
5	IO_L74N_5/GCLK5S	AM22	
5	IO_L74P_5/GCLK4P	AN22	
5	IO_L73N_5	AV22	
5	IO_L73P_5	AW22	
5	IO_L69N_5/VREF_5	AT22	
5	IO_L69P_5	AU22	
5	IO_L68N_5	AM23	
5	IO_L68P_5	AN23	
5	IO_L67N_5	AP22	
5	IO_L67P_5	AR22	
5	IO_L66N_5/VREF_5	AY23	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L52P_6	AF40	
6	IO_L52N_6	AF41	
6	IO_L53P_6	AC36	
6	IO_L53N_6	AC37	
6	IO_L54P_6	AE41	
6	IO_L54N_6	AE42	
6	IO_L55P_6	AE40	
6	IO_L55N_6	AD40	
6	IO_L56P_6	AC31	
6	IO_L56N_6	AC32	
6	IO_L57P_6	AE38	
6	IO_L57N_6/VREF_6	AE39	
6	IO_L58P_6	AD41	
6	IO_L58N_6	AD42	
6	IO_L59P_6	AB35	
6	IO_L59N_6	AB36	
6	IO_L60P_6	AD37	
6	IO_L60N_6	AD38	
6	IO_L85P_6	AC40	
6	IO_L85N_6	AC41	
6	IO_L86P_6	AB33	
6	IO_L86N_6	AB34	
6	IO_L87P_6	AC39	
6	IO_L87N_6/VREF_6	AB39	
6	IO_L88P_6	AB40	
6	IO_L88N_6	AB41	
6	IO_L89P_6	AB31	
6	IO_L89N_6	AB32	
6	IO_L90P_6	AB37	
6	IO_L90N_6	AB38	
7	IO_L90P_7	AA40	
7	IO_L90N_7	AA41	
7	IO_L89P_7	AA35	
7	IO_L89N_7	AA36	
7	IO_L88P_7	Y39	
7	IO_L88N_7/VREF_7	AA39	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD22	
N/A	GND	AC22	
N/A	GND	AB22	
N/A	GND	AA22	
N/A	GND	Y22	
N/A	GND	W22	
N/A	GND	V22	
N/A	GND	U22	
N/A	GND	AF21	
N/A	GND	AE21	
N/A	GND	AD21	
N/A	GND	AC21	
N/A	GND	AB21	
N/A	GND	AA21	
N/A	GND	Y21	
N/A	GND	W21	
N/A	GND	V21	
N/A	GND	U21	
N/A	GND	BB20	
N/A	GND	AV20	
N/A	GND	AP20	
N/A	GND	AF20	
N/A	GND	AE20	
N/A	GND	AD20	
N/A	GND	AC20	
N/A	GND	AB20	
N/A	GND	AA20	
N/A	GND	Y20	
N/A	GND	W20	
N/A	GND	V20	
N/A	GND	U20	
N/A	GND	J20	
N/A	GND	E20	
N/A	GND	A20	
N/A	GND	AL19	
N/A	GND	AF19	
N/A	GND	AE19	