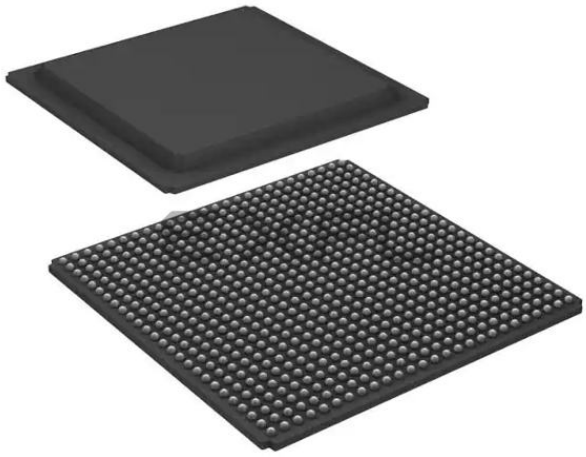

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3424
Number of Logic Elements/Cells	30816
Total RAM Bits	2506752
Number of I/O	416
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp30-5fg676c

cation is given at the receiver interface. The realignment indicator is a distinct output.

The transceiver continuously monitors the data for the presence of the 10-bit character(s). Upon each occurrence of a 10-bit character, the data is checked for word alignment. If comma detect is disabled, the data is not aligned to any particular pattern. The programmable option allows a user to align data on comma+, comma–, both, or a unique user-defined and programmed sequence.

Comma detection has been expanded beyond 10-bit symbol detection and alignment to include 8-bit symbol detection and alignment for 16-, 20-, 32-, and 40-bit paths. The ability to detect symbols, and then either align to 1-word, 2-word, or 4-word boundaries is included. The RXSLIDE input allows the user to “slide” or “slip” the alignment by one bit in each 16-, 20-, 32- and 40-bit mode at any time for SONET applications. Comma detection can be bypassed when needed.

Clock Correction

RXRECCLK (the recovered clock) reflects the data rate of the incoming data. RXUSRCLK defines the rate at which the FPGA fabric consumes the data. Ideally, these rates are identical. However, since the clocks typically have different sources, one of the clocks will be faster than the other. The receiver buffer accommodates this difference between the clock rates. See Figure 6.

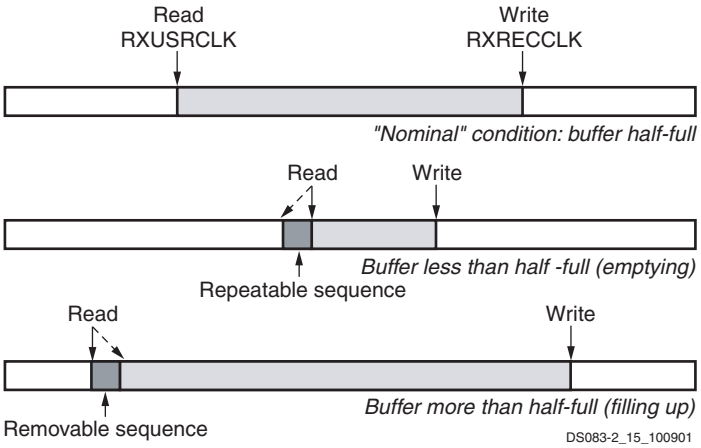

Figure 6: **Clock Correction in Receiver**

Nominally, the buffer is always half full. This is shown in the top buffer, Figure 6, where the shaded area represents buffered data not yet read. Received data is inserted via the write pointer under control of RXRECCLK. The FPGA fabric reads data via the read pointer under control of RXUSRCLK. The half full/half empty condition of the buffer gives a cushion for the differing clock rates. This operation continues indefinitely, regardless of whether or not "meaningful" data is being received. When there is no meaningful data to be received, the incoming data will consist of IDLE characters or other padding.

If RXUSRCLK is faster than RXRECCLK, the buffer becomes more empty over time. The clock correction logic corrects for this by decrementing the read pointer to reread a repeatable byte sequence. This is shown in the middle buffer, Figure 6, where the solid read pointer decrements to the value represented by the dashed pointer. By decrementing the read pointer instead of incrementing it in the usual fashion, the buffer is partially refilled. The transceiver design will repeat a single repeatable byte sequence when necessary to refill a buffer. If the byte sequence length is greater than one, and if attribute CLK_COR_REPEAT_WAIT is 0, then the transceiver may repeat the same sequence multiple times until the buffer is refilled to the desired extent.

Similarly, if RXUSRCLK is slower than RXRECCLK, the buffer will fill up over time. The clock correction logic corrects for this by incrementing the read pointer to skip over a removable byte sequence that need not appear in the final FPGA fabric byte stream. This is shown in the bottom buffer, Figure 6, where the solid read pointer increments to the value represented by the dashed pointer. This accelerates the emptying of the buffer, preventing its overflow. The transceiver design will skip a single byte sequence when necessary to partially empty a buffer. If attribute CLK_COR_REPEAT_WAIT is 0, the transceiver may also skip two consecutive removable byte sequences in one step to further empty the buffer when necessary.

These operations require the clock correction logic to recognize a byte sequence that can be freely repeated or omitted in the incoming data stream. This sequence is generally an IDLE sequence, or other sequence comprised of special values that occur in the gaps separating packets of meaningful data. These gaps are required to occur sufficiently often to facilitate the timely execution of clock correction.

Channel Bonding

Some gigabit I/O standards such as Infiniband specify the use of multiple transceivers in parallel for even higher data rates. Words of data are split into bytes, with each byte sent over a separate channel (transceiver). See Figure 7.

The top half of the figure shows the transmission of words split across four transceivers (channels or lanes). PPPP, QQQQ, RRRR, SSSS, and TTTT represent words sent over the four channels.

The bottom-left portion of Figure 7 shows the initial situation in the FPGA’s receivers at the other end of the four channels. Due to variations in transmission delay—especially if the channels are routed through repeaters—the FPGA fabric might not correctly assemble the bytes into complete words. The bottom-left illustration shows the incorrect assembly of data words PQPP, QRQQ, RSRR, and so forth.

To support correction of this misalignment, the data stream includes special byte sequences that define corresponding points in the several channels. In the bottom half of Figure 7, the shaded "P" bytes represent these special characters. Each receiver recognizes the "P" channel bond-

Functional Description: RocketIO Multi-Gigabit Transceiver (MGT)

This section summarizes the features of the RocketIO multi-gigabit transceiver. For an in-depth discussion of the RocketIO MGT, including digital and analog design considerations, refer to the ***RocketIO Transceiver User Guide***.

RocketIO Overview

Up to twenty RocketIO MGTs are available. The MGT is designed to operate at any baud rate in the range of 622 Mb/s to 3.125 Gb/s per channel. This includes specific baud rates used by various standards as listed in Table 4.

The RocketIO MGT consists of the *Physical Media Attachment* (PMA) and *Physical Coding Sublayer* (PCS). The PMA contains the 3.125 Gb/s serializer/deserializer (SERDES), TX/RX buffers, clock generator, and clock recovery circuitry. The PCS contains the bypassable 8B/10B encoder/ decoder, elastic buffers, and Cyclic Redundancy Check (CRC) units. The encoder and decoder handle the 8B/10B coding scheme. The elastic buffers support the clock correction (rate matching) and channel bonding features. The CRC units perform CRC generation and checking.

See Table 7, page 17, for a summary of the differences between the RocketIO X PMA/PCS and the RocketIO PMA/PCS.

Figure 10, page 11 shows a high-level block diagram of the RocketIO transceiver and its FPGA interface signals.

Table 4: **Protocols Supported by RocketIO Transceiver**

Mode	Channels (Lanes)(1)	I/O Bit Rate (Gb/s)
Fibre Channel	1	1.06
		2.12
		3.1875 (2)
Gigabit Ethernet	1	1.25
10Gbit Ethernet	4	3.125
Infiniband	1, 4, 12	2.5
Aurora	1, 2, 3, 4, ...	0.622 – 3.125
Custom Protocol	1, 2, 3, 4, ...	up to 3.125

Notes:
1. One channel is considered to be one transceiver.
2. Virtex-II Pro MGT can support the 10G Fibre Channel data rates of 3.1875 Gb/s across 6" of standard FR-4 PCB and one connector (Molex 74441 or equivalent) with a bit error rate of 10^{-12} or better.

PMA

Transmitter Output

The RocketIO transceiver is implemented in *Current Mode Logic* (CML). A CML transmitter output consists of transistors configured as shown in Figure 8. CML uses a positive supply and offers easy interface requirements. In this configuration, both legs of the driver, VP and VN, sink current, with one leg always sinking more current than its complement. The CML output consists of a differential pair with 50Ω (or, optionally, 75Ω) source resistors. The signal swing is created by switching the current in a common-source differential pair.

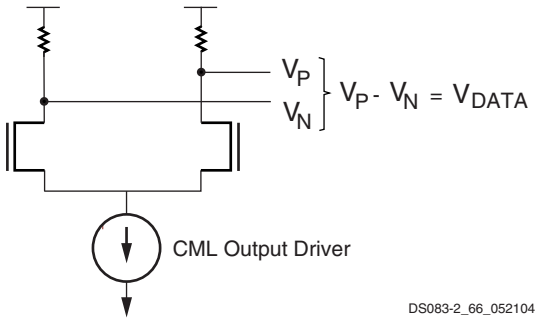

Figure 8: **CML Output Configuration**

Transmitter Termination

On-chip termination is provided at the transmitter, eliminating the need for external termination. The output driver and termination are powered by V_{TTX}. This configuration uses a CML approach with selectable 50Ω or 75Ω termination to TXP and TXN as shown in Figure 9.

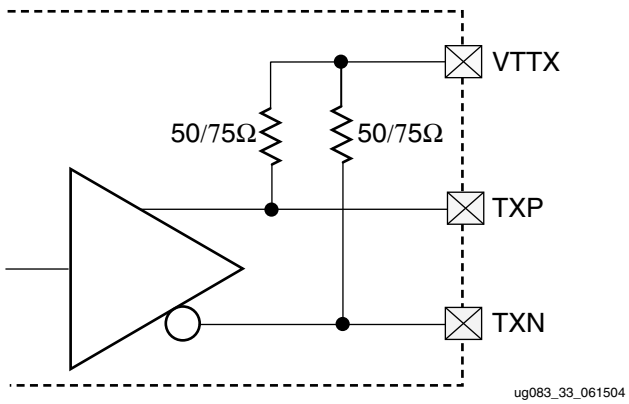

Figure 9: **RocketIO Transmit Termination**

Functional Description: Processor Block

This section briefly describes the interfaces and components of the Processor Block. The subsequent section, Functional Description: Embedded PowerPC 405 Core beginning on page 20, offers a summary of major PPC405 core features. For an in-depth discussion on both the Processor Block and PPC405, see tthe **PowerPC Processor Reference Guide** and the **PowerPC 405 Processor Block Reference Guide** available on the Xilinx website at **http://www.xilinx.com**.

Processor Block Overview

Figure 14 shows the internal architecture of the Processor Block.

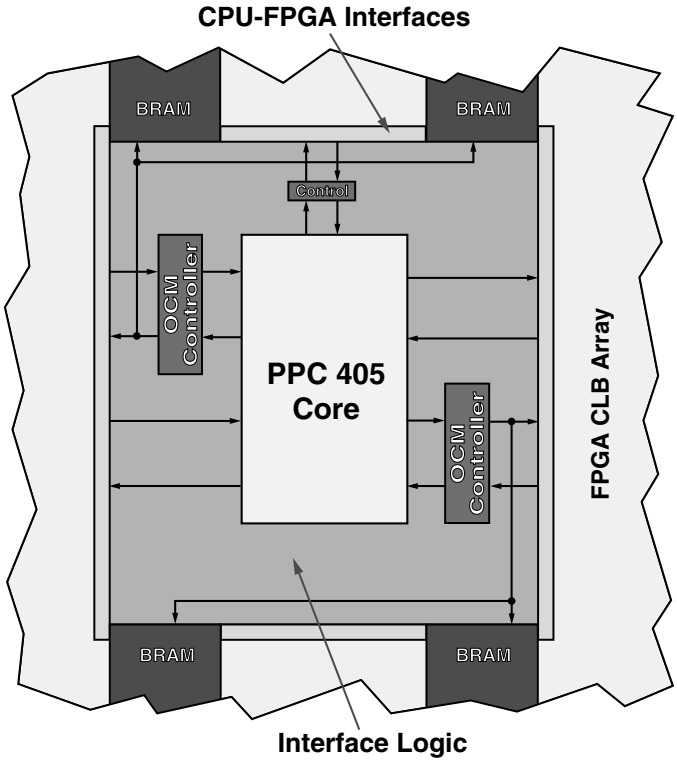

Figure 14: **Processor Block Architecture**

Within the Virtex-II Pro Processor Block, there are four components:

- Embedded IBM PowerPC 405-D5 RISC CPU core
- On-Chip Memory (OCM) controllers and interfaces
- Clock/control interface logic
- CPU-FPGA Interfaces

Embedded PowerPC 405 RISC Core

The PowerPC 405D5 core is a 0.13 µm implementation of the IBM PowerPC 405D4 core. The advanced process technology enables the embedded PowerPC 405 (PPC405) core to operate at 300+ MHz while maintaining low power consumption. Specially designed interface logic integrates the core with the surrounding CLBs, block RAMs, and general routing resources. Up to four Processor Blocks can be available in a single Virtex-II Pro device.

The embedded PPC405 core implements the PowerPC User Instruction Set Architecture (UISA), user-level registers, programming model, data types, and addressing modes for 32-bit fixed-point operations. 64-bit operations, auxiliary processor operations, and floating-point operations are trapped and can be emulated in software.

Most of the PPC405 core features are compatible with the specifications for the PowerPC Virtual Environment Architecture (VEA) and Operating Environment Architecture (OEA). They also provide a number of optimizations and extensions to the lower layers of the PowerPC Architecture. The full architecture of the PPC405 is defined by the PowerPC Embedded Environment and PowerPC UISA documentation, available from IBM.

On-Chip Memory (OCM) Controllers

Introduction

The OCM controllers serve as dedicated interfaces between the block RAMs in the FPGA fabric (see 18 Kb Block SelectRAM+ Resources, page 44) and OCM signals available on the embedded PPC405 core. The OCM signals on the PPC405 core are designed to provide very quick access to a fixed amount of instruction and data memory space. The OCM controller provides an interface to both the 64-bit Instruction-Side Block RAM (ISBRAM) and the 32-bit Data-Side Block RAM (DSBRAM). The designer can choose to implement:

- ISBRAM only
- DSBRAM only
- Both ISBRAM and DSBRAM
- No ISBRAM and no DSBRAM

One of OCM's primary advantages is that it guarantees a fixed latency of execution for a higher level of determinism. Additionally, it reduces cache pollution and thrashing, since the cache remains available for caching code from other memory resources.

Typical applications for DSOCM include scratch-pad memory, as well as use of the dual-port feature of block RAM to enable bidirectional data transfer between processor and FPGA. Typical applications for ISOCM include storage of interrupt service routines.

Functional Features

Common Features

- Separate Instruction and Data memory interface between processor core and BRAMs in FPGA
- Dedicated interface to Device Control Register (DCR) bus for ISOCM and DSOCM

Date	Version	Revision
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s.
03/05/07	4.6	*No changes in Module 2 for this revision.*
11/05/07	4.7	• Updated copyright notice and legal disclaimer. • Debug Interface, page 19, and Boundary-Scan (JTAG, IEEE 1532) Mode, page 57: Updated IEEE 1149.1 compliance statement.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner.

Notice of Disclaimer

Virtex-II Pro Data Sheet

The Virtex-II Pro Data Sheet contains the following modules:

- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Functional Description (Module 2)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Pinout Information (Module 4)

Table 25: **RocketIO Receiver Switching Characteristics**

Description	Symbol	Conditions	Min	Typ	Max	Units
Receive total jitter tolerance	T_{JTOL}	2.126 Gb/s – 3.125 Gb/s			0.65	UI(1)
		1.0626 Gb/s – 2.125 Gb/s			0.65	UI
		1.0 Gb/s – 1.0625 Gb/s			0.68	UI
		600 Mb/s – 999 Mb/s			0.68(2)	UI
Receive deterministic jitter tolerance	T_{DJTOL}	2.126 Gb/s – 3.125 Gb/s			0.41	UI
		1.0626 Gb/s – 2.125 Gb/s			0.43	UI
		1.0 Gb/s – 1.0625 Gb/s			0.47	UI
		600 Mb/s – 999 Mb/s			0.47(2)	
Receive latency(3)	T_{RXLAT}			25	42(4)	RXUSRCLK cycles
RXUSRCLK duty cycle	T_{RXDC}		45	50	55	%
RXUSRCLK2 duty cycle	T_{RX2DC}		45	50	55	%

Notes:

1. UI = Unit Interval
2. The oversampling techniques described in **XAPP572** are required to meet these specifications for serial rates less than 1 Gb/s.
3. Receive latency delay RXP/RXN to RXDATA. Refer to ***RocketIO Transceiver User Guide*** for more information on calculating latency.
4. This maximum may occur when certain conditions are present and clock correction and channel bonding are enabled. If these functions are both disabled, the maximum will be near the typical values.

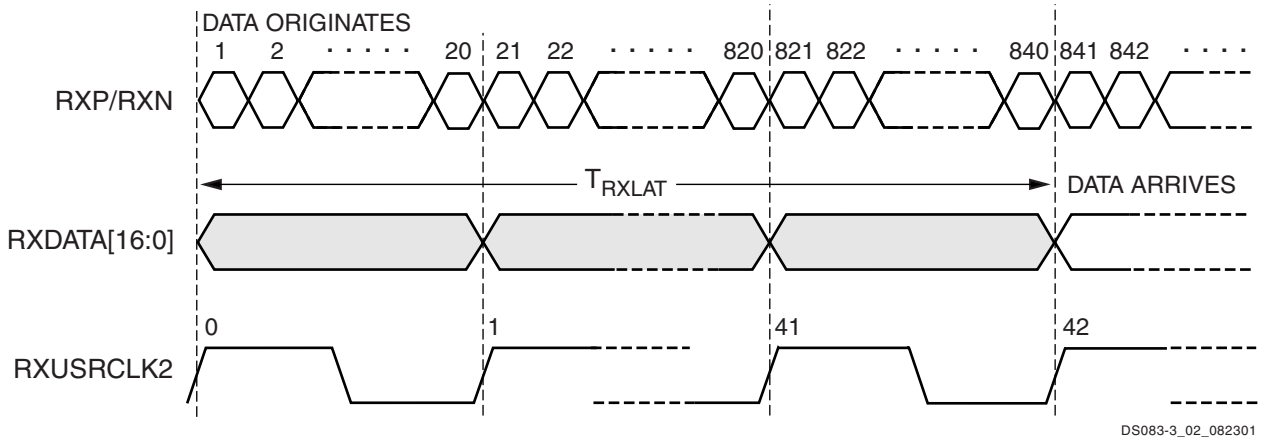

Figure 4: **RocketIO Receive Latency (Maximum)**

JTAG Test Access Port Switching Characteristics

Characterization data for some of the most commonly requested timing parameters shown in Figure 11 is listed in Table 52.

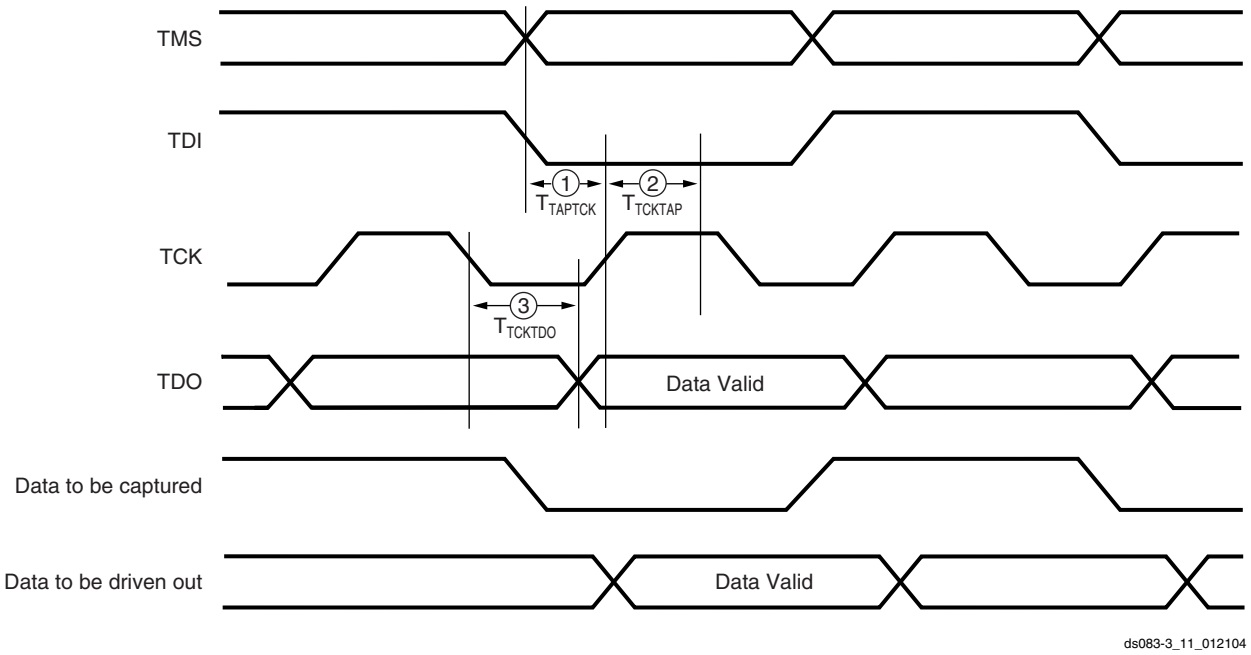

Figure 11: **Virtex-II Pro Boundary Scan Port Timing Waveforms**

Table 52: **Boundary-Scan Port Timing Specifications**

	Description	Figure References	Symbol	Value	Units
TCK	TMS and TDI setup time	1	T_{TAPTCK}	5.5	ns, min
	TMS and TDI hold times	2	T_{TCKTAP}	2.0	ns, min
	Falling edge to TDO output valid	3	T_{TCKTDO}	11.0	ns, max
	Maximum frequency		F_{TCK}	33.0	MHz, max

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-II Pro source-synchronous transmitter and receiver data-valid windows.

Table 64: **Duty Cycle Distortion and Clock-Tree Skew**

Description	Symbol	Device	Speed Grade			Units
			–7	–6	–5	
Duty Cycle Distortion(1)	T_{DCD_LOCAL}	All	0.10	0.10	0.20	ns
	T_{DCD_CLK180}		0.10	0.11	0.13	ns
Clock Tree Skew(2)	T_{CKSKEW}	XC2VP2	0.13	0.13	0.13	ns
		XC2VP4	0.13	0.13	0.13	ns
		XC2VP7	0.13	0.13	0.13	ns
		XC2VP20	0.20	0.21	0.22	ns
		XC2VPX20	0.20	0.21	0.22	ns
		XC2VP30	0.20	0.22	0.24	ns
		XC2VP40	0.33	0.34	0.35	ns
		XC2VP50	0.40	0.41	0.42	ns
		XC2VP70	0.54	0.59	0.64	ns
		XC2VPX70	0.54	0.59	0.64	ns
		XC2VP100	N/A	0.79	0.87	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.

   T_{DCD_LOCAL} applies to cases where the dedicated path from the DCM to the BUFG is bypassed and where local (IOB) inversion is used to provide the negative-edge clock to the DDR element in the I/O. Users must follow the implementation guidelines contained in **XAPP685** for these specifications to apply.

   T_{DCD_CLK180} applies to cases where the CLK180 output of the DCM is used to provide the negative-edge clock to the DDR element in the I/O.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 4: **Virtex-II Pro Pin Definitions *(Continued)***

Pin Name	Direction	Description
GCLKx (S/P)	Input/Output	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks. These pins can be used to clock the RocketIO transceiver. See the **RocketIO Transceiver User Guide** for design guidelines and BREFCLK-specific pins, by device.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
V_{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins:(1)		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection. Pin is biased by V_{CCAUX} (must be 2.5V). These pins should not connect to 3.3V unless 100Ω series resistors are used. The mode pins are not to be toggled (changed) while in operation during and after configuration.
HSWAP_EN	Input	Enable I/O pull-ups during configuration.
TCK	Input	Boundary Scan Clock. This pin is 3.3V compatible.
TDI	Input	Boundary Scan Data Input. This pin is 3.3V compatible.
TDO	Output (open-drain)	Boundary Scan Data Output. Pin is open-drain and can be pulled up to 3.3V. It is recommended that the external pull-up be greater than 200Ω. There is no internal pull-up.
TMS	Input	Boundary Scan Mode Select. This pin is 3.3V compatible.
PWRDWN_B	Input *(unsupported)*	Active Low power-down pin (unsupported). *Driving this pin Low can adversely affect device operation and configuration.* PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up.
Other Pins:		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V_{BATT}	Input	Decryptor key memory backup supply. (Connect to V_{CCAUX} or GND if battery not used.)
RSVD	N/A	Reserved pin - do not connect.
V_{CCO}	Input	Power-supply pins for the output drivers (per bank).
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V_{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.
AVCCAUXRX#	Input	Analog power supply for receive circuitry of the RocketIO MGT (2.5V).
AVCCAUXTX#	Input	Analog power supply for transmit circuitry of the RocketIO MGT (2.5V).
BREFCLKN, BREFCLKP(2)	Input	Differential clock input that clocks the RocketIO X MGTs populating the same side of the chip (top or bottom). Can also drive DCMs for RocketIO X MGT use.

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
5	IO_L74P_5/GCLK4P	AB14			
5	IO_L73N_5	AA14			
5	IO_L73P_5	Y14			
5	IO_L69N_5/VREF_5	W14			
5	IO_L69P_5	W15			
5	IO_L68N_5	AD15			
5	IO_L68P_5	AC15			
5	IO_L67N_5	AB15			
5	IO_L67P_5	AA15			
5	IO_L45N_5/VREF_5	AC16	NC	NC	
5	IO_L45P_5	AB16	NC	NC	
5	IO_L44N_5	Y15	NC	NC	
5	IO_L44P_5	Y16	NC	NC	
5	IO_L43N_5	AC17	NC	NC	
5	IO_L43P_5	AB17	NC	NC	
5	IO_L39N_5	AA16	NC	NC	
5	IO_L39P_5	AA17	NC	NC	
5	IO_L38N_5	W16	NC	NC	
5	IO_L38P_5	Y17	NC	NC	
5	IO_L37N_5	AD18	NC	NC	
5	IO_L37P_5	AC18	NC	NC	
5	IO_L09N_5/VREF_5	AA18			
5	IO_L09P_5	Y18			
5	IO_L08N_5	AF19			
5	IO_L08P_5	AE19			
5	IO_L07N_5/VREF_5	AD19			
5	IO_L07P_5	AC19			
5	IO_L06N_5/VRP_5	AB18			
5	IO_L06P_5/VRN_5	AB19			
5	IO_L05_5/No_Pair	Y19			
5	IO_L03N_5/D4	AA19			
5	IO_L03P_5/D5	AA20			
5	IO_L02N_5/D6	AC20			
5	IO_L02P_5/D7	AB20			
5	IO_L01N_5/RDWR_B	AD21			
5	IO_L01P_5/CS_B	AC21			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L52N_6	U22	NC		
6	IO_L53P_6	U23	NC		
6	IO_L53N_6	U24	NC		
6	IO_L54P_6	V26	NC		
6	IO_L54N_6	U26	NC		
6	IO_L55P_6	U20	NC		
6	IO_L55N_6	T19	NC		
6	IO_L56P_6	T20	NC		
6	IO_L56N_6	R20	NC		
6	IO_L57P_6	T21	NC		
6	IO_L57N_6/VREF_6	T22	NC		
6	IO_L58P_6	T23	NC		
6	IO_L58N_6	T24	NC		
6	IO_L59P_6	T25	NC		
6	IO_L59N_6	T26	NC		
6	IO_L60P_6	R19	NC		
6	IO_L60N_6	P19	NC		
6	IO_L85P_6	R21			
6	IO_L85N_6	R22			
6	IO_L86P_6	R23			
6	IO_L86N_6	R24			
6	IO_L87P_6	R25			
6	IO_L87N_6/VREF_6	R26			
6	IO_L88P_6	P20			
6	IO_L88N_6	P21			
6	IO_L89P_6	P22			
6	IO_L89N_6	P23			
6	IO_L90P_6	P24			
6	IO_L90N_6	P25			
7	IO_L90P_7	N25			
7	IO_L90N_7	N24			
7	IO_L89P_7	N23			
7	IO_L89N_7	N22			
7	IO_L88P_7	N21			
7	IO_L88N_7/VREF_7	N20			
7	IO_L87P_7	M26			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
0	IO_L01N_0/VRP_0		E25			
0	IO_L01P_0/VRN_0		E24			
0	IO_L02N_0		F24			
0	IO_L02P_0		F23			
0	IO_L03N_0		E23			
0	IO_L03P_0/VREF_0		E22			
0	IO_L05_0/No_Pair		G23			
0	IO_L06N_0		H22			
0	IO_L06P_0		G22			
0	IO_L07N_0		F22			
0	IO_L07P_0		F21			
0	IO_L08N_0		D24			
0	IO_L08P_0		C24			
0	IO_L09N_0		H21			
0	IO_L09P_0/VREF_0		G21			
0	IO_L37N_0		E21			
0	IO_L37P_0		D21			
0	IO_L38N_0		D23			
0	IO_L38P_0		C23			
0	IO_L39N_0		H20			
0	IO_L39P_0		G20			
0	IO_L43N_0		E20			
0	IO_L43P_0		D20			
0	IO_L44N_0		B23			
0	IO_L44P_0		A23			
0	IO_L45N_0		H19			
0	IO_L45P_0/VREF_0		G19			
0	IO_L46N_0		E19	NC		
0	IO_L46P_0		E18	NC		
0	IO_L47N_0		C22	NC		
0	IO_L47P_0		B22	NC		
0	IO_L48N_0		F20	NC		
0	IO_L48P_0		F19	NC		
0	IO_L49N_0		G17	NC		
0	IO_L49P_0		F17	NC		
0	IO_L50_0/No_Pair		B21	NC		

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
2	IO_L41N_2		L8	NC		
2	IO_L41P_2		L7	NC		
2	IO_L42N_2		H4	NC		
2	IO_L42P_2		H3	NC		
2	IO_L43N_2		H2			
2	IO_L43P_2		J2			
2	IO_L44N_2		M8			
2	IO_L44P_2		M7			
2	IO_L45N_2		K6			
2	IO_L45P_2		K5			
2	IO_L46N_2/VREF_2		J1			
2	IO_L46P_2		K1			
2	IO_L47N_2		M6			
2	IO_L47P_2		M5			
2	IO_L48N_2		J4			
2	IO_L48P_2		J3			
2	IO_L49N_2		K2			
2	IO_L49P_2		L2			
2	IO_L50N_2		N8			
2	IO_L50P_2		N7			
2	IO_L51N_2		K4			
2	IO_L51P_2		K3			
2	IO_L52N_2/VREF_2		L1			
2	IO_L52P_2		M1			
2	IO_L53N_2		N6			
2	IO_L53P_2		N5			
2	IO_L54N_2		L5			
2	IO_L54P_2		L4			
2	IO_L55N_2		M2			
2	IO_L55P_2		N2			
2	IO_L56N_2		P9			
2	IO_L56P_2		R9			
2	IO_L57N_2		M4			
2	IO_L57P_2		M3			
2	IO_L58N_2/VREF_2		N1			
2	IO_L58P_2		P1			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	GND		N17			
N/A	GND		N16			
N/A	GND		N15			
N/A	GND		N14			
N/A	GND		N13			
N/A	GND		N12			
N/A	GND		M19			
N/A	GND		M18			
N/A	GND		M17			
N/A	GND		M16			
N/A	GND		M15			
N/A	GND		M14			
N/A	GND		M13			
N/A	GND		M12			
N/A	GND		L28			
N/A	GND		L25			
N/A	GND		L20			
N/A	GND		L11			
N/A	GND		L6			
N/A	GND		L3			
N/A	GND		H30			
N/A	GND		H1			
N/A	GND		F25			
N/A	GND		F18			
N/A	GND		F13			
N/A	GND		F6			
N/A	GND		E26			
N/A	GND		E5			
N/A	GND		D27			
N/A	GND		D22			
N/A	GND		D19			
N/A	GND		D12			
N/A	GND		D9			
N/A	GND		D4			
N/A	GND		C28			
N/A	GND		C17			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L05N_2	J8				
2	IO_L05P_2	J7				
2	IO_L06N_2	F5				
2	IO_L06P_2	F4				
2	IO_L15N_2	G4	NC			
2	IO_L15P_2	G3	NC			
2	IO_L16N_2/VREF_2	G6	NC			
2	IO_L16P_2	G5	NC			
2	IO_L17N_2	F2	NC			
2	IO_L17P_2	F1	NC			
2	IO_L18N_2	L10	NC			
2	IO_L18P_2	L9	NC			
2	IO_L19N_2	H6	NC			
2	IO_L19P_2	H5	NC			
2	IO_L20N_2	G2	NC			
2	IO_L20P_2	G1	NC			
2	IO_L21N_2	J6	NC			
2	IO_L21P_2	J5	NC			
2	IO_L22N_2/VREF_2	J4	NC			
2	IO_L22P_2	J3	NC			
2	IO_L23N_2	K8	NC			
2	IO_L23P_2	K7	NC			
2	IO_L24N_2	H4	NC			
2	IO_L24P_2	H3	NC			
2	IO_L31N_2	H2				
2	IO_L31P_2	H1				
2	IO_L32N_2	M10				
2	IO_L32P_2	M9				
2	IO_L33N_2	K5				
2	IO_L33P_2	K4				
2	IO_L34N_2/VREF_2	J2				
2	IO_L34P_2	K2				
2	IO_L35N_2	L8				
2	IO_L35P_2	L7				
2	IO_L36N_2	L6				
2	IO_L36P_2	L5				
2	IO_L37N_2	K1				
2	IO_L37P_2	L1				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
4	VCCO_4	AD15				
4	VCCO_4	AJ10				
4	VCCO_4	AK15				
4	VCCO_4	AM6				
5	VCCO_5	AC18				
5	VCCO_5	AC19				
5	VCCO_5	AC20				
5	VCCO_5	AC21				
5	VCCO_5	AC22				
5	VCCO_5	AD20				
5	VCCO_5	AD21				
5	VCCO_5	AD22				
5	VCCO_5	AD23				
5	VCCO_5	AJ25				
5	VCCO_5	AK20				
5	VCCO_5	AM29				
6	VCCO_6	V23				
6	VCCO_6	W23				
6	VCCO_6	Y23				
6	VCCO_6	Y24				
6	VCCO_6	Y30				
6	VCCO_6	AA23				
6	VCCO_6	AA24				
6	VCCO_6	AB23				
6	VCCO_6	AB24				
6	VCCO_6	AC24				
6	VCCO_6	AE29				
6	VCCO_6	AJ32				
7	VCCO_7	F32				
7	VCCO_7	K29				
7	VCCO_7	M24				
7	VCCO_7	N23				
7	VCCO_7	N24				
7	VCCO_7	P23				
7	VCCO_7	P24				
7	VCCO_7	R23				
7	VCCO_7	R24				
7	VCCO_7	R30				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
3	IO_L55N_3	Y1		
3	IO_L55P_3	Y2		
3	IO_L54N_3	AA5		
3	IO_L54P_3	AA6		
3	IO_L53N_3	Y10		
3	IO_L53P_3	Y11		
3	IO_L52N_3	AA4		
3	IO_L52P_3	AB4		
3	IO_L51N_3/VREF_3	AA1		
3	IO_L51P_3	AA2		
3	IO_L50N_3	Y9		
3	IO_L50P_3	AA9		
3	IO_L49N_3	AB6		
3	IO_L49P_3	AB7		
3	IO_L48N_3	AB2		
3	IO_L48P_3	AB3		
3	IO_L47N_3	AA10		
3	IO_L47P_3	AA11		
3	IO_L46N_3	AC5		
3	IO_L46P_3	AC6		
3	IO_L45N_3/VREF_3	AC3		
3	IO_L45P_3	AC4		
3	IO_L44N_3	AA7		
3	IO_L44P_3	AA8		
3	IO_L43N_3	AC1		
3	IO_L43P_3	AC2		
3	IO_L42N_3	AD5		
3	IO_L42P_3	AD6		
3	IO_L41N_3	AB10		
3	IO_L41P_3	AB11		
3	IO_L40N_3	AD3		
3	IO_L40P_3	AE3		
3	IO_L39N_3/VREF_3	AD1		
3	IO_L39P_3	AD2		
3	IO_L38N_3	AB8		
3	IO_L38P_3	AC7		
3	IO_L37N_3	AE5		
3	IO_L37P_3	AE6		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
1	IO_L64N_1	E18		
1	IO_L64P_1	D18		
1	IO_L60N_1	G18		
1	IO_L60P_1	F18		
1	IO_L59N_1	L18		
1	IO_L59P_1	K18		
1	IO_L58N_1	J18		
1	IO_L58P_1	H18		
1	IO_L57N_1/VREF_1	D17		
1	IO_L57P_1	C17		
1	IO_L56N_1	N18		
1	IO_L56P_1	M18		
1	IO_L55N_1	E17		
1	IO_L55P_1	E16		
1	IO_L54N_1	G17		
1	IO_L54P_1	F16		
1	IO_L53_1/No_Pair	J17		
1	IO_L50_1/No_Pair	H17		
1	IO_L49N_1	J16		
1	IO_L49P_1	H16		
1	IO_L48N_1	D15		
1	IO_L48P_1	C15		
1	IO_L47N_1	L17		
1	IO_L47P_1	K16		
1	IO_L46N_1	F15		
1	IO_L46P_1	E15		
1	IO_L45N_1/VREF_1	H15		
1	IO_L45P_1	G15		
1	IO_L44N_1	N17		
1	IO_L44P_1	M17		
1	IO_L43N_1	D14		
1	IO_L43P_1	C14		
1	IO_L39N_1	F14		
1	IO_L39P_1	E14		
1	IO_L38N_1	M16		
1	IO_L38P_1	M15		
1	IO_L37N_1	H14		
1	IO_L37P_1	G14		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
1	IO_L36N_1/VREF_1	E13	NC	
1	IO_L36P_1	D13	NC	
1	IO_L35N_1	K15	NC	
1	IO_L35P_1	J15	NC	
1	IO_L34N_1	G13	NC	
1	IO_L34P_1	F12	NC	
1	IO_L30N_1	J13	NC	
1	IO_L30P_1	H13	NC	
1	IO_L29N_1	L15	NC	
1	IO_L29P_1	L14	NC	
1	IO_L28N_1	E12	NC	
1	IO_L28P_1	D12	NC	
1	IO_L27N_1/VREF_1	J12		
1	IO_L27P_1	H12		
1	IO_L26N_1	K14		
1	IO_L26P_1	J14		
1	IO_L25N_1	D11		
1	IO_L25P_1	C11		
1	IO_L21N_1	F11		
1	IO_L21P_1	E11		
1	IO_L20N_1	M14		
1	IO_L20P_1	M13		
1	IO_L19N_1	H11		
1	IO_L19P_1	G11		
1	IO_L09N_1/VREF_1	J11		
1	IO_L09P_1	J10		
1	IO_L08N_1	L13		
1	IO_L08P_1	L12		
1	IO_L07N_1	D10		
1	IO_L07P_1	C10		
1	IO_L06N_1	F10		
1	IO_L06P_1	E10		
1	IO_L05_1/No_Pair	K10		
1	IO_L03N_1/VREF_1	H10		
1	IO_L03P_1	G10		
1	IO_L02N_1	K12		
1	IO_L02P_1	K11		
1	IO_L01N_1/VRP_1	E9		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
5	IO_L64N_5		AU24		
5	IO_L64P_5		AV24		
5	IO_L60N_5		AR24		
5	IO_L60P_5		AT24		
5	IO_L59N_5		AN24		
5	IO_L59P_5		AP24		
5	IO_L58N_5		AL24		
5	IO_L58P_5		AM24		
5	IO_L57N_5/VREF_5		AY26		
5	IO_L57P_5		AY25		
5	IO_L56N_5		AV25		
5	IO_L56P_5		AV26		
5	IO_L55N_5		AR25		
5	IO_L55P_5		AT25		
5	IO_L54N_5		AM25		
5	IO_L54P_5		AN25		
5	IO_L53_5/No_Pair		AW26		
5	IO_L50_5/No_Pair		AW27		
5	IO_L49N_5		AT26		
5	IO_L49P_5		AU26		
5	IO_L48N_5		AP26		
5	IO_L48P_5		AR26		
5	IO_L47N_5		AN26		
5	IO_L47P_5		AM26		
5	IO_L46N_5		AL26		
5	IO_L46P_5		AL25		
5	IO_L45N_5/VREF_5		AU27		
5	IO_L45P_5		AV27		
5	IO_L44N_5		AT27		
5	IO_L44P_5		AR27		
5	IO_L43N_5		AN27		
5	IO_L43P_5		AP27		
5	IO_L39N_5		AL27		
5	IO_L39P_5		AM27		
5	IO_L38N_5		AY28		
5	IO_L38P_5		AY29		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	RXPPAD21		BB31		
N/A	GNDA21		AY31		
N/A	TXPPAD21		BB32		
N/A	TXNPAD21		BB33		
N/A	VTTXPAD21		BA33		
N/A	AVCCAUXTX21		BA32		
N/A	AVCCAUXRX22		BA34		
N/A	VTRXPAD22		BA35		
N/A	RXNPAD22		BB34		
N/A	RXPPAD22		BB35		
N/A	GNDA22		AY35		
N/A	TXPPAD22		BB36		
N/A	TXNPAD22		BB37		
N/A	VTTXPAD22		BA37		
N/A	AVCCAUXTX22		BA36		
N/A	AVCCAUXRX23		BA38		
N/A	VTRXPAD23		BA39		
N/A	RXNPAD23		BB38		
N/A	RXPPAD23		BB39		
N/A	GNDA23		AY39		
N/A	TXPPAD23		BB40		
N/A	TXNPAD23		BB41		
N/A	VTTXPAD23		BA41		
N/A	AVCCAUXTX23		BA40		
N/A	VCCINT		AB27		
N/A	VCCINT		AB16		
N/A	VCCINT		AC27		
N/A	VCCINT		AC16		
N/A	VCCINT		AD27		
N/A	VCCINT		AD16		
N/A	VCCINT		AE27		
N/A	VCCINT		AE16		
N/A	VCCINT		AF27		
N/A	VCCINT		AF26		
N/A	VCCINT		AF17		