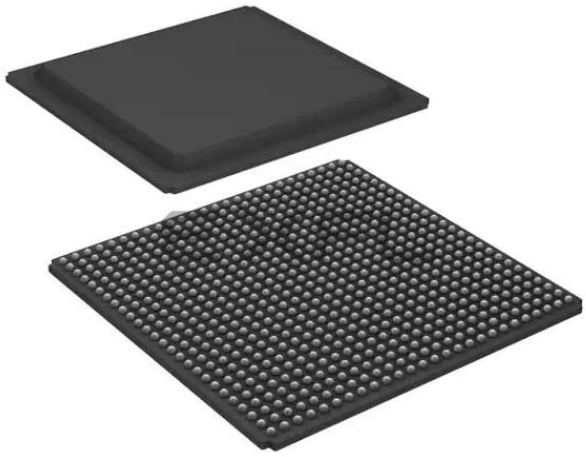

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3424
Number of Logic Elements/Cells	30816
Total RAM Bits	2506752
Number of I/O	416
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp30-5fg676i

ing character, and remembers its location in the buffer. At some point, one transceiver designated as the master instructs all the transceivers to align to the channel bonding character "P" (or to some location relative to the channel bonding character).

After this operation, words transmitted to the FPGA fabric are properly aligned: RRRR, SSSS, TTTT, and so forth, as shown in the bottom-right portion of Figure 7. To ensure that the channels remain properly aligned following the channel bonding operation, the master transceiver must also control the clock correction operations described in the previous section for all channel-bonded transceivers.

Transmitter Buffer

The transmitter's buffer write pointer (TXUSRCLK) is frequency-locked to its read pointer (REFCLK). Therefore, clock correction and channel bonding are not required. The purpose of the transmitter's buffer is to accommodate a phase difference between TXUSRCLK and REFCLK. A simple FIFO suffices for this purpose. A FIFO depth of four will permit reliable operation with simple detection of overflow or underflow, which could occur if the clocks are not frequency-locked.

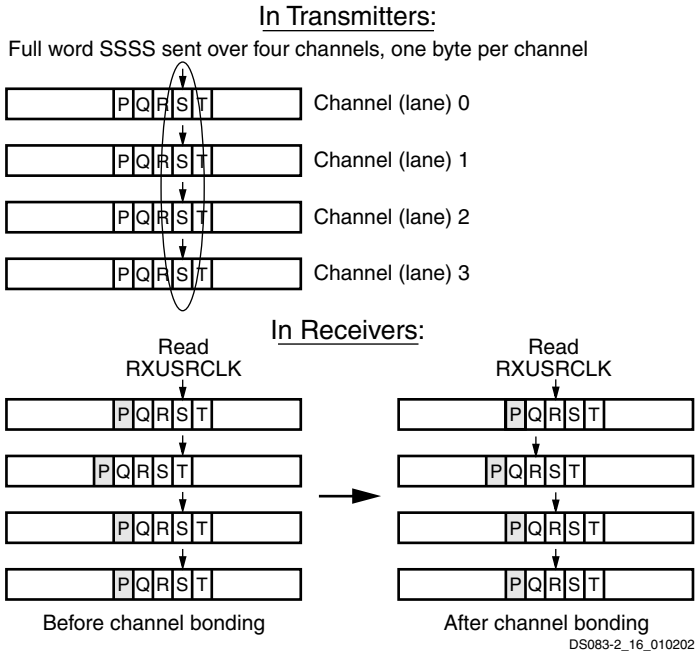


Figure 7: **Channel Bonding (Alignment)**

RocketIO X Configuration

This section outlines functions that can be selected or controlled by configuration. Xilinx implementation software supports the transceiver primitives shown in Table 3.

Table 3: **Supported RocketIO X Transceiver Primitives**

Primitive	Description
GT10_CUSTOM	Fully customizable by user
GT10_OC48_1	SONET OC-48, 1-byte data path
GT10_OC48_2	SONET OC-48, 2-byte data path
GT10_OC48_4	SONET OC-48, 4-byte data path
GT10_PCI_EXPRESS_1	PCI Express, 1-byte data path
GT10_PCI_EXPRESS_2	PCI Express, 2-byte data path
GT10_PCI_EXPRESS_4	PCI Express, 4-byte data path
GT10_INFINIBAND_1	Infiniband, 1-byte data path
GT10_INFINIBAND_2	Infiniband, 2-byte data path
GT10_INFINIBAND_4	Infiniband, 4-byte data path

Serializer

The serializer multiplies the reference frequency provided on REFCLK by 20. The multiplication of the clock is achieved by using an embedded PLL.

Data is converted from parallel to serial format and transmitted on the TXP and TXN differential outputs. The electrical connection of TXP and TXN can be interchanged through configuration. This option can be controlled by an input (TXPOLARITY) at the FPGA transmitter interface.

Deserializer

The serial transceiver input is locked to the input data stream through Clock and Data Recovery (CDR), a built-in feature of the RocketIO transceiver. CDR keys off the rising and falling edges of incoming data and derives a clock that is representative of the incoming data rate.

The derived clock, RXRECCLK, is generated and locked to as long as it remains within the specified component range. This clock is presented to the FPGA fabric at $^1/_{20}$ the incoming data rate.

A sufficient number of transitions must be present in the data stream for CDR to work properly. CDR requires approximately 5,000 transitions upon power-up to guarantee locking to the incoming data rate. Once lock is achieved, up to 75 missing transitions can be tolerated before lock to the incoming data stream is lost. The CDR circuit is guaranteed to work with 8B/10B encoding.

Another feature of CDR is its ability to accept an external precision reference clock, REFCLK, which either acts to clock incoming data or to assist in synchronizing the derived RXRECCLK.

For further clarity, the TXUSRCLK is used to clock data from the FPGA fabric to the TX FIFO. The FIFO depth accounts for the slight phase difference between these two clocks. If the clocks are locked in frequency, then the FIFO acts much like a pass-through buffer.

The receiver can be configured to reverse the RXP and RXN inputs. This can be useful in the event that printed circuit board traces have been reversed.

Receiver Termination

On-chip termination is provided at the receiver, eliminating the need for external termination. The receiver includes programmable on-chip termination circuitry for 50Ω (default) or 75Ω impedance, as shown in Figure 11.

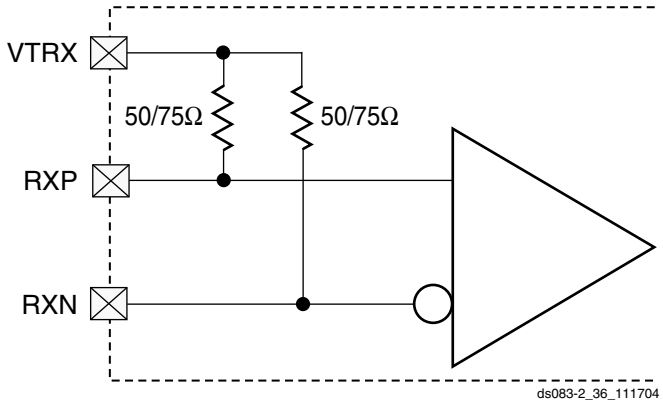


Figure 11: **RocketIO Receive Termination**

PCS

Fabric Data Interface

Internally, the PCS operates in 2-byte mode (16/20 bits). The FPGA fabric interface can either be 1, 2, or 4 bytes wide. When accompanied by the predefined modes of the PMA, the user thus has a large combination of protocols and data rates from which to choose.

USRCLK2 clocks data on the fabric side, while USRCLK clocks data on the PCS side. This creates distinct USRCLK/USRCLK2 frequency ratios for different combinations of fabric and internal data widths. Table 5 summarizes the USRCLK2 to USRCLK ratios for the three fabric data widths.

No fixed phase relationship is assumed between REFCLK, RXRECCLK, and/or any other clock that is not tied to either of these clocks. When RXUSRCLK and RXUSRCLK2 have different frequencies, each edge of the slower clock is aligned to a falling edge of the faster clock. The same relationships apply to TXUSRCLK and TXUSRCLK2.

- Single-cycle and multi-cycle mode option for I-side and D-side interfaces
- Single cycle = one CPU clock cycle; multi-cycle = minimum of two and maximum of eight CPU clock cycles
- FPGA configurable DCR addresses within DSOCM and ISOCM.
- Independent 16 MB logical memory space available within PPC405 memory map for each of the DSOCM and ISOCM. The number of block RAMs in the device might limit the maximum amount of OCM supported.
- Maximum of 64K and 128K bytes addressable from DSOCM and ISOCM interfaces, respectively, using address outputs from OCM directly without additional decoding logic.

Data-Side OCM (DSOCM)

- 32-bit Data Read bus and 32-bit Data Write bus
- Byte write access to DSBRAM support
- Second port of dual port DSBRAM is available to read/write from an FPGA interface
- 22-bit address to DSBRAM port
- 8-bit DCR Registers: DSCNTL, DSARC
- Three alternatives to write into DSBRAM: BRAM initialization, CPU, FPGA H/W using second port

Instruction-Side OCM (ISOCM)

The ISOCM interface contains a 64-bit read only port, for instruction fetches, and a 32-bit write only port, to initialize or test the ISBRAM. When implementing the read only port, the user must deassert the write port inputs. The preferred method of initializing the ISBRAM is through the configuration bitstream.

- 64-bit Data Read Only bus (two instructions per cycle)
- 32-bit Data Write Only bus (through DCR)
- Separate 21-bit address to ISBRAM
- 8-bit DCR Registers: ISCNTL, ISARC
- 32-bit DCR Registers: ISINIT, ISFILL
- Two alternatives to write into ISBRAM: BRAM initialization, DCR and write instruction

Clock/Control Interface Logic

The clock/control interface logic provides proper initialization and connections for PPC405 clock/power management, resets, PLB cycle control, and OCM interfaces. It also couples user signals between the FPGA fabric and the embedded PPC405 CPU core.

The processor clock connectivity is similar to CLB clock pins. It can connect either to global clock nets or general routing resources. Therefore the processor clock source can come from DCM, CLB, or user package pin.

CPU-FPGA Interfaces

All Processor Block user pins link up with the general FPGA routing resources through the CPU-FPGA interface. Therefore processor signals have the same routability as other non-Processor Block user signals. Longlines and hex lines travel across the Processor Block both vertically and horizontally, allowing signals to route through the Processor Block.

Processor Local Bus (PLB) Interfaces

The PPC405 core accesses high-speed system resources through PLB interfaces on the instruction and data cache controllers. The PLB interfaces provide separate 32-bit address/64-bit data buses for the instruction and data sides.

The cache controllers are both PLB masters. PLB arbiters are implemented in the FPGA fabric and are available as soft IP cores.

Device Control Register (DCR) Bus Interface

The device control register (DCR) bus has 10 bits of address space for components external to the PPC405 core. Using the DCR bus to manage status and configuration registers reduces PLB traffic and improves system integrity. System resources on the DCR bus are protected or isolated from wayward code since the DCR bus is not part of the system memory map.

External Interrupt Controller (EIC) Interface

Two level-sensitive user interrupt pins (critical and non-critical) are available. They can be either driven by user defined logic or Xilinx soft interrupt controller IP core outside the Processor Block.

Clock/Power Management (CPM) Interface

The CPM interface supports several methods of clock distribution and power management. Three modes of operation that reduce power consumption below the normal operational level are available.

Reset Interface

There are three user reset input pins (core, chip, and system) and three user reset output pins for different levels of reset, if required.

Debug Interface

Debugging interfaces on the embedded PPC405 core, consisting of the JTAG and Trace ports, offer access to resources internal to the core and assist in software development. The JTAG port provides basic JTAG chip testing functionality as well as the ability for external debug tools to gain control of the processor for debug purposes. The Trace port furnishes programmers with a mechanism for acquiring instruction execution traces.

The JTAG port is compatible with IEEE Std 1149.1, which defines a test access port (TAP) and Boundary-Scan architecture. Extensions to the JTAG interface provide debuggers with processor control that includes stopping, starting, and stepping the PPC405 core. These extensions are compliant with the IEEE 1149.1 specifications for vendor-specific extensions.

Table 15: **SelectIO-Ultra Differential Buffers With On-Chip Termination**

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
LVDS 2.5V	LVDS_25	LVDS_25_DCI
LVDS Extended 2.5V	LVDSEXT_25	LVDSEXT_25_DCI

Figure 28 provides examples illustrating the use of the HSTL_I_DCI, HSTL_II_DCI, HSTL_III_DCI, and HSTL_IV_DCI I/O standards. For a complete list, see the ***Virtex-II Pro Platform FPGA User Guide***.

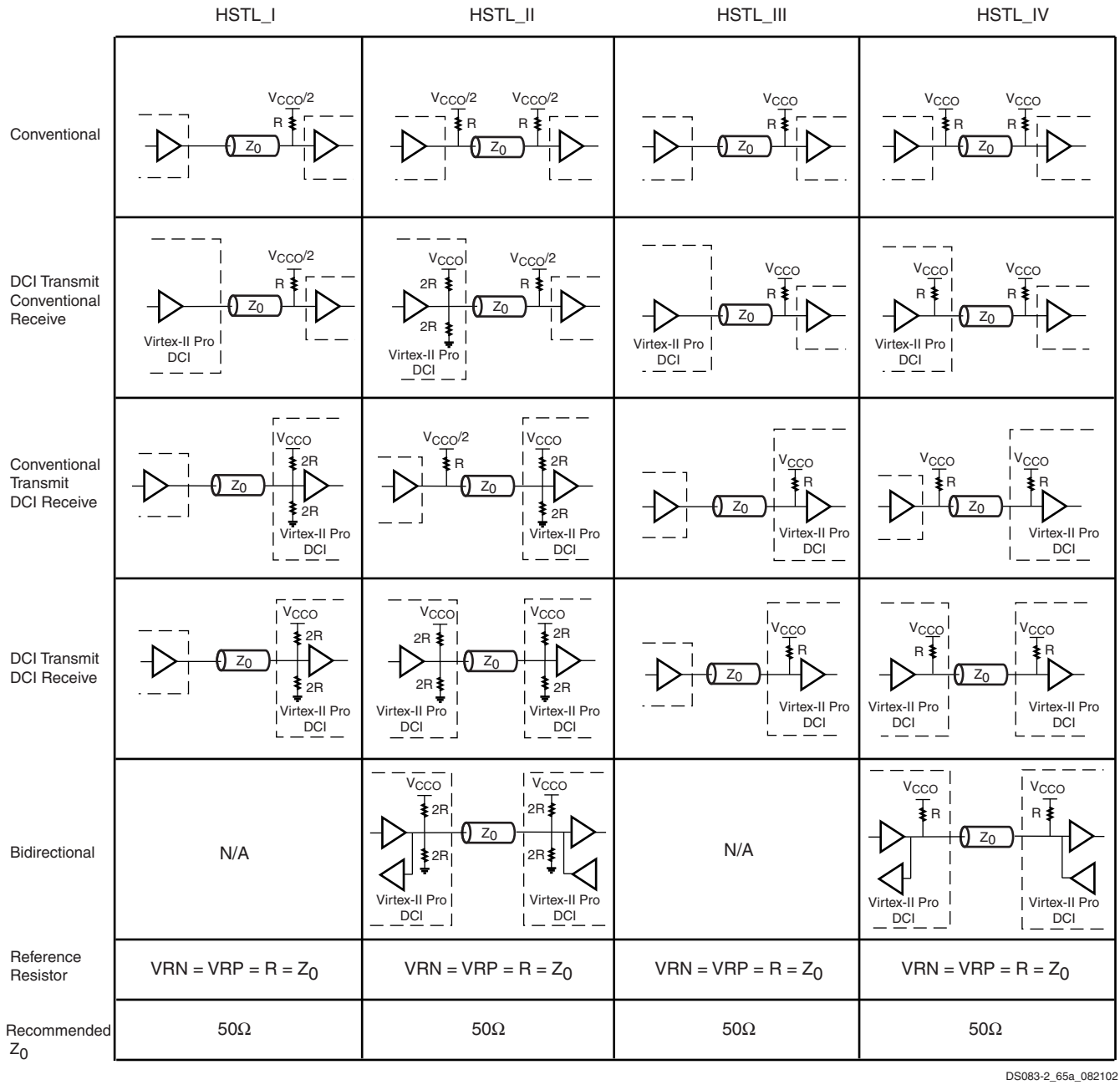


Figure 28: **HSTL DCI Usage Examples**

Table 4: **Quiescent Supply Current**

Symbol	Description	Device	Typ(1)	Max	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC2VP2	20	300	mA
		XC2VP4	30	400	mA
		XC2VP7	35	500	mA
		XC2VP20	40	600	mA
		XC2VPX20	40	600	mA
		XC2VP30	50	800	mA
		XC2VP40	60	1050	mA
		XC2VP50	70	1250	mA
		XC2VP70	85	1700	mA
		XC2VPX70	85	1700	mA
		XC2VP100	100	2200	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC2VP2	1.0	8.0	mA
		XC2VP4	1.0	8.0	mA
		XC2VP7	1.0	8.0	mA
		XC2VP20	1.25	10	mA
		XC2VPX20	1.25	10	mA
		XC2VP30	1.25	10	mA
		XC2VP40	1.25	10	mA
		XC2VP50	1.5	12	mA
		XC2VP70	1.5	12	mA
		XC2VPX70	1.5	12	mA
		XC2VP100	1.75	15	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC2VP2	5	50	mA
		XC2VP4	5	50	mA
		XC2VP7	5	50	mA
		XC2VP20	10	75	mA
		XC2VPX20	10	75	mA
		XC2VP30	10	75	mA
		XC2VP40	10	75	mA
		XC2VP50	20	100	mA
		XC2VP70	20	100	mA
		XC2VPX70	20	100	mA
		XC2VP100	20	125	mA

Notes:
1. Typical values are specified at nominal voltage, 25° C.
2. Quiescent current parameter values are specified for Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.5.
3. With no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
4. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the Power Estimator or XPOWER™.

Table 38: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
HSTL, Class II	HSTL_II	T_{OHSTL_II}	0.30	0.35	0.38	ns
HSTL, Class III	HSTL_III	T_{OHSTL_IIII}	0.31	0.35	0.39	ns
HSTL, Class IV	HSTL_IV	T_{OHSTL_IV}	0.15	0.17	0.19	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{OHSTL\_I\_18}$	0.56	0.64	0.70	ns
HSTL, Class II, 1.8V	HSTL_II_18	$T_{OHSTL\_II\_18}$	0.30	0.35	0.38	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{OHSTL\_IIII\_18}$	0.36	0.41	0.45	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{OHSTL\_IV\_18}$	0.19	0.22	0.24	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{OSSTL18\_I}$	0.80	0.92	1.01	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{OSSTL18\_II}$	0.45	0.51	0.56	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{OSSTL2_I}	0.63	0.72	0.79	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{OSSTL2_II}	0.22	0.25	0.27	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{OLVDCI_33}	0.72	0.83	0.91	ns
LVDCI, 2.5V	LVDCI_25	T_{OLVDCI_25}	0.56	0.64	0.71	ns
LVDCI, 1.8V	LVDCI_18	T_{OLVDCI_18}	0.65	0.75	0.82	ns
LVDCI, 1.5V	LVDCI_15	T_{OLVDCI_15}	1.00	1.15	1.26	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{OLVDCI\_DV2\_25}$	0.06	0.07	0.08	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{OLVDCI\_DV2\_18}$	0.30	0.34	0.38	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{OLVDCI\_DV2\_15}$	0.60	0.69	0.76	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{OHSLVDCI\_15}$	1.00	1.15	1.26	ns
HSLVDCI, 1.8V	HSLVDCI_18	$T_{OHSLVDCI\_18}$	0.65	0.75	0.82	ns
HSLVDCI, 2.5V	HSLVDCI_25	$T_{OHSLVDCI\_25}$	0.56	0.64	0.71	ns
HSLVDCI, 3.3V	HSLVDCI_33	$T_{OHSLVDCI\_33}$	0.72	0.83	0.91	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T_{OGTL_DCI}	1.21	1.39	1.53	ns
GTL Plus with DCI	GTLP_DCI	T_{OGTLP_DCI}	0.05	0.06	0.07	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	$T_{OHSTL\_I\_DCI}$	0.55	0.63	0.69	ns
HSTL, Class II, with DCI	HSTL_II_DCI	$T_{OHSTL\_II\_DCI}$	0.47	0.54	0.60	ns
HSTL, Class III, with DCI	HSTL_III_DCI	$T_{OHSTL\_III\_DCI}$	0.31	0.36	0.40	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	$T_{OHSTL\_IV\_DCI}$	1.81	2.08	2.29	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	$T_{OHSTL\_I\_DCI\_18}$	0.55	0.63	0.70	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	$T_{OHSTL\_II\_DCI\_18}$	0.24	0.28	0.31	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	$T_{OHSTL\_III\_DCI\_18}$	0.35	0.40	0.44	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	$T_{OHSTL\_IV\_DCI\_18}$	1.48	1.70	1.87	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	$T_{OSSTL18\_I\_DCI}$	0.54	0.62	0.68	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	$T_{OSSTL18\_II\_DCI}$	0.24	0.28	0.31	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	$T_{OSSTL2\_I\_DCI}$	0.48	0.56	0.61	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	$T_{OSSTL2\_II\_DCI}$	0.48	0.56	0.61	ns

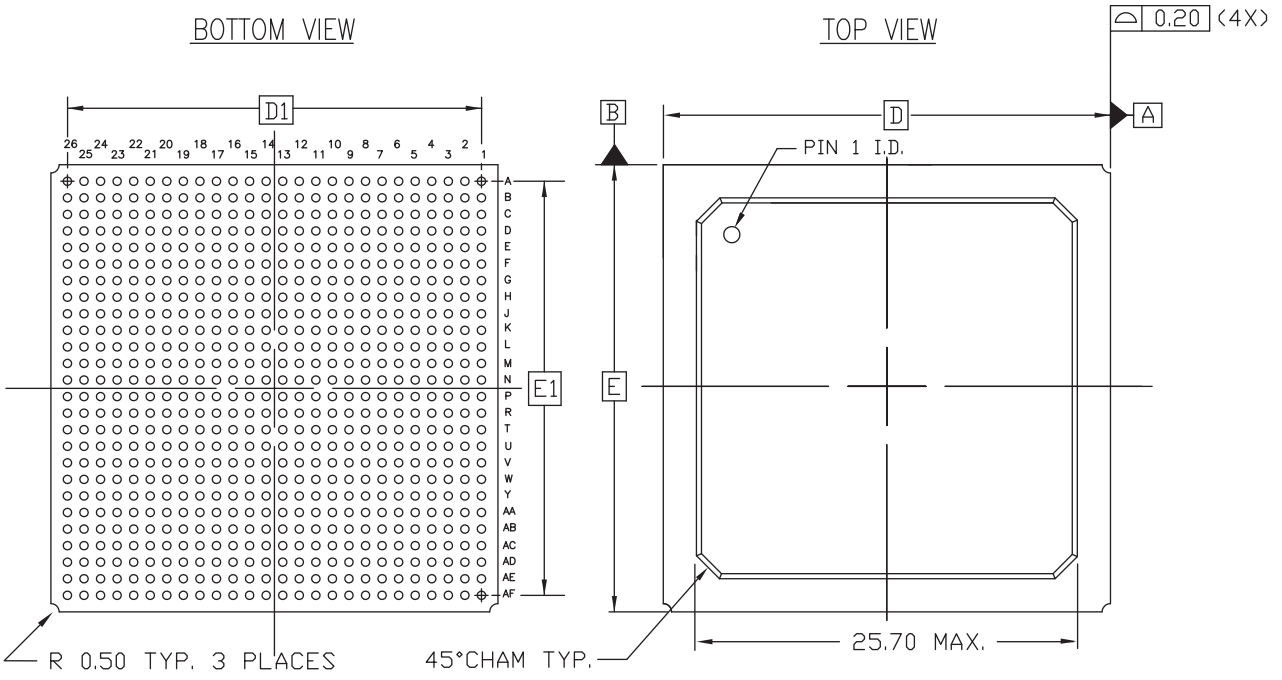
Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

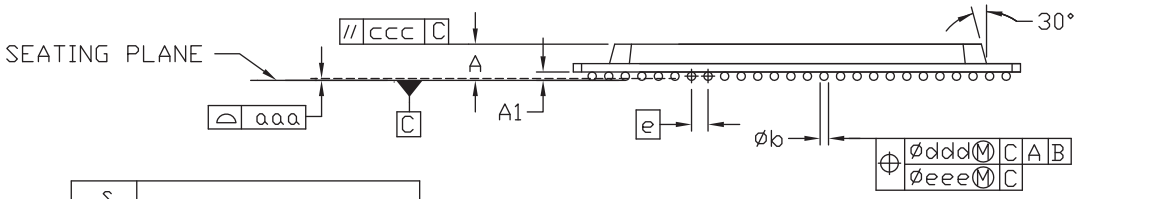
Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
2	IO_L31P_2	F26			
2	IO_L32N_2	G22			
2	IO_L32P_2	H22			
2	IO_L34N_2/VREF_2	G23			
2	IO_L34P_2	G24			
2	IO_L36N_2	G25			
2	IO_L36P_2	G26			
2	IO_L37N_2	H20			
2	IO_L37P_2	H21			
2	IO_L38N_2	H25			
2	IO_L38P_2	H26			
2	IO_L40N_2/VREF_2	J19			
2	IO_L40P_2	J20			
2	IO_L42N_2	J21			
2	IO_L42P_2	J22			
2	IO_L43N_2	J23			
2	IO_L43P_2	J24			
2	IO_L44N_2	J25			
2	IO_L44P_2	J26			
2	IO_L46N_2/VREF_2	K19			
2	IO_L46P_2	L19			
2	IO_L48N_2	K22			
2	IO_L48P_2	K23			
2	IO_L49N_2	K24			
2	IO_L49P_2	L24			
2	IO_L50N_2	K25			
2	IO_L50P_2	K26			
2	IO_L52N_2/VREF_2	L20			
2	IO_L52P_2	M20			
2	IO_L54N_2	L21			
2	IO_L54P_2	L22			
2	IO_L55N_2	L25			
2	IO_L55P_2	L26			
2	IO_L56N_2	M18			
2	IO_L56P_2	M19			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
2	IO_L58N_2/VREF_2	M21			
2	IO_L58P_2	N21			
2	IO_L60N_2	M22			
2	IO_L60P_2	M23			
2	IO_L85N_2	M25			
2	IO_L85P_2	M26			
2	IO_L86N_2	N18			
2	IO_L86P_2	N19			
2	IO_L88N_2/VREF_2	N22			
2	IO_L88P_2	N23			
2	IO_L90N_2	N24			
2	IO_L90P_2	N25			
3	IO_L90N_3	P25			
3	IO_L90P_3	P24			
3	IO_L89N_3	P23			
3	IO_L89P_3	P22			
3	IO_L87N_3/VREF_3	P19			
3	IO_L87P_3	P18			
3	IO_L85N_3	R26			
3	IO_L85P_3	R25			
3	IO_L60N_3	R23			
3	IO_L60P_3	R22			
3	IO_L59N_3	P21			
3	IO_L59P_3	R21			
3	IO_L57N_3/VREF_3	R19			
3	IO_L57P_3	R18			
3	IO_L55N_3	T26			
3	IO_L55P_3	T25			
3	IO_L54N_3	T22			
3	IO_L54P_3	T21			
3	IO_L53N_3	R20			
3	IO_L53P_3	T20			
3	IO_L51N_3/VREF_3	U26			
3	IO_L51P_3	U25			

FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)





FG676 - 63/37 (Sn/Pb) Solder Balls
FGG676 - Sn/Ag/Cu Solder Balls

SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.02	2.23	2.44
A_1	0.40	0.50	0.60
D/E	27.00 BSC		
D_1/E_1	25.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa	~	~	0.20
ccc	~	~	0.35
ddd	~	~	0.30
eee	~	~	0.10
M	26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

ds083_4_03_053111

Figure 3: **FG676/FGG676 Fine-Pitch BGA Package Specifications**

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
6	IO_L01P_6/VRN_6	AF24			
6	IO_L01N_6/VRP_6	AE24			
6	IO_L02P_6	AD23			
6	IO_L02N_6	AC24			
6	IO_L03P_6	AE26			
6	IO_L03N_6/VREF_6	AF25			
6	IO_L04P_6	AD25			
6	IO_L04N_6	AD26			
6	IO_L05P_6	AC25			
6	IO_L05N_6	AC26			
6	IO_L06P_6	AB23			
6	IO_L06N_6	AB24			
6	IO_L39P_6	AB25	NC	NC	NC
6	IO_L39N_6/VREF_6	AB26	NC	NC	NC
6	IO_L41P_6	AA22	NC	NC	NC
6	IO_L41N_6	AA23	NC	NC	NC
6	IO_L42P_6	AA24	NC	NC	NC
6	IO_L42N_6	AA25	NC	NC	NC
6	IO_L43P_6	Y21	NC		
6	IO_L43N_6	Y22	NC		
6	IO_L44P_6	Y23	NC		
6	IO_L44N_6	Y24	NC		
6	IO_L45P_6	AA26	NC		
6	IO_L45N_6/VREF_6	Y26	NC		
6	IO_L46P_6	W21	NC		
6	IO_L46N_6	W22	NC		
6	IO_L47P_6	W23	NC		
6	IO_L47N_6	W24	NC		
6	IO_L48P_6	W25	NC		
6	IO_L48N_6	W26	NC		
6	IO_L49P_6	V20	NC		
6	IO_L49N_6	V21	NC		
6	IO_L50P_6	V22	NC		
6	IO_L50N_6	V23	NC		
6	IO_L51P_6	V24	NC		
6	IO_L51N_6/VREF_6	V25	NC		
6	IO_L52P_6	U21	NC		

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
0	IO_L43P_0	E22				
0	IO_L44N_0	E25				
0	IO_L44P_0	D25				
0	IO_L45N_0	H21				
0	IO_L45P_0/VREF_0	G21				
0	IO_L46N_0	D22				
0	IO_L46P_0	D23				
0	IO_L47N_0	D24				
0	IO_L47P_0	C24				
0	IO_L48N_0	K20				
0	IO_L48P_0	J20				
0	IO_L49N_0	F21				
0	IO_L49P_0	E21				
0	IO_L50_0/No_Pair	C21				
0	IO_L53_0/No_Pair	C22				
0	IO_L54N_0	L19				
0	IO_L54P_0	K19				
0	IO_L55N_0	G20				
0	IO_L55P_0	F20				
0	IO_L56N_0	D21				
0	IO_L56P_0	D20				
0	IO_L57N_0	J19				
0	IO_L57P_0/VREF_0	H19				
0	IO_L67N_0	G19				
0	IO_L67P_0	F19				
0	IO_L68N_0	E19				
0	IO_L68P_0	D19				
0	IO_L69N_0	L18				
0	IO_L69P_0/VREF_0	K18				
0	IO_L73N_0	G18				
0	IO_L73P_0	F18				
0	IO_L74N_0/GCLK7P	E18				
0	IO_L74P_0/GCLK6S	D18				
0	IO_L75N_0/GCLK5P	J18				
0	IO_L75P_0/GCLK4S	H18				
1	IO_L75N_1/GCLK3P	H17				
1	IO_L75P_1/GCLK2S	J17				

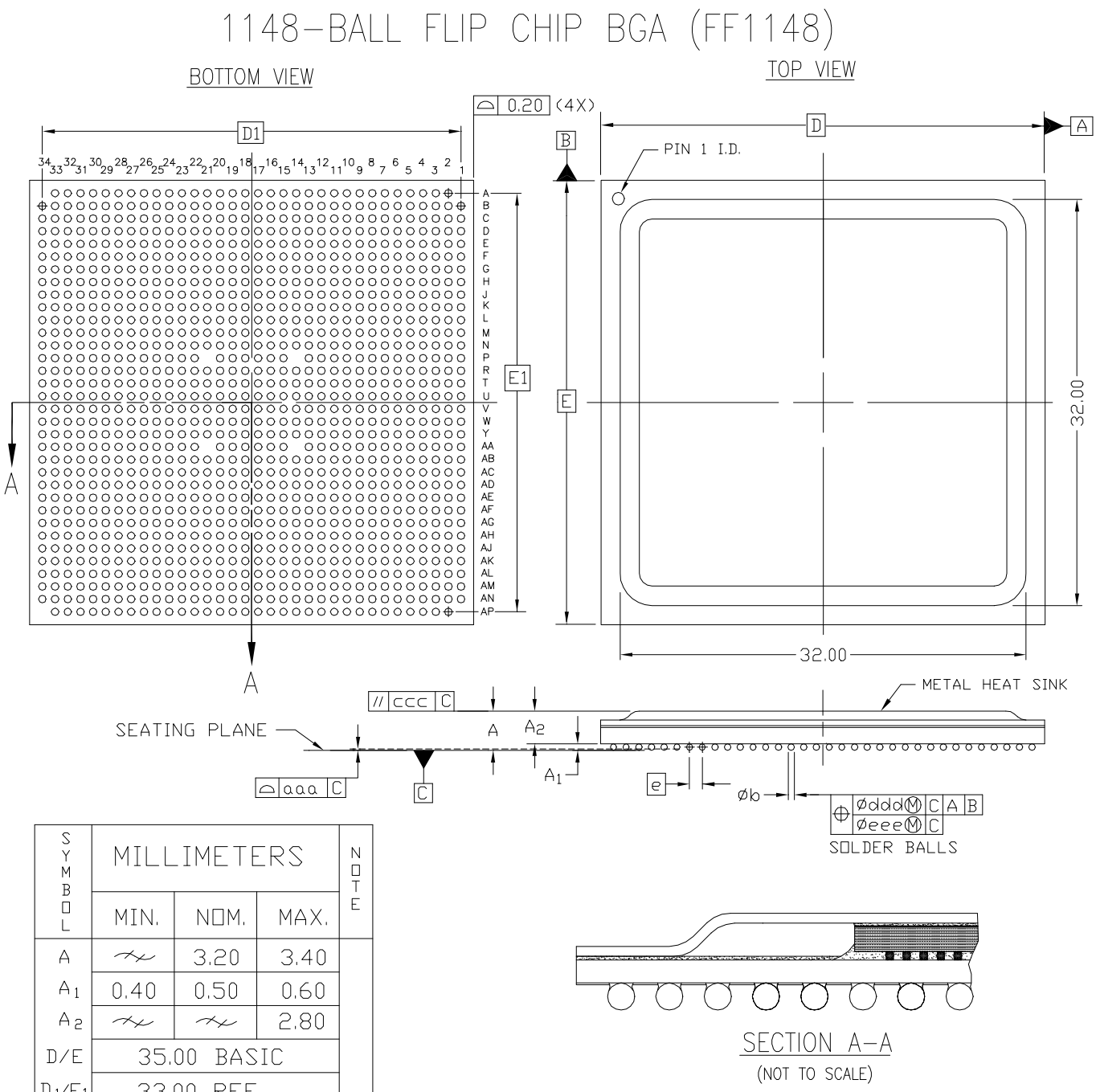
Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
6	IO_L53P_6	W25				
6	IO_L53N_6	W26				
6	IO_L54P_6	AB33				
6	IO_L54N_6	AA33				
6	IO_L55P_6	Y28				
6	IO_L55N_6	Y29				
6	IO_L56P_6	W27				
6	IO_L56N_6	W28				
6	IO_L57P_6	Y31				
6	IO_L57N_6/VREF_6	Y32				
6	IO_L58P_6	W29				
6	IO_L58N_6	W30				
6	IO_L59P_6	W24				
6	IO_L59N_6	V24				
6	IO_L60P_6	AA34				
6	IO_L60N_6	Y34				
6	IO_L85P_6	W31				
6	IO_L85N_6	W32				
6	IO_L86P_6	V25				
6	IO_L86N_6	V26				
6	IO_L87P_6	Y33				
6	IO_L87N_6/VREF_6	W33				
6	IO_L88P_6	V29				
6	IO_L88N_6	V30				
6	IO_L89P_6	V27				
6	IO_L89N_6	V28				
6	IO_L90P_6	V31				
6	IO_L90N_6	V32				
7	IO_L90P_7	U32				
7	IO_L90N_7	U31				
7	IO_L89P_7	U28				
7	IO_L89N_7	U27				
7	IO_L88P_7	V33				
7	IO_L88N_7/VREF_7	U33				
7	IO_L87P_7	U30				
7	IO_L87N_7	U29				
7	IO_L86P_7	U26				

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
1	IO_L75N_1/GCLK3P	C17		
1	IO_L75P_1/GCLK2S	B17		
1	IO_L74N_1/GCLK1P	L17		
1	IO_L74P_1/GCLK0S	K17		
1	IO_L73N_1	E17		
1	IO_L73P_1	D17		
1	IO_L69N_1/VREF_1	G17		
1	IO_L69P_1	F17		
1	IO_L68N_1	J17		
1	IO_L68P_1	H17		
1	IO_L67N_1	C16		
1	IO_L67P_1	B16		
1	IO_L66N_1/VREF_1	G16	NC	
1	IO_L66P_1	F16	NC	
1	IO_L57N_1/VREF_1	B15		
1	IO_L57P_1	A15		
1	IO_L56N_1	L16		
1	IO_L56P_1	K16		
1	IO_L55N_1	D16		
1	IO_L55P_1	C15		
1	IO_L54N_1	F15		
1	IO_L54P_1	E15		
1	IO_L53_1/No_Pair	H16		
1	IO_L50_1/No_Pair	G15		
1	IO_L49N_1	B14		
1	IO_L49P_1	A14		
1	IO_L48N_1	D14		
1	IO_L48P_1	C14		
1	IO_L47N_1	L15		
1	IO_L47P_1	K15		
1	IO_L46N_1	F14		
1	IO_L46P_1	E14		
1	IO_L45N_1/VREF_1	H14		
1	IO_L45P_1	G14		
1	IO_L44N_1	L14		
1	IO_L44P_1	K14		
1	IO_L43N_1	C13		

FF1148 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	---	3.20	3.40	
A_1	0.40	0.50	0.60	
A_2	---	---	2.80	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	---	---	0.20	
ccc	---	---	0.35	
ddd	---	---	0.30	
eee	---	---	0.10	
M	34			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAR-1 (DEPOPULATED)

Figure 7: **FF1148 Flip-Chip Fine-Pitch BGA Package Specifications**

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	IO_L35N_3		AH11		
3	IO_L35P_3		AH12		
3	IO_L34N_3		AH5		
3	IO_L34P_3		AH6		
3	IO_L33N_3/VREF_3		AH9		
3	IO_L33P_3		AH10		
3	IO_L32N_3		AJ11		
3	IO_L32P_3		AJ12		
3	IO_L31N_3		AJ1		
3	IO_L31P_3		AJ2		
3	IO_L30N_3		AJ5		
3	IO_L30P_3		AJ6		
3	IO_L29N_3		AJ9		
3	IO_L29P_3		AJ10		
3	IO_L28N_3		AJ7		
3	IO_L28P_3		AJ8		
3	IO_L27N_3/VREF_3		AK1		
3	IO_L27P_3		AK2		
3	IO_L26N_3		AK11		
3	IO_L26P_3		AK12		
3	IO_L25N_3		AK3		
3	IO_L25P_3		AK4		
3	IO_L24N_3		AK5		
3	IO_L24P_3		AK6		
3	IO_L23N_3		AK9		
3	IO_L23P_3		AK10		
3	IO_L22N_3		AK7		
3	IO_L22P_3		AK8		
3	IO_L21N_3/VREF_3		AL2		
3	IO_L21P_3		AL3		
3	IO_L20N_3		AL11		
3	IO_L20P_3		AL12		
3	IO_L19N_3		AL4		
3	IO_L19P_3		AL5		
3	IO_L18N_3		AL7		
3	IO_L18P_3		AL8		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
3	VCCO_3		AD14		
3	VCCO_3		AC15		
3	VCCO_3		AC14		
3	VCCO_3		AC8		
3	VCCO_3		AC5		
3	VCCO_3		AB15		
3	VCCO_3		AB14		
4	VCCO_4		AW18		
4	VCCO_4		AT20		
4	VCCO_4		AT15		
4	VCCO_4		AT11		
4	VCCO_4		AP18		
4	VCCO_4		AP14		
4	VCCO_4		AJ21		
4	VCCO_4		AJ20		
4	VCCO_4		AJ19		
4	VCCO_4		AJ18		
4	VCCO_4		AJ17		
4	VCCO_4		AH21		
4	VCCO_4		AH20		
4	VCCO_4		AH19		
4	VCCO_4		AH18		
5	VCCO_5		AW25		
5	VCCO_5		AT32		
5	VCCO_5		AT28		
5	VCCO_5		AT23		
5	VCCO_5		AP29		
5	VCCO_5		AP25		
5	VCCO_5		AJ26		
5	VCCO_5		AJ25		
5	VCCO_5		AJ24		
5	VCCO_5		AJ23		
5	VCCO_5		AJ22		
5	VCCO_5		AH25		
5	VCCO_5		AH24		
5	VCCO_5		AH23		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	TXPPAD3		A36		
N/A	GNDA3		C35		
N/A	RXPPAD3		A35		
N/A	RXNPAD3		A34		
N/A	VTRXPAD3		B35		
N/A	AVCCAUXRX3		B34		
N/A	AVCCAUXTX4		B32		
N/A	VTTXPAD4		B33		
N/A	TXNPAD4		A33		
N/A	TXPPAD4		A32		
N/A	GNDA4		C31		
N/A	RXPPAD4		A31		
N/A	RXNPAD4		A30		
N/A	VTRXPAD4		B31		
N/A	AVCCAUXRX4		B30		
N/A	AVCCAUXTX5		B28		
N/A	VTTXPAD5		B29		
N/A	TXNPAD5		A29		
N/A	TXPPAD5		A28		
N/A	GNDA5		C27		
N/A	RXPPAD5		A27		
N/A	RXNPAD5		A26		
N/A	VTRXPAD5		B27		
N/A	AVCCAUXRX5		B26		
N/A	AVCCAUXTX6		B24		
N/A	VTTXPAD6		B25		
N/A	TXNPAD6		A25		
N/A	TXPPAD6		A24		
N/A	GNDA6		C22		
N/A	RXPPAD6		A23		
N/A	RXNPAD6		A22		
N/A	VTRXPAD6		B23		
N/A	AVCCAUXRX6		B22		
N/A	AVCCAUXTX7		B20		
N/A	VTTXPAD7		B21		
N/A	TXNPAD7		A21		

FF1696 Flip-Chip Fine-Pitch BGA Package

As shown in Table 14, XC2VP100 Virtex-II Pro devices are available in the FF1696 flip-chip fine-pitch BGA package. Following this table are the FF1696 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
0	IO_L01N_0/VRP_0	E33	
0	IO_L01P_0/VRN_0	F33	
0	IO_L02N_0	K32	
0	IO_L02P_0	L32	
0	IO_L03N_0	C32	
0	IO_L03P_0/VREF_0	C33	
0	IO_L05_0/No_Pair	G33	
0	IO_L06N_0	A33	
0	IO_L06P_0	B33	
0	IO_L07N_0	F32	
0	IO_L07P_0	G32	
0	IO_L08N_0	H32	
0	IO_L08P_0	J32	
0	IO_L09N_0	D32	
0	IO_L09P_0/VREF_0	E32	
0	IO_L19N_0	A32	
0	IO_L19P_0	B32	
0	IO_L20N_0	K31	
0	IO_L20P_0	L31	
0	IO_L21N_0	H30	
0	IO_L21P_0	G31	
0	IO_L25N_0	E31	
0	IO_L25P_0	F31	
0	IO_L26N_0	H31	
0	IO_L26P_0	J31	
0	IO_L27N_0	D30	
0	IO_L27P_0/VREF_0	D31	
0	IO_L28N_0	B31	
0	IO_L28P_0	C31	
0	IO_L29N_0	K30	
0	IO_L29P_0	L30	
0	IO_L30N_0	F30	
0	IO_L30P_0	G30	
0	IO_L34N_0	B30	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
3	IO_L67P_3	AU5	
3	IO_L66N_3	AU1	
3	IO_L66P_3	AU2	
3	IO_L65N_3	AJ9	
3	IO_L65P_3	AK8	
3	IO_L64N_3	AU8	
3	IO_L64P_3	AV8	
3	IO_L63N_3/VREF_3	AU7	
3	IO_L63P_3	AV7	
3	IO_L62N_3	AL8	
3	IO_L62P_3	AL9	
3	IO_L61N_3	AU3	
3	IO_L61P_3	AV2	
3	IO_L84N_3	AV6	
3	IO_L84P_3	AW5	
3	IO_L83N_3	AM8	
3	IO_L83P_3	AM9	
3	IO_L82N_3	AV4	
3	IO_L82P_3	AW4	
3	IO_L81N_3/VREF_3	AV3	
3	IO_L81P_3	AW3	
3	IO_L80N_3	AN9	
3	IO_L80P_3	AP8	
3	IO_L79N_3	AW1	
3	IO_L79P_3	AW2	
3	IO_L78N_3	AY7	
3	IO_L78P_3	AY8	
3	IO_L77N_3	AR8	
3	IO_L77P_3	AR9	
3	IO_L76N_3	AW7	
3	IO_L76P_3	AY6	
3	IO_L75N_3/VREF_3	AY3	
3	IO_L75P_3	AY4	
3	IO_L74N_3	AT9	
3	IO_L74P_3	AU9	
3	IO_L73N_3	AY5	
3	IO_L73P_3	BA5	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L45N_7	T36	
7	IO_L44P_7	W32	
7	IO_L44N_7	W33	
7	IO_L43P_7	R41	
7	IO_L43N_7	R42	
7	IO_L42P_7	P40	
7	IO_L42N_7	R40	
7	IO_L41P_7	V36	
7	IO_L41N_7	V37	
7	IO_L40P_7	R38	
7	IO_L40N_7/VREF_7	R39	
7	IO_L39P_7	P38	
7	IO_L39N_7	R37	
7	IO_L38P_7	V34	
7	IO_L38N_7	V35	
7	IO_L37P_7	P41	
7	IO_L37N_7	P42	
7	IO_L36P_7	P36	
7	IO_L36N_7	P37	
7	IO_L35P_7	V32	
7	IO_L35N_7	V33	
7	IO_L34P_7	M41	
7	IO_L34N_7/VREF_7	N41	
7	IO_L33P_7	N39	
7	IO_L33N_7	N40	
7	IO_L32P_7	U35	
7	IO_L32N_7	U36	
7	IO_L31P_7	N36	
7	IO_L31N_7	N37	
7	IO_L30P_7	M39	
7	IO_L30N_7	M40	
7	IO_L29P_7	U32	
7	IO_L29N_7	U33	
7	IO_L28P_7	M37	
7	IO_L28N_7/VREF_7	M38	
7	IO_L27P_7	L37	
7	IO_L27N_7	M36	