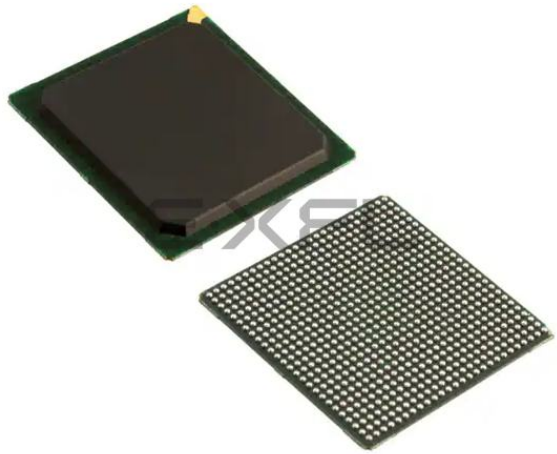

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 3424 |
| Number of Logic Elements/Cells | 30816 |
| Total RAM Bits | 2506752 |
| Number of I/O | 416 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 676-BGA |
| Supplier Device Package | 676-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2vp30-5fgg676c |

## Configurable Logic Blocks (CLBs)

The Virtex-II Pro configurable logic blocks (CLB) are organized in an array and are used to build combinatorial and synchronous logic designs. Each CLB element is tied to a switch matrix to access the general routing matrix, as shown in Figure 32. A CLB element comprises 4 similar slices, with fast local feedback within the CLB. The four slices are split in two columns of two slices with two independent carry logic chains and one common shift chain.

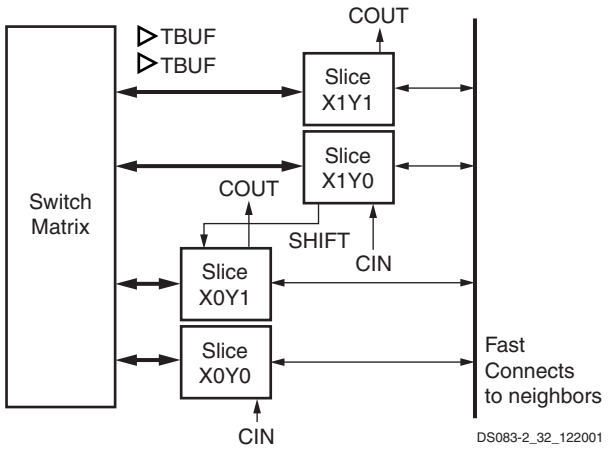



*Figure 32:* **Virtex-II Pro CLB Element**

### Slice Description

Each slice includes two 4-input function generators, carry logic, arithmetic logic gates, wide function multiplexers and two storage elements. As shown in Figure 33, each 4-input function generator is programmable as a 4-input LUT, 16 bits of distributed SelectRAM+ memory, or a 16-bit variable-tap shift register element.

The output from the function generator in each slice drives both the slice output and the D input of the storage element. Figure 34 shows a more detailed view of a single slice.

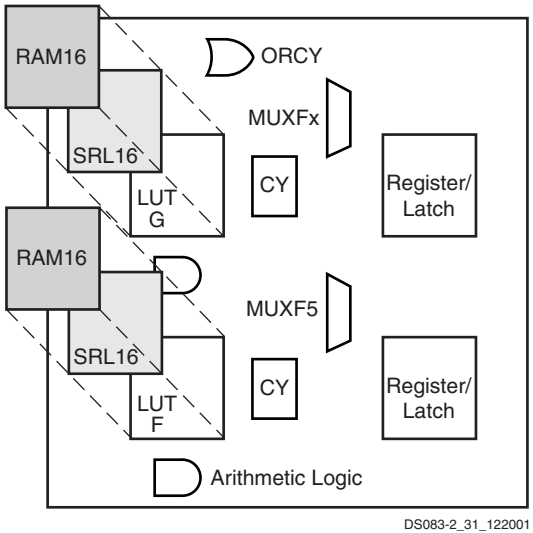



*Figure 33:* **Virtex-II Pro Slice Configuration**

### Configurations

#### Look-Up Table

Virtex-II Pro function generators are implemented as 4-input look-up tables (LUTs). Four independent inputs are provided to each of the two function generators in a slice (F and G). These function generators are each capable of implementing any arbitrarily defined boolean function of four inputs. The propagation delay is therefore independent of the function implemented. Signals from the function generators can exit the slice (X or Y output), can input the XOR dedicated gate (see arithmetic logic), or input the carry-logic multiplexer (see fast look-ahead carry logic), or feed the D input of the storage element, or go to the MUXF5 (not shown in Figure 34).

In addition to the basic LUTs, the Virtex-II Pro slice contains logic (MUXF5 and MUXFX multiplexers) that combines function generators to provide any function of five, six, seven, or eight inputs. The MUXFX is either MUXF6, MUXF7, or MUXF8 according to the slice considered in the CLB. Selected functions up to nine inputs (MUXF5 multiplexer) can be implemented in one slice. The MUXFX can also be a MUXF6, MUXF7, or MUXF8 multiplexer to map any function of six, seven, or eight inputs and selected wide logic functions.

#### Register/Latch

The storage elements in a Virtex-II Pro slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D input can be directly driven by the X or Y output via the DX or DY input, or by the slice inputs bypassing the function generators via the BX or BY input. The clock enable signal (CE) is active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

In addition to clock (CK) and clock enable (CE) signals, each slice has set and reset signals (SR and BY slice inputs). SR forces the storage element into the state specified by the attribute SRHIGH or SRLOW. SRHIGH forces a logic 1 when SR is asserted. SRLOW forces a logic 0. When SR is used, an optional second input (BY) forces the storage element into the opposite state via the REV pin. The reset condition is predominant over the set condition. (See Figure 35.)

The initial state after configuration or global initial state is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1. For each slice, set and reset can be set to be synchronous or asynchronous. Virtex-II Pro devices also have the ability to set INIT0 and INIT1 independent of SRHIGH and SRLOW.

The control signals clock (CLK), clock enable (CE) and set/reset (SR) are common to both storage elements in one slice. All of the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

### Sum of Products

Each Virtex-II Pro slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice, as shown in Figure 43.

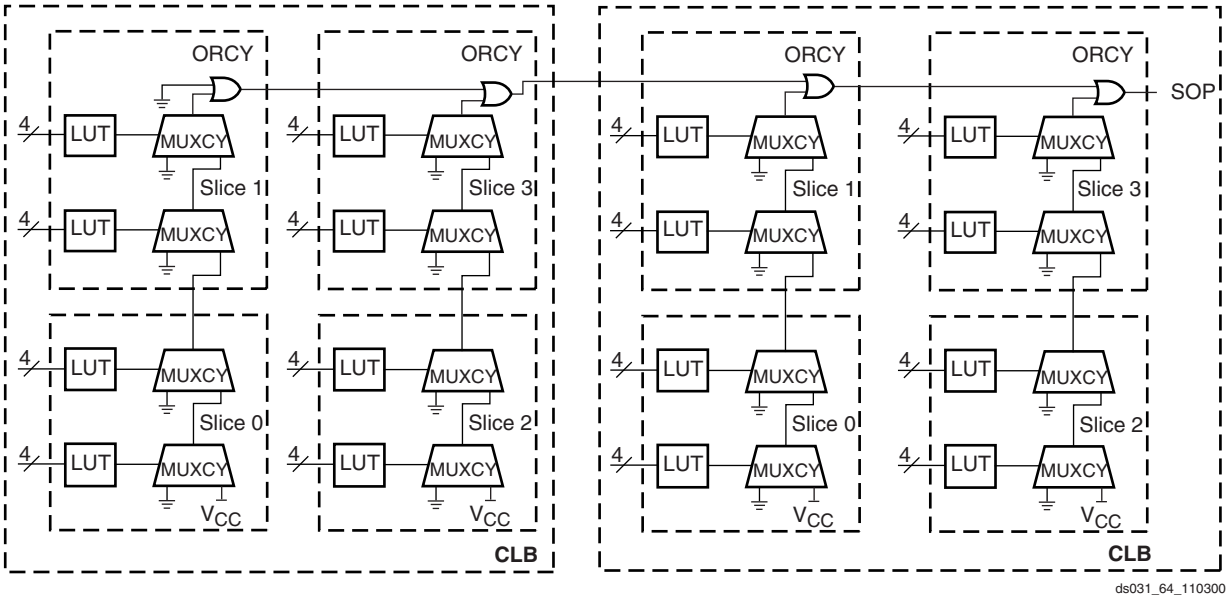



*Figure 43:* **Horizontal Cascade Chain**

LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 44 illustrates LUT and MUXCY resources configured as a 16-input AND gate.

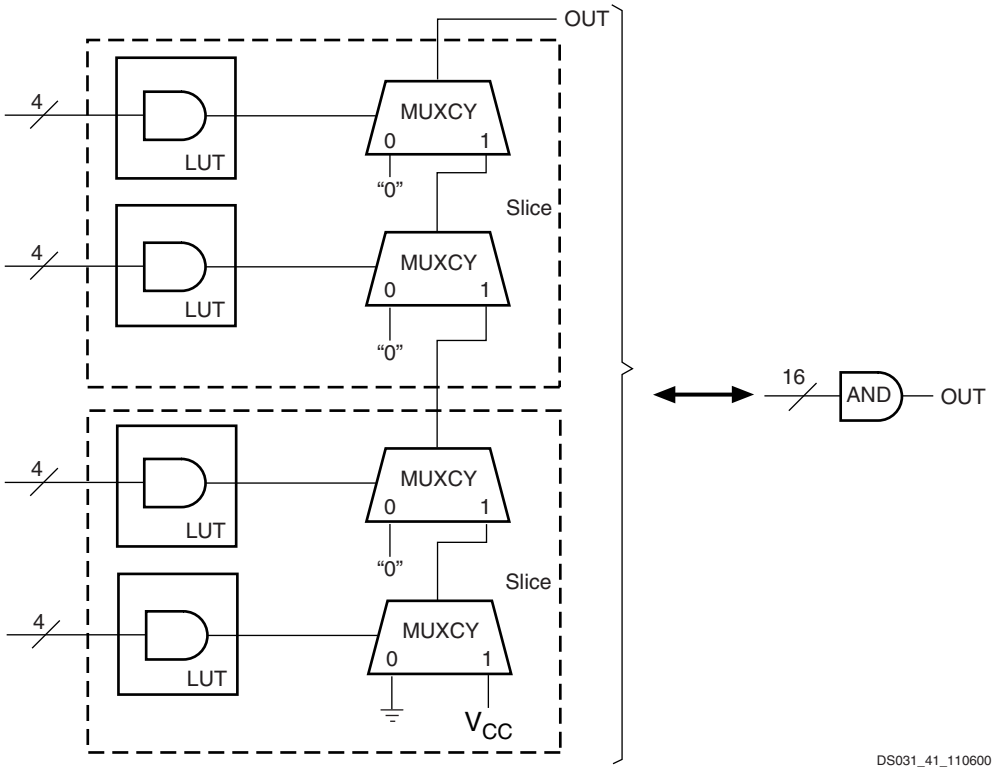



*Figure 44:* **Wide-Input AND Gate (16 Inputs)**

# Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics

DS083 (v5.0) June 21, 2011 **Product Specification**

## Virtex-II Pro[1] Electrical Characteristics

Virtex™-II Pro devices are provided in -7, -6, and -5 speed grades, with -7 having the highest performance.

Virtex-II Pro DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -6 speed grade industrial device are the same as for a -6 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

### Virtex-II Pro DC Characteristics

*Table 1:* **Absolute Maximum Ratings**

| Symbol | Description[1] | | Virtex-II Pro X | Virtex-II Pro | Units |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND | | –0.5 to 1.6 | | V |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | | –0.5 to 3.0 | | V |
| $V_{CCO}$ | Output drivers supply voltage relative to GND | | –0.5 to 3.75 | | V |
| $V_{BATT}$ | Key memory battery backup supply | | –0.5 to 4.05 | | V |
| $V_{REF}$ | Input reference voltage | | –0.3 to 3.75 | | V |
| $V_{IN}$ | 3.3V I/O input voltage relative to GND (user and dedicated I/Os) | | –0.3 to 4.05[3] | | V |
| | 2.5V or below I/O input voltage relative to GND (user and dedicated I/Os) | | –0.5 to $V_{CCO}$ + 0.5 | | V |
| $V_{TS}$ | Voltage applied to 3-state 3.3V output (user and dedicated I/Os) | | –0.3 to 4.05[3] | | V |
| | Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os) | | –0.5 to $V_{CCO}$ + 0.5 | | V |
| AVCCAUXRX | Receive auxilliary supply voltage relative to GNDA (analog ground) | | –0.5 to 2.0 | –0.5 to 3.0 | V |
| AVCCAUXTX | Transmit auxilliary supply voltage relative to GNDA (analog ground) | | –0.5 to 3.0 | –0.5 to 3.0 | V |
| $V_{TRX}$ | Terminal receive supply voltage relative to GND | | –0.5 to 3.0 | –0.5 to 3.0 | V |
| $V_{TTX}$ | Terminal transmit supply voltage relative to GND | | –0.5 to 1.6 | –0.5 to 3.0 | V |
| $T_{STG}$ | Storage temperature (ambient) | | –65 to +150 | | °C |
| $T_{SOL}$ | Maximum soldering temperature[2] | All regular FG/FF flip-chip packages | +220 | | °C |
| | | Pb-free FGG256 wire-bond package | N/A | +260 | °C |
| | | Pb-free FGG456 and FGG676 wire-bond packages | N/A | +250 | °C |
| $T_J$ | Maximum junction temperature[2] | | +125 | | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see the **Device Packaging and Thermal Characteristics Guide** information on the Xilinx website.
3. 3.3V I/O Absolute Maximum limit applied to DC and AC signals. Refer to **XAPP659** for more details.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

*Table 17:* **Processor Block Switching Characteristics**

| | | Speed Grade | | | |
|---|---|---|---|---|---|
| **Description** | **Symbol** | **-7** | **-6** | **-5** | **Units** |
| **Setup and Hold Relative to Clock (CPMC405CLOCK)** | | | | | |
| Device Control Register Bus control inputs | $T_{PCCK\_}DCR/T_{PCKC\_}DCR$ | 0.38/–0.18 | 0.44/–0.20 | 0.48/–0.23 | ns, min |
| Device Control Register Bus data inputs | $T_{PDCK\_}DCR/T_{PCKD\_}DCR$ | 0.65/–0.01 | 0.75/–0.01 | 0.82/–0.02 | ns, min |
| Clock and Power Management control inputs | $T_{PCCK\_}CPM/T_{PCKC\_}CPM$ | 0.16/ 0.03 | 0.19/ 0.03 | 0.20/ 0.03 | ns, min |
| Reset control inputs | $T_{PCCK\_}RST/T_{PCKC\_}RST$ | 0.16/ 0.03 | 0.19/ 0.03 | 0.20/ 0.03 | ns, min |
| Debug control inputs | $T_{PCCK\_}DBG/T_{PCKC\_}DBG$ | 0.27/ 0.30 | 0.31/ 0.35 | 0.34/ 0.38 | ns, min |
| Trace control inputs | $T_{PCCK\_}TRC/T_{PCKC\_}TRC$ | 1.37/–0.41 | 1.57/–0.48 | 1.73/–0.52 | ns, min |
| External Interrupt Controller control inputs | $T_{PCCK\_}EIC/T_{PCKC\_}EIC$ | 0.57/–0.22 | 0.66/–0.25 | 0.72/–0.27 | ns, min |
| **Clock to Out** | | | | | |
| Device Control Register Bus control outputs | $T_{PCKCO\_}DCR$ | 1.32 | 1.52 | 1.67 | ns, max |
| Device Control Register Bus address outputs | $T_{PCKAO\_}DCR$ | 1.72 | 1.98 | 2.17 | ns, max |
| Device Control Register Bus data outputs | $T_{PCKDO\_}DCR$ | 1.76 | 2.02 | 2.22 | ns, max |
| Clock and Power Management control outputs | $T_{PCKCO\_}CPM$ | 1.26 | 1.45 | 1.59 | ns, max |
| Reset control outputs | $T_{PCKCO\_}RST$ | 1.32 | 1.51 | 1.66 | ns, max |
| Debug control outputs | $T_{PCKCO\_}DBG$ | 1.94 | 2.22 | 2.44 | ns, max |
| Trace control outputs | $T_{PCKCO\_}TRC$ | 1.35 | 1.56 | 1.71 | ns, max |
| **Clock** | | | | | |
| CPMC405CLOCK minimum pulse width, high | $T_{CPWH}$ | 1.25 | 1.42 | 1.66 | ns, min |
| CPMC405CLOCK minimum pulse width, low | $T_{CPWL}$ | 1.25 | 1.42 | 1.66 | ns, min |

*Table 18:* **Processor Block PLB Switching Characteristics**

| | | Speed Grade | | | |
|---|---|---|---|---|---|
| **Description** | **Symbol** | **-7** | **-6** | **-5** | **Units** |
| **Setup and Hold Relative to Clock (PLBCLK)** | | | | | |
| Processor Local Bus(ICU/DCU) control inputs | $T_{PCCK\_}PLB/T_{PCKC\_}PLB$ | 0.98/ 0.18 | 1.12/ 0.21 | 1.23/ 0.23 | ns, min |
| Processor Local Bus (ICU/DCU) data inputs | $T_{PDCK\_}PLB/T_{PCKD\_}PLB$ | 0.62/ 0.16 | 0.71/ 0.18 | 0.78/ 0.20 | ns, min |
| **Clock to Out** | | | | | |
| Processor Local Bus(ICU/DCU) control outputs | $T_{PCKCO\_}PLB$ | 1.34 | 1.54 | 1.69 | ns, max |
| Processor Local Bus(ICU/DCU) address bus outputs | $T_{PCKAO\_}PLB$ | 1.16 | 1.34 | 1.47 | ns, max |
| Processor Local Bus(ICU/DCU) data bus outputs | $T_{PCKDO\_}PLB$ | 1.44 | 1.65 | 1.81 | ns, max |

## Output Clock Jitter

*Table 59:* **Output Clock Jitter**

| Description | Symbol | Constraints | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | –7 | –6 | –5 | |
| **Clock Synthesis Period Jitter** | | | | | | |
| CLK0 | CLKOUT_PER_JITT_0 | | ±100 | ±100 | ±100 | ps |
| CLK90 | CLKOUT_PER_JITT_90 | | ±150 | ±150 | ±150 | ps |
| CLK180 | CLKOUT_PER_JITT_180 | | ±150 | ±150 | ±150 | ps |
| CLK270 | CLKOUT_PER_JITT_270 | | ±150 | ±150 | ±150 | ps |
| CLK2X, CLK2X180 | CLKOUT_PER_JITT_2X | | ±200 | ±200 | ±200 | ps |
| CLKDV (integer division) | CLKOUT_PER_JITT_DV1 | | ±150 | ±150 | ±150 | ps |
| CLKDV (non-integer division) | CLKOUT_PER_JITT_DV2 | | ±300 | ±300 | ±300 | ps |
| CLKFX, CLKFX180 | CLKOUT_PER_JITT_FX | | Note (1) | Note (1) | Note (1) | ps |

**Notes:**
1. Use the **Jitter Calculator** on the Xilinx website (http://www.xilinx.com/applications/web_ds_v2/jitter_calc.htm) for CLKFX and CLKFX180 output jitter.

## Output Clock Phase Alignment

*Table 60:* **Output Clock Phase Alignment**

| Description | Symbol | Constraints | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | –7 | –6 | –5 | |
| **Phase Offset Between CLKIN and CLKFB** | | | | | | |
| CLKIN/CLKFB | CLKIN_CLKFB_PHASE | | ±50 | ±50 | ±50 | ps |
| **Phase Offset Between Any DCM Outputs** | | | | | | |
| All CLK* outputs | CLKOUT_PHASE | | ±140 | ±140 | ±140 | ps |
| **Duty Cycle Precision** | | | | | | |
| DLL outputs(1) | CLKOUT_DUTY_CYCLE_DLL(2) | | ±150 | ±150 | ±150 | ps |
| CLKFX outputs | CLKOUT_DUTY_CYCLE_FX | | ±100 | ±100 | ±100 | ps |

**Notes:**
1. “DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION = TRUE.
3. Specification also applies to PSCLK.

*Table 7:* **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 |
| 5 | IO_L46N_5 | W11 | | | |
| 5 | IO_L46P_5 | W10 | | | |
| 5 | IO_L45N_5/VREF_5 | AD9 | | | |
| 5 | IO_L45P_5 | AC9 | | | |
| 5 | IO_L43N_5 | AB9 | | | |
| 5 | IO_L43P_5 | AA9 | | | |
| 5 | IO_L39N_5 | Y9 | | | |
| 5 | IO_L39P_5 | W9 | | | |
| 5 | IO_L37N_5 | AF8 | | | |
| 5 | IO_L37P_5 | AE8 | | | |
| 5 | IO_L09N_5/VREF_5 | AB8 | | | |
| 5 | IO_L09P_5 | AA8 | | | |
| 5 | IO_L07N_5/VREF_5 | Y8 | | | |
| 5 | IO_L07P_5 | W8 | | | |
| 5 | IO_L06N_5/VRP_5 | AD7 | | | |
| 5 | IO_L06P_5/VRN_5 | AC7 | | | |
| 5 | IO_L05_5/No_Pair | AB7 | | | |
| 5 | IO_L03N_5/D4 | AA7 | | | |
| 5 | IO_L03P_5/D5 | Y7 | | | |
| 5 | IO_L02N_5/D6 | AC6 | | | |
| 5 | IO_L02P_5/D7 | AB6 | | | |
| 5 | IO_L01N_5/RDWR_B | AC5 | | | |
| 5 | IO_L01P_5/CS_B | AB5 | | | |
| | | | | | |
| 6 | IO_L01P_6/VRN_6 | AE1 | | | |
| 6 | IO_L01N_6/VRP_6 | AD1 | | | |
| 6 | IO_L02P_6 | AD2 | | | |
| 6 | IO_L02N_6 | AC3 | | | |
| 6 | IO_L03P_6 | AC2 | | | |
| 6 | IO_L03N_6/VREF_6 | AC1 | | | |
| 6 | IO_L05P_6 | AB4 | | | |
| 6 | IO_L05N_6 | AA5 | | | |
| 6 | IO_L06P_6 | AB2 | | | |
| 6 | IO_L06N_6 | AB1 | | | |
| 6 | IO_L23P_6 | AA6 | NC | | |

*Table 8:* **FF672 — XC2VP2, XC2VP4, and XC2VP7**

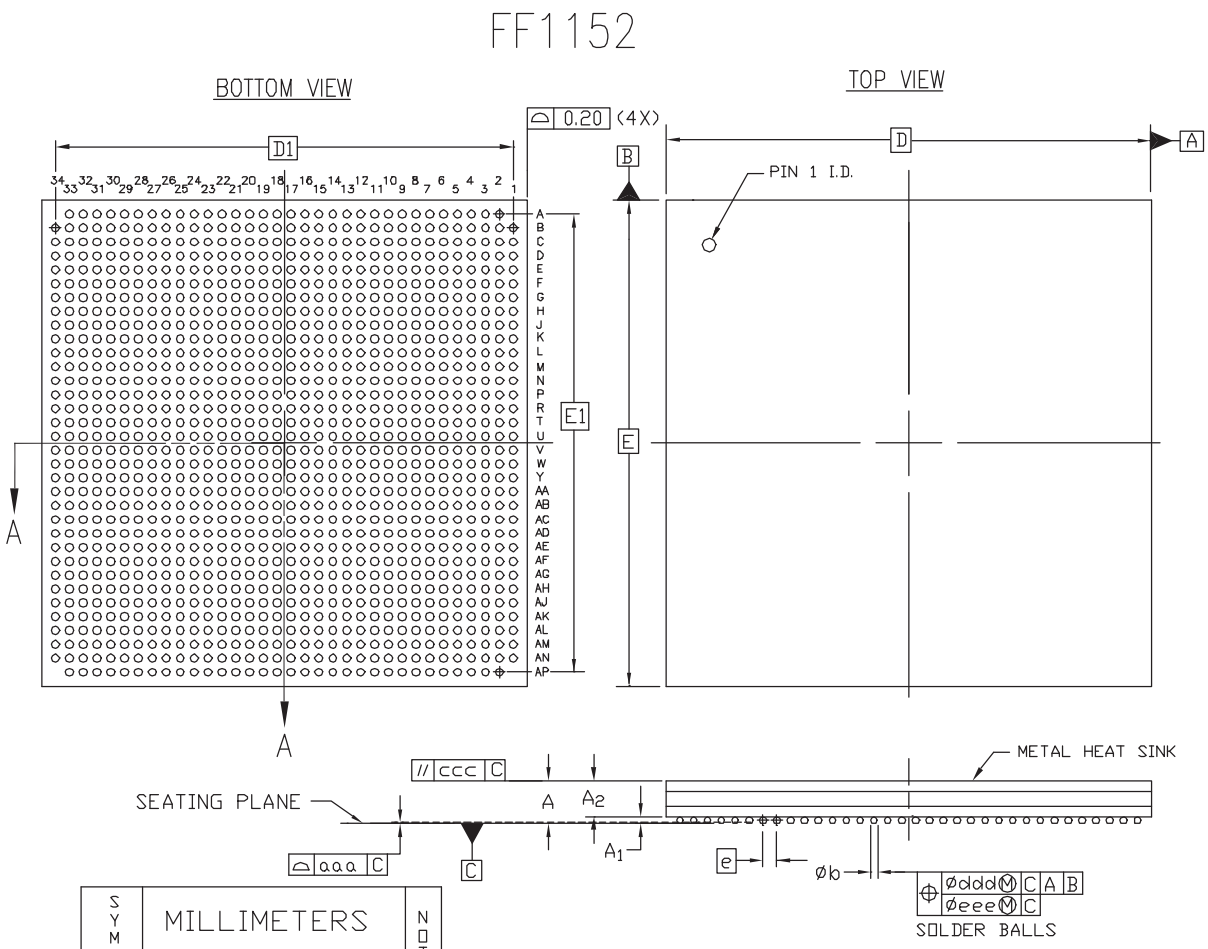
| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP2 | XC2VP4 | XC2VP7 |
| 6 | IO_L52N_6 | U22 | NC | | |
| 6 | IO_L53P_6 | U23 | NC | | |
| 6 | IO_L53N_6 | U24 | NC | | |
| 6 | IO_L54P_6 | V26 | NC | | |
| 6 | IO_L54N_6 | U26 | NC | | |
| 6 | IO_L55P_6 | U20 | NC | | |
| 6 | IO_L55N_6 | T19 | NC | | |
| 6 | IO_L56P_6 | T20 | NC | | |
| 6 | IO_L56N_6 | R20 | NC | | |
| 6 | IO_L57P_6 | T21 | NC | | |
| 6 | IO_L57N_6/VREF_6 | T22 | NC | | |
| 6 | IO_L58P_6 | T23 | NC | | |
| 6 | IO_L58N_6 | T24 | NC | | |
| 6 | IO_L59P_6 | T25 | NC | | |
| 6 | IO_L59N_6 | T26 | NC | | |
| 6 | IO_L60P_6 | R19 | NC | | |
| 6 | IO_L60N_6 | P19 | NC | | |
| 6 | IO_L85P_6 | R21 | | | |
| 6 | IO_L85N_6 | R22 | | | |
| 6 | IO_L86P_6 | R23 | | | |
| 6 | IO_L86N_6 | R24 | | | |
| 6 | IO_L87P_6 | R25 | | | |
| 6 | IO_L87N_6/VREF_6 | R26 | | | |
| 6 | IO_L88P_6 | P20 | | | |
| 6 | IO_L88N_6 | P21 | | | |
| 6 | IO_L89P_6 | P22 | | | |
| 6 | IO_L89N_6 | P23 | | | |
| 6 | IO_L90P_6 | P24 | | | |
| 6 | IO_L90N_6 | P25 | | | |
| | | | | | |
| 7 | IO_L90P_7 | N25 | | | |
| 7 | IO_L90N_7 | N24 | | | |
| 7 | IO_L89P_7 | N23 | | | |
| 7 | IO_L89N_7 | N22 | | | |
| 7 | IO_L88P_7 | N21 | | | |
| 7 | IO_L88N_7/VREF_7 | N20 | | | |
| 7 | IO_L87P_7 | M26 | | | |

*Table 8:* **FF672 — XC2VP2, XC2VP4, and XC2VP7**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP2 | XC2VP4 | XC2VP7 |
| N/A | GND | R15 | | | |
| N/A | GND | R16 | | | |
| N/A | GND | R17 | | | |
| N/A | GND | T11 | | | |
| N/A | GND | T12 | | | |
| N/A | GND | T13 | | | |
| N/A | GND | T14 | | | |
| N/A | GND | T15 | | | |
| N/A | GND | T16 | | | |
| N/A | GND | U10 | | | |
| N/A | GND | U12 | | | |
| N/A | GND | U13 | | | |
| N/A | GND | U14 | | | |
| N/A | GND | U15 | | | |
| N/A | GND | U17 | | | |
| N/A | GND | Y20 | | | |
| N/A | GND | AA21 | | | |
| N/A | GND | AB22 | | | |
| N/A | GND | AC23 | | | |
| N/A | GND | AD24 | | | |

**Notes:**
1. See Table 4 for an explanation of the signals available on this pin.

## FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)




| SYMBOL | MILLIMETERS | | | NOTE |
|---|---|---|---|---|
| | MIN. | NOM. | MAX. | |
| A | --- | 3.20 | 3.40 | |
| $A_1$ | 0.40 | 0.50 | 0.60 | |
| $A_2$ | --- | --- | 2.80 | |
| D/E | 35.00 BASIC | | | |
| $D_1/E_1$ | 33.00 REF | | | |
| e | 1.00 BASIC | | | |
| øb | 0.50 | 0.60 | 0.70 | |
| aaa | --- | --- | 0.20 | |
| ccc | --- | --- | 0.35 | |
| ddd | --- | --- | 0.30 | |
| eee | --- | --- | 0.10 | |
| M | 34 | | | 2 |

NOTES:
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

*Figure 6:* **FF1152 Flip-Chip Fine-Pitch BGA Package Specifications**

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| 0 | IO_L43N_0 | B22 | | |
| 0 | IO_L43P_0 | C22 | | |
| 0 | IO_L44N_0 | K21 | | |
| 0 | IO_L44P_0 | L21 | | |
| 0 | IO_L45N_0 | G21 | | |
| 0 | IO_L45P_0/VREF_0 | H21 | | |
| 0 | IO_L46N_0 | E21 | | |
| 0 | IO_L46P_0 | F21 | | |
| 0 | IO_L47N_0 | K20 | | |
| 0 | IO_L47P_0 | L20 | | |
| 0 | IO_L48N_0 | C21 | | |
| 0 | IO_L48P_0 | D21 | | |
| 0 | IO_L49N_0 | A21 | | |
| 0 | IO_L49P_0 | B21 | | |
| 0 | IO_L50_0/No_Pair | G20 | | |
| 0 | IO_L53_0/No_Pair | H19 | | |
| 0 | IO_L54N_0 | E20 | | |
| 0 | IO_L54P_0 | F20 | | |
| 0 | IO_L55N_0 | C20 | | |
| 0 | IO_L55P_0 | D19 | | |
| 0 | IO_L56N_0 | K19 | | |
| 0 | IO_L56P_0 | L19 | | |
| 0 | IO_L57N_0 | A20 | | |
| 0 | IO_L57P_0/VREF_0 | B20 | | |
| 0 | IO_L66N_0 | F19 | NC | |
| 0 | IO_L66P_0/VREF_0 | G19 | NC | |
| 0 | IO_L67N_0 | B19 | | |
| 0 | IO_L67P_0 | C19 | | |
| 0 | IO_L68N_0 | H18 | | |
| 0 | IO_L68P_0 | J18 | | |
| 0 | IO_L69N_0 | F18 | | |
| 0 | IO_L69P_0/VREF_0 | G18 | | |
| 0 | IO_L73N_0 | D18 | | |
| 0 | IO_L73P_0 | E18 | | |
| 0 | IO_L74N_0/GCLK7P | K18 | | |
| 0 | IO_L74P_0/GCLK6S | L18 | | |
| 0 | IO_L75N_0/GCLK5P | B18 | | |
| 0 | IO_L75P_0/GCLK4S | C18 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 0 | IO_L34P_0 | E27 | NC | |
| 0 | IO_L35N_0 | L26 | NC | |
| 0 | IO_L35P_0 | L25 | NC | |
| 0 | IO_L36N_0 | G26 | NC | |
| 0 | IO_L36P_0/VREF_0 | H26 | NC | |
| 0 | IO_L37N_0 | E26 | | |
| 0 | IO_L37P_0 | F26 | | |
| 0 | IO_L38N_0 | K25 | | |
| 0 | IO_L38P_0 | K24 | | |
| 0 | IO_L39N_0 | C26 | | |
| 0 | IO_L39P_0 | D26 | | |
| 0 | IO_L43N_0 | H25 | | |
| 0 | IO_L43P_0 | J25 | | |
| 0 | IO_L44N_0 | M25 | | |
| 0 | IO_L44P_0 | M24 | | |
| 0 | IO_L45N_0 | F25 | | |
| 0 | IO_L45P_0/VREF_0 | G25 | | |
| 0 | IO_L46N_0 | C25 | | |
| 0 | IO_L46P_0 | D25 | | |
| 0 | IO_L47N_0 | L23 | | |
| 0 | IO_L47P_0 | M22 | | |
| 0 | IO_L48N_0 | H24 | | |
| 0 | IO_L48P_0 | J24 | | |
| 0 | IO_L49N_0 | E25 | | |
| 0 | IO_L49P_0 | E24 | | |
| 0 | IO_L50_0/No_Pair | N23 | | |
| 0 | IO_L53_0/No_Pair | M23 | | |
| 0 | IO_L54N_0 | H23 | | |
| 0 | IO_L54P_0 | J23 | | |
| 0 | IO_L55N_0 | F24 | | |
| 0 | IO_L55P_0 | G23 | | |
| 0 | IO_L56N_0 | K22 | | |
| 0 | IO_L56P_0 | L22 | | |
| 0 | IO_L57N_0 | C23 | | |
| 0 | IO_L57P_0/VREF_0 | D23 | | |
| 0 | IO_L58N_0 | H22 | | |
| 0 | IO_L58P_0 | J22 | | |
| 0 | IO_L59N_0 | N22 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| N/A | GNDA18 | AU16 | | |
| N/A | TXPPAD18 | AW18 | | |
| N/A | TXNPAD18 | AW19 | | |
| N/A | VTTXPAD18 | AV19 | | |
| N/A | AVCCAUXTX18 | AV18 | | |
| N/A | AVCCAUXRX19 | AV21 | | |
| N/A | VTRXPAD19 | AV22 | | |
| N/A | RXNPAD19 | AW21 | | |
| N/A | RXPPAD19 | AW22 | | |
| N/A | GNDA19 | AU24 | | |
| N/A | TXPPAD19 | AW23 | | |
| N/A | TXNPAD19 | AW24 | | |
| N/A | VTTXPAD19 | AV24 | | |
| N/A | AVCCAUXTX19 | AV23 | | |
| N/A | AVCCAUXRX20 | AV25 | | |
| N/A | VTRXPAD20 | AV26 | | |
| N/A | RXNPAD20 | AW25 | | |
| N/A | RXPPAD20 | AW26 | | |
| N/A | GNDA20 | AU27 | | |
| N/A | TXPPAD20 | AW27 | | |
| N/A | TXNPAD20 | AW28 | | |
| N/A | VTTXPAD20 | AV28 | | |
| N/A | AVCCAUXTX20 | AV27 | | |
| N/A | AVCCAUXRX21 | AV29 | | |
| N/A | VTRXPAD21 | AV30 | | |
| N/A | RXNPAD21 | AW29 | | |
| N/A | RXPPAD21 | AW30 | | |
| N/A | GNDA21 | AU31 | | |
| N/A | TXPPAD21 | AW31 | | |
| N/A | TXNPAD21 | AW32 | | |
| N/A | VTTXPAD21 | AV32 | | |
| N/A | AVCCAUXTX21 | AV31 | | |
| N/A | AVCCAUXRX23 | AV33 | | |
| N/A | VTRXPAD23 | AV34 | | |
| N/A | RXNPAD23 | AW33 | | |
| N/A | RXPPAD23 | AW34 | | |
| N/A | GNDA23 | AU34 | | |
| N/A | TXPPAD23 | AW35 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 1 | IO_L48N_1 | | J17 | | |
| 1 | IO_L48P_1 | | H17 | | |
| 1 | IO_L47N_1 | | K17 | | |
| 1 | IO_L47P_1 | | L17 | | |
| 1 | IO_L46N_1 | | M17 | | |
| 1 | IO_L46P_1 | | M18 | | |
| 1 | IO_L45N_1/VREF_1 | | F16 | | |
| 1 | IO_L45P_1 | | E16 | | |
| 1 | IO_L44N_1 | | G16 | | |
| 1 | IO_L44P_1 | | H16 | | |
| 1 | IO_L43N_1 | | K16 | | |
| 1 | IO_L43P_1 | | J16 | | |
| 1 | IO_L39N_1 | | M16 | | |
| 1 | IO_L39P_1 | | L16 | | |
| 1 | IO_L38N_1 | | C15 | | |
| 1 | IO_L38P_1 | | C14 | | |
| 1 | IO_L37N_1 | | F15 | | |
| 1 | IO_L37P_1 | | E15 | | |
| 1 | IO_L87N_1/VREF_1 | | J15 | NC | |
| 1 | IO_L87P_1 | | H15 | NC | |
| 1 | IO_L86N_1 | | K15 | NC | |
| 1 | IO_L86P_1 | | L15 | NC | |
| 1 | IO_L85N_1 | | E14 | NC | |
| 1 | IO_L85P_1 | | D14 | NC | |
| 1 | IO_L84N_1 | | G14 | NC | |
| 1 | IO_L84P_1 | | F14 | NC | |
| 1 | IO_L83_1/No_Pair | | H14 | NC | |
| 1 | IO_L78N_1 | | L14 | NC | |
| 1 | IO_L78P_1 | | K14 | NC | |
| 1 | IO_L36N_1/VREF_1 | | M14 | | |
| 1 | IO_L36P_1 | | M15 | | |
| 1 | IO_L35N_1 | | C13 | | |
| 1 | IO_L35P_1 | | D13 | | |
| 1 | IO_L34N_1 | | F13 | | |
| 1 | IO_L34P_1 | | E13 | | |
| 1 | IO_L30N_1 | | H13 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 1 | IO_L30P_1 | | G13 | | |
| 1 | IO_L29N_1 | | K13 | | |
| 1 | IO_L29P_1 | | J13 | | |
| 1 | IO_L28N_1 | | M13 | | |
| 1 | IO_L28P_1 | | L13 | | |
| 1 | IO_L27N_1/VREF_1 | | E12 | | |
| 1 | IO_L27P_1 | | D12 | | |
| 1 | IO_L26N_1 | | F12 | | |
| 1 | IO_L26P_1 | | G12 | | |
| 1 | IO_L25N_1 | | J12 | | |
| 1 | IO_L25P_1 | | H12 | | |
| 1 | IO_L21N_1 | | L12 | | |
| 1 | IO_L21P_1 | | K12 | | |
| 1 | IO_L20N_1 | | C11 | | |
| 1 | IO_L20P_1 | | C10 | | |
| 1 | IO_L19N_1 | | F11 | | |
| 1 | IO_L19P_1 | | E11 | | |
| 1 | IO_L09N_1/VREF_1 | | J11 | | |
| 1 | IO_L09P_1 | | H11 | | |
| 1 | IO_L08N_1 | | D10 | | |
| 1 | IO_L08P_1 | | E10 | | |
| 1 | IO_L07N_1 | | G10 | | |
| 1 | IO_L07P_1 | | F10 | | |
| 1 | IO_L06N_1 | | J10 | | |
| 1 | IO_L06P_1 | | H10 | | |
| 1 | IO_L05_1/No_Pair | | K11 | | |
| 1 | IO_L03N_1/VREF_1 | | D9 | | |
| 1 | IO_L03P_1 | | C9 | | |
| 1 | IO_L02N_1 | | E9 | | |
| 1 | IO_L02P_1 | | F9 | | |
| 1 | IO_L01N_1/VRP_1 | | H9 | | |
| 1 | IO_L01P_1/VRN_1 | | G9 | | |
| | | | | | |
| 2 | IO_L01N_2/VRP_2 | | C5 | | |
| 2 | IO_L01P_2/VRN_2 | | C6 | | |
| 2 | IO_L02N_2 | | E7 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 6 | IO_L52N_6 | | AE42 | | |
| 6 | IO_L53P_6 | | AE32 | | |
| 6 | IO_L53N_6 | | AE33 | | |
| 6 | IO_L54P_6 | | AD35 | | |
| 6 | IO_L54N_6 | | AD36 | | |
| 6 | IO_L55P_6 | | AD37 | | |
| 6 | IO_L55N_6 | | AD38 | | |
| 6 | IO_L56P_6 | | AD31 | | |
| 6 | IO_L56N_6 | | AD32 | | |
| 6 | IO_L57P_6 | | AD39 | | |
| 6 | IO_L57N_6/VREF_6 | | AD40 | | |
| 6 | IO_L58P_6 | | AD41 | | |
| 6 | IO_L58N_6 | | AD42 | | |
| 6 | IO_L59P_6 | | AD33 | | |
| 6 | IO_L59N_6 | | AD34 | | |
| 6 | IO_L60P_6 | | AC33 | | |
| 6 | IO_L60N_6 | | AC34 | | |
| 6 | IO_L85P_6 | | AC36 | | |
| 6 | IO_L85N_6 | | AC37 | | |
| 6 | IO_L86P_6 | | AC31 | | |
| 6 | IO_L86N_6 | | AC32 | | |
| 6 | IO_L87P_6 | | AC39 | | |
| 6 | IO_L87N_6/VREF_6 | | AC40 | | |
| 6 | IO_L88P_6 | | AB33 | | |
| 6 | IO_L88N_6 | | AB34 | | |
| 6 | IO_L89P_6 | | AB36 | | |
| 6 | IO_L89N_6 | | AB37 | | |
| 6 | IO_L90P_6 | | AB39 | | |
| 6 | IO_L90N_6 | | AB40 | | |
| | | | | | |
| 7 | IO_L90P_7 | | AA39 | | |
| 7 | IO_L90N_7 | | AA40 | | |
| 7 | IO_L89P_7 | | AB31 | | |
| 7 | IO_L89N_7 | | AA31 | | |
| 7 | IO_L88P_7 | | AA36 | | |
| 7 | IO_L88N_7/VREF_7 | | AA37 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| N/A | GND | | AB18 | | |
| N/A | GND | | AB17 | | |
| N/A | GND | | AB11 | | |
| N/A | GND | | AB8 | | |
| N/A | GND | | AB5 | | |
| N/A | GND | | AC41 | | |
| N/A | GND | | AC26 | | |
| N/A | GND | | AC25 | | |
| N/A | GND | | AC24 | | |
| N/A | GND | | AC23 | | |
| N/A | GND | | AC22 | | |
| N/A | GND | | AC21 | | |
| N/A | GND | | AC20 | | |
| N/A | GND | | AC19 | | |
| N/A | GND | | AC18 | | |
| N/A | GND | | AC17 | | |
| N/A | GND | | AC2 | | |
| N/A | GND | | AD26 | | |
| N/A | GND | | AD25 | | |
| N/A | GND | | AD24 | | |
| N/A | GND | | AD23 | | |
| N/A | GND | | AD22 | | |
| N/A | GND | | AD21 | | |
| N/A | GND | | AD20 | | |
| N/A | GND | | AD19 | | |
| N/A | GND | | AD18 | | |
| N/A | GND | | AD17 | | |
| N/A | GND | | AE37 | | |
| N/A | GND | | AE34 | | |
| N/A | GND | | AE26 | | |
| N/A | GND | | AE25 | | |
| N/A | GND | | AE24 | | |
| N/A | GND | | AE23 | | |
| N/A | GND | | AE22 | | |
| N/A | GND | | AE21 | | |
| N/A | GND | | AE20 | | |

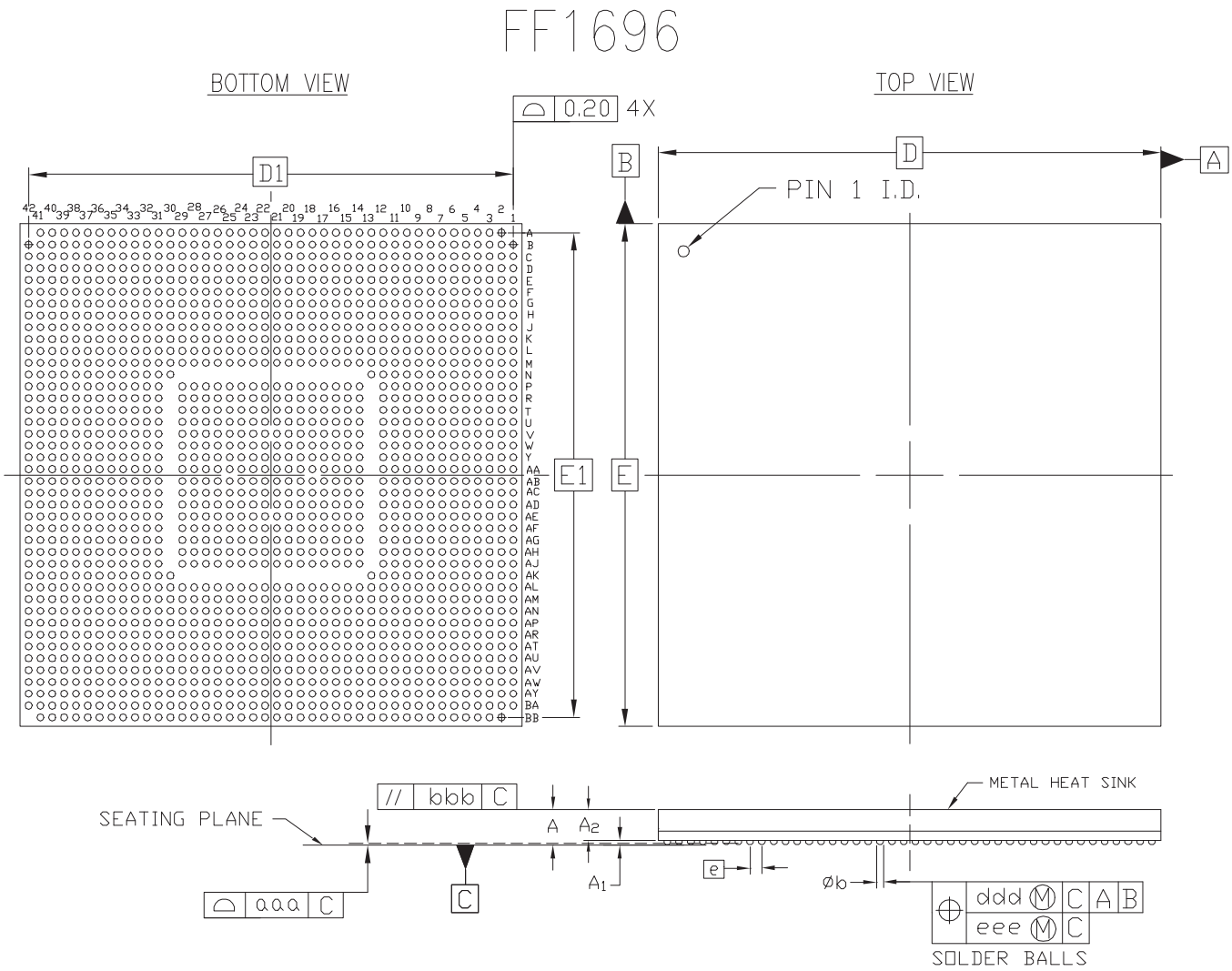
*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 2 | IO_L22N_2/VREF_2 | L4 | |
| 2 | IO_L22P_2 | L5 | |
| 2 | IO_L23N_2 | T8 | |
| 2 | IO_L23P_2 | T9 | |
| 2 | IO_L24N_2 | L3 | |
| 2 | IO_L24P_2 | K3 | |
| 2 | IO_L25N_2 | L1 | |
| 2 | IO_L25P_2 | L2 | |
| 2 | IO_L26N_2 | U12 | |
| 2 | IO_L26P_2 | V12 | |
| 2 | IO_L27N_2 | M7 | |
| 2 | IO_L27P_2 | L6 | |
| 2 | IO_L28N_2/VREF_2 | M5 | |
| 2 | IO_L28P_2 | M6 | |
| 2 | IO_L29N_2 | U10 | |
| 2 | IO_L29P_2 | U11 | |
| 2 | IO_L30N_2 | M3 | |
| 2 | IO_L30P_2 | M4 | |
| 2 | IO_L31N_2 | N6 | |
| 2 | IO_L31P_2 | N7 | |
| 2 | IO_L32N_2 | U7 | |
| 2 | IO_L32P_2 | U8 | |
| 2 | IO_L33N_2 | N3 | |
| 2 | IO_L33P_2 | N4 | |
| 2 | IO_L34N_2/VREF_2 | N2 | |
| 2 | IO_L34P_2 | M2 | |
| 2 | IO_L35N_2 | V10 | |
| 2 | IO_L35P_2 | V11 | |
| 2 | IO_L36N_2 | P6 | |
| 2 | IO_L36P_2 | P7 | |
| 2 | IO_L37N_2 | P1 | |
| 2 | IO_L37P_2 | P2 | |
| 2 | IO_L38N_2 | V8 | |
| 2 | IO_L38P_2 | V9 | |
| 2 | IO_L39N_2 | R6 | |
| 2 | IO_L39P_2 | P5 | |
| 2 | IO_L40N_2/VREF_2 | R4 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 2 | VCCO_2 | F4 | |
| 1 | VCCO_1 | R21 | |
| 1 | VCCO_1 | P21 | |
| 1 | VCCO_1 | R20 | |
| 1 | VCCO_1 | P20 | |
| 1 | VCCO_1 | R19 | |
| 1 | VCCO_1 | P19 | |
| 1 | VCCO_1 | R18 | |
| 1 | VCCO_1 | P18 | |
| 1 | VCCO_1 | H18 | |
| 1 | VCCO_1 | D18 | |
| 1 | VCCO_1 | P17 | |
| 1 | VCCO_1 | H14 | |
| 1 | VCCO_1 | D14 | |
| 1 | VCCO_1 | M13 | |
| 1 | VCCO_1 | D10 | |
| 0 | VCCO_0 | D33 | |
| 0 | VCCO_0 | M30 | |
| 0 | VCCO_0 | H29 | |
| 0 | VCCO_0 | D29 | |
| 0 | VCCO_0 | P26 | |
| 0 | VCCO_0 | R25 | |
| 0 | VCCO_0 | P25 | |
| 0 | VCCO_0 | H25 | |
| 0 | VCCO_0 | D25 | |
| 0 | VCCO_0 | R24 | |
| 0 | VCCO_0 | P24 | |
| 0 | VCCO_0 | R23 | |
| 0 | VCCO_0 | P23 | |
| 0 | VCCO_0 | R22 | |
| 0 | VCCO_0 | P22 | |
| | | | |
| N/A | CCLK | AM10 | |
| N/A | PROG_B | J33 | |
| N/A | DONE | AN10 | |
| N/A | M0 | AP33 | |
| N/A | M1 | AN33 | |

## FF1696 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)




| SYMBOL | MILLIMETERS | | | NOTE |
|---|---|---|---|---|
| | MIN. | NOM. | MAX. | |
| A | | 3.20 | 3.45 | |
| $A_1$ | 0.40 | 0.50 | 0.60 | |
| $A_2$ | | | 2.85 | |
| D/E | 42.50 BASIC | | | |
| $D_1/E_1$ | 41.00 REF | | | |
| e | 1.00 BASIC | | | |
| øb | 0.50 | 0.60 | 0.70 | |
| aaa | | | 0.20 | |
| bbb | | | 0.25 | |
| ddd | | | 0.25 | |
| eee | | | 0.10 | |
| M | | 42 | | 2 |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)

*Figure 10:* **FF1696 Flip-Chip Fine-Pitch BGA Package Specifications**

## Revision History

This section records the change history for this module of the data sheet.

| Date | Version | Revision |
|---|---|---|
| 01/31/02 | 1.0 | Initial Xilinx release. |
| 08/14/02 | 2.0 | Added package and pinout information for new devices. |
| 08/27/02 | 2.1 | • Updated SelectIO-Ultra information in Table 4. (Table deleted in v2.3.)<br>• Corrected direction for RXNPAD and TXPPAD in Table 4 (formerly Table 5). |
| 09/27/02 | 2.2 | Corrected Table 2 and Table 3 entries for XC2VP30, FF1152 package, maximum I/Os from 692 to 644. |
| 11/20/02 | 2.3 | Added Number of Differential Pairs data to Table 3. Removed former Table 4. |
| 12/03/02 | 2.4 | Corrections in Table 4:<br>• Reclassified GCLKx (S/P) pins as Input/Output, since these pins can be used as normal I/Os if not used as clocks.<br>• Added cautionary note to PWRDWN_B pin, indicating that this function is not supported. |
| 01/20/03 | 2.5 | Added and removed package/pinout information for existing devices:<br>• In Table 1, added FG676 package information.<br>• In Table 3, added FG676 package option for XC2VP20, XC2VP30, and XC2VP40.<br>• In Table 12, removed FF1517 package option for XC2VP40.<br>• Added FG676 package pinouts (Table 7) for XC2VP20, XC2VP30, and XC2VP40.<br>• Added package diagram (Figure 3) for FG676 package. |
| 05/19/03 | 2.5.1 | • Added section **BREFCLK Pin Definitions**, page 5.<br>• Added clarification to Table 4 and all device pinout tables regarding the dual-use nature of pins D0/DIN and BUSY/DOUT during configuration. |
| 06/19/03 | 2.5.3 | • Added notation of "open-drain" to TDO pin in Table 4.<br>• The final GND pin in each of six pinout tables was inadvertently deleted in v2.5.1. This revision restores the deleted GND pins as follows:<br>- Pin A1, Table 6, page 16 (FG456)<br>- Pin AF26, Table 7, page 30 (FG676)<br>- Pin AN34, Table 10, page 98 (FF1152)<br>- Pin E1, Table 11, page 130 (FF1148)<br>- Pin C38, Table 12, page 162 (FF1517)<br>- Pin E1, Table 14, page 253 (FF1696) |
| 08/25/03 | 2.5.5 | • Table 4: Deleted Note 2, obsolete. There is only one GNDA pin per MGT.<br>• Table 4: Deleted pins ALT_VRP and ALT_VRN. Not used in Virtex-II Pro FPGAs. |
| 12/10/03 | 3.0 | • XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**. |
| 02/19/04 | 3.1 | • Table 4, signal descriptions column:<br>- For signals TDI, TMS, and TCK, added: Pins are 3.3V-compatible.<br>- For signals M2, M1, M0, added: Tie to 3.3V only with 100Ω series resistor. No toggling during or after configuration.<br>- For signal TDO, added: No internal pull-up. External pull-up to 3.3V OK with resistor greater than 200Ω. |
| 03/09/04 | 3.1.1 | • Recompiled for backward compatibility with Acrobat 4 and above. No content changes. |
| 06/30/04 | 4.0 | Merged in DS110-4 (Module 4 of Virtex-II Pro X data sheet). Added data on available Pb-free packages and updated package diagrams for affected devices. |