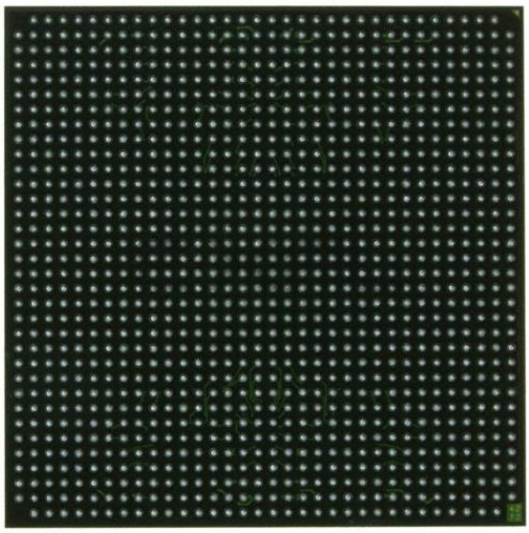
AMD Xilinx - XC2VP30-6FF1152C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3424
Number of Logic Elements/Cells	30816
Total RAM Bits	2506752
Number of I/O	644
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp30-6ff1152c

Virtex-II Pro Ordering Examples

Virtex-II Pro ordering examples are shown in Figure 1 (flip-chip package) and Figure 2 (Pb-free wire-bond package).

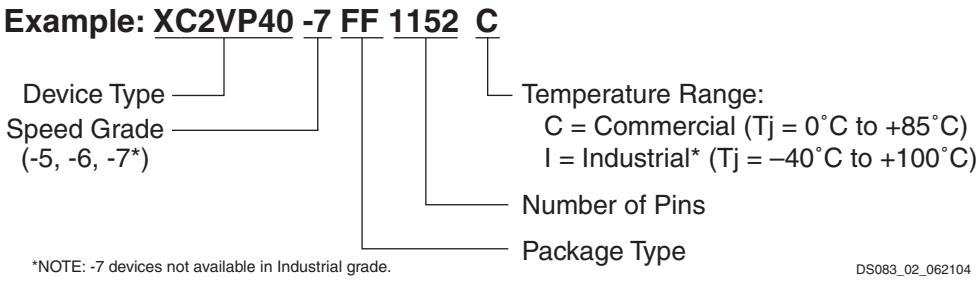

Figure 1: **Virtex-II Pro Ordering Example, Flip-Chip Package**

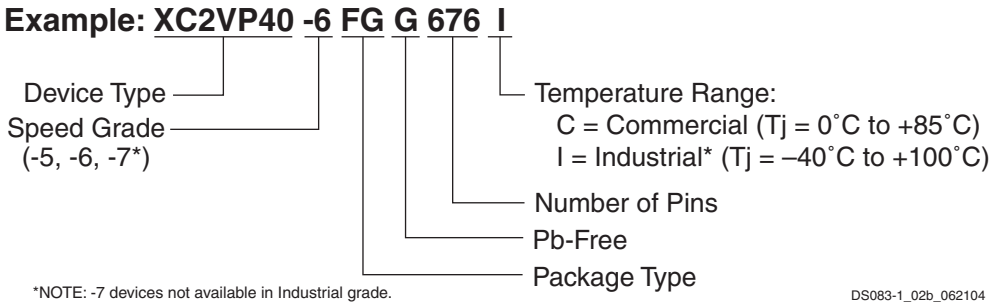

Figure 2: **Virtex-II Pro Ordering Example, Pb-Free Wire-Bond Package**

Virtex-II Pro X Ordering Example

A Virtex-II Pro X ordering example is shown in Figure 3.

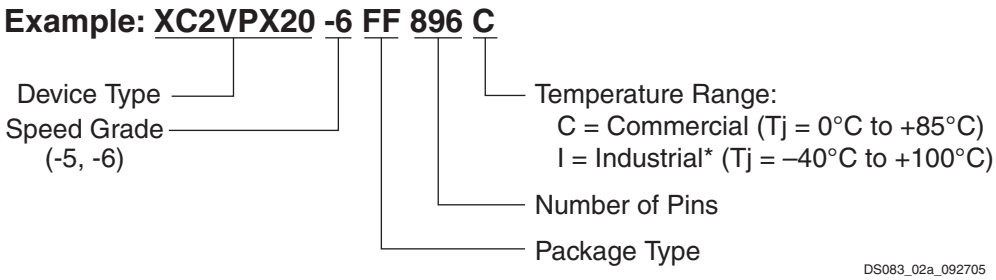

Figure 3: **Virtex-II Pro X Ordering Example, Flip-Chip Package**

cation is given at the receiver interface. The realignment indicator is a distinct output.

The transceiver continuously monitors the data for the presence of the 10-bit character(s). Upon each occurrence of a 10-bit character, the data is checked for word alignment. If comma detect is disabled, the data is not aligned to any particular pattern. The programmable option allows a user to align data on comma+, comma–, both, or a unique user-defined and programmed sequence.

Comma detection has been expanded beyond 10-bit symbol detection and alignment to include 8-bit symbol detection and alignment for 16-, 20-, 32-, and 40-bit paths. The ability to detect symbols, and then either align to 1-word, 2-word, or 4-word boundaries is included. The RXSLIDE input allows the user to “slide” or “slip” the alignment by one bit in each 16-, 20-, 32- and 40-bit mode at any time for SONET applications. Comma detection can be bypassed when needed.

Clock Correction

RXRECCLK (the recovered clock) reflects the data rate of the incoming data. RXUSRCLK defines the rate at which the FPGA fabric consumes the data. Ideally, these rates are identical. However, since the clocks typically have different sources, one of the clocks will be faster than the other. The receiver buffer accommodates this difference between the clock rates. See Figure 6.

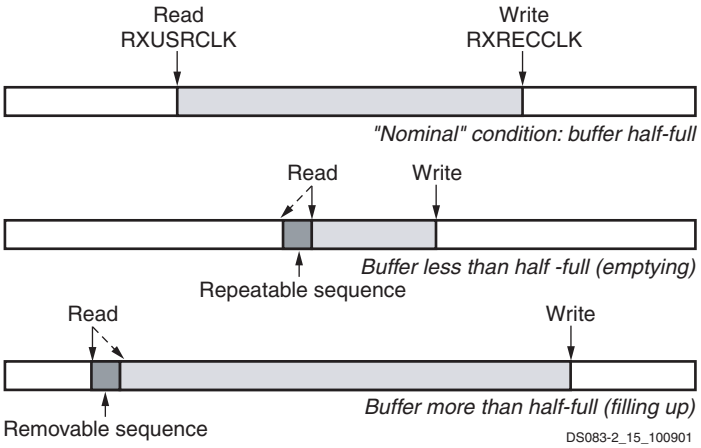

Figure 6: **Clock Correction in Receiver**

Nominally, the buffer is always half full. This is shown in the top buffer, Figure 6, where the shaded area represents buffered data not yet read. Received data is inserted via the write pointer under control of RXRECCLK. The FPGA fabric reads data via the read pointer under control of RXUSRCLK. The half full/half empty condition of the buffer gives a cushion for the differing clock rates. This operation continues indefinitely, regardless of whether or not "meaningful" data is being received. When there is no meaningful data to be received, the incoming data will consist of IDLE characters or other padding.

If RXUSRCLK is faster than RXRECCLK, the buffer becomes more empty over time. The clock correction logic corrects for this by decrementing the read pointer to reread a repeatable byte sequence. This is shown in the middle buffer, Figure 6, where the solid read pointer decrements to the value represented by the dashed pointer. By decrementing the read pointer instead of incrementing it in the usual fashion, the buffer is partially refilled. The transceiver design will repeat a single repeatable byte sequence when necessary to refill a buffer. If the byte sequence length is greater than one, and if attribute CLK_COR_REPEAT_WAIT is 0, then the transceiver may repeat the same sequence multiple times until the buffer is refilled to the desired extent.

Similarly, if RXUSRCLK is slower than RXRECCLK, the buffer will fill up over time. The clock correction logic corrects for this by incrementing the read pointer to skip over a removable byte sequence that need not appear in the final FPGA fabric byte stream. This is shown in the bottom buffer, Figure 6, where the solid read pointer increments to the value represented by the dashed pointer. This accelerates the emptying of the buffer, preventing its overflow. The transceiver design will skip a single byte sequence when necessary to partially empty a buffer. If attribute CLK_COR_REPEAT_WAIT is 0, the transceiver may also skip two consecutive removable byte sequences in one step to further empty the buffer when necessary.

These operations require the clock correction logic to recognize a byte sequence that can be freely repeated or omitted in the incoming data stream. This sequence is generally an IDLE sequence, or other sequence comprised of special values that occur in the gaps separating packets of meaningful data. These gaps are required to occur sufficiently often to facilitate the timely execution of clock correction.

Channel Bonding

Some gigabit I/O standards such as Infiniband specify the use of multiple transceivers in parallel for even higher data rates. Words of data are split into bytes, with each byte sent over a separate channel (transceiver). See Figure 7.

The top half of the figure shows the transmission of words split across four transceivers (channels or lanes). PPPP, QQQQ, RRRR, SSSS, and TTTT represent words sent over the four channels.

The bottom-left portion of Figure 7 shows the initial situation in the FPGA’s receivers at the other end of the four channels. Due to variations in transmission delay—especially if the channels are routed through repeaters—the FPGA fabric might not correctly assemble the bytes into complete words. The bottom-left illustration shows the incorrect assembly of data words PQPP, QRQQ, RSRR, and so forth.

To support correction of this misalignment, the data stream includes special byte sequences that define corresponding points in the several channels. In the bottom half of Figure 7, the shaded "P" bytes represent these special characters. Each receiver recognizes the "P" channel bond-

- Execution unit
- Timers
- Debug logic unit

It operates on instructions in a five stage pipeline consisting of a fetch, decode, execute, write-back, and load write-back stage. Most instructions execute in a single cycle, including loads and stores.

Instruction and Data Cache

The embedded PPC405 core provides an instruction cache unit (ICU) and a data cache unit (DCU) that allow concurrent accesses and minimize pipeline stalls. The instruction and data cache array are 16 KB each. Both cache units are two-way set associative. Each way is organized into 256 lines of 32 bytes (eight words). The instruction set provides a rich assortment of cache control instructions, including instructions to read tag information and data arrays.

The PPC405 core accesses external memory through the instruction (ICU) and data cache units (DCU). The cache units each include a 64-bit PLB master interface, cache arrays, and a cache controller. The ICU and DCU handle cache misses as requests over the PLB to another PLB device such as an external bus interface unit. Cache hits are handled as single cycle memory accesses to the instruction and data caches.

Instruction Cache Unit (ICU)

The ICU provides one or two instructions per cycle to the instruction queue over a 64-bit bus. A line buffer (built into the output of the array for manufacturing test) enables the ICU to be accessed only once for every four instructions, to reduce power consumption by the array.

The ICU can forward any or all of the four or eight words of a line fill to the EXU to minimize pipeline stalls caused by cache misses. The ICU aborts speculative fetches abandoned by the EXU, eliminating unnecessary line fills and enabling the ICU to handle the next EXU fetch. Aborting abandoned requests also eliminates unnecessary external bus activity, thereby increasing external bus utilization.

Data Cache Unit (DCU)

The DCU transfers one, two, three, four, or eight bytes per cycle, depending on the number of byte enables presented by the CPU. The DCU contains a single-element command and store data queue to reduce pipeline stalls; this queue enables the DCU to independently process load/store and cache control instructions. Dynamic PLB request prioritization reduces pipeline stalls even further. When the DCU is busy with a low-priority request while a subsequent storage operation requested by the CPU is stalled; the DCU automatically increases the priority of the current request to the PLB.

The DCU provides additional features that allow the programmer to tailor its performance for a given application. The DCU can function in write-back or write-through mode, as controlled by the Data Cache Write-through Register (DCWR) or the Translation Look-aside Buffer (TLB); the cache controller can be tuned for a balance of performance and memory coherency. Write-on-allocate, controlled by the store word on allocate (SWOA) field of the Core Configuration Register 0 (CCR0), can inhibit line fills caused by store misses, to further reduce potential pipeline stalls and unwanted external bus traffic.

Fetch and Decode Logic

The fetch/decode logic maintains a steady flow of instructions to the execution unit by placing up to two instructions in the fetch queue. The fetch queue consists of three buffers: pre-fetch buffer 1 (PFB1), pre-fetch buffer 0 (PFB0), and decode (DCD). The fetch logic ensures that instructions proceed directly to decode when the queue is empty.

Static branch prediction as implemented on the PPC405 core takes advantage of some standard statistical properties of code. Branches with negative address displacement are by default assumed taken. Branches that do not test the condition or count registers are also predicted as taken. The PPC405 core bases branch prediction upon these default conditions when a branch is not resolved and speculatively fetches along the predicted path. The default prediction can be overridden by software at assembly or compile time.

Branches are examined in the decode and pre-fetch buffer 0 fetch queue stages. Two branch instructions can be handled simultaneously. If the branch in decode is not taken, the fetch logic fetches along the predicted path of the branch instruction in pre-fetch buffer 0. If the branch in decode is taken, the fetch logic ignores the branch instruction in pre-fetch buffer 0.

Execution Unit

The embedded PPC405 core has a single issue execution unit (EXU) containing the register file, arithmetic logic unit (ALU), and the multiply-accumulate (MAC) unit. The execution unit performs all 32-bit PowerPC integer instructions in hardware.

The register file is comprised of thirty-two 32-bit general purpose registers (GPR), which are accessed with three read ports and two write ports. During the decode stage, data is read out of the GPRs and fed to the execution unit. Likewise, during the write-back stage, results are written to the GPR. The use of the five ports on the register file enables either a load or a store operation to execute in parallel with an ALU operation.

Memory Management Unit (MMU)

The embedded PPC405 core has a 4 GB address space, which is presented as a flat address space.

The MMU provides address translation, protection functions, and storage attribute control for embedded applications. The MMU supports demand-paged virtual memory and other management schemes that require precise control of logical-to-physical address mapping and flexible

Figure 36, Figure 37, and Figure 38 illustrate various example configurations.

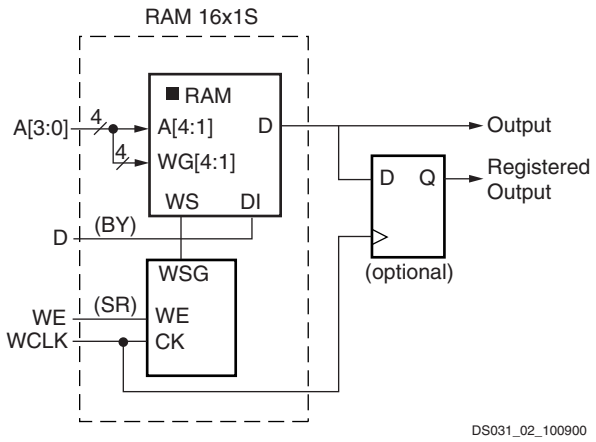

Figure 36: **Distributed SelectRAM+ (RAM16x1S)**

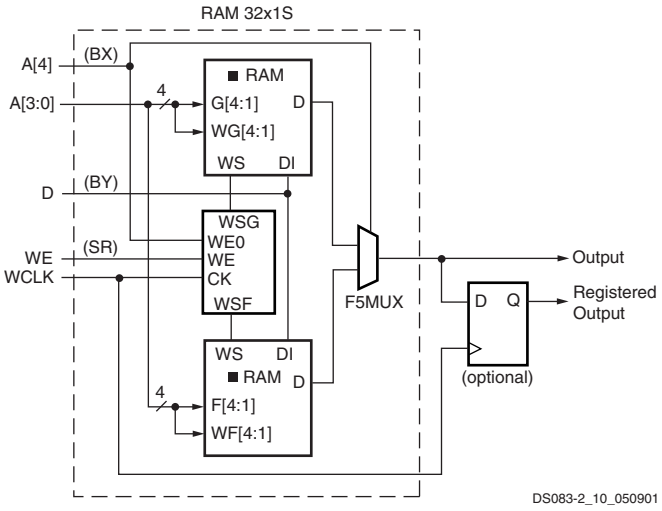

Figure 37: **Single-Port Distributed SelectRAM+ (RAM32x1S)**

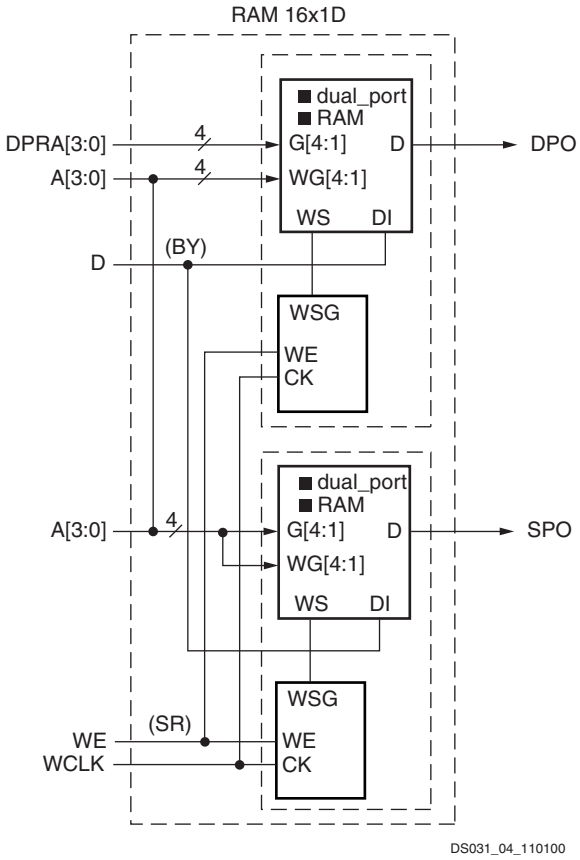

Figure 38: **Dual-Port Distributed SelectRAM+ (RAM16x1D)**

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 17 shows the number of LUTs occupied by each configuration.

Table 17: **ROM Configuration**

ROM	Number of LUTs
16 x 1	1
32 x 1	2
64 x 1	4
128 x 1	8 (1 CLB)
256 x 1	16 (2 CLBs)

Date	Version	Revision
03/24/03	2.5.1	• Table 10: Corrected I/O standard names SSTL18_I and SSTL18_II to SSTL18_I_DCI and SSTL18_II_DCI respectively. • Figure 61, text below: Corrected wording of criteria for clock switching.
05/27/03	2.6	• Removed Compatible Output Standards and Compatible Input Standards tables. • Added new Table 12, Summary of Voltage Supply Requirements for All Input and Output Standards. This table replaces deleted I/O standards tables. • Corrected sentence in section Input/Output Individual Options, page 27, to read “The optional weak-keeper circuit is connected to each *user I/O pad*.” • Added section Rules for Combining I/O Standards in the Same Bank, page 29.
06/02/03	2.7	• Added four Differential Termination I/O standards to Table 9 and Table 12. • Added section On-Chip Differential Termination and Figure 31, page 34.
08/25/03	2.7.1	• Added footnote referring to XAPP659 to 3.3V I/O callouts in Table 8 and Table 12.
09/10/03	2.8	• Section Configuration, page 56: Added text indicating that the mode pins M0-M2 must be held to a constant DC level during and after configuration.
10/14/03	2.9	• Deleted section Functional Description: RocketIO Multi-Gigabit Transceiver (MGT), page 10. Added section Local Clocking, page 51. • Sections Slave-Serial Mode and Master-Serial Mode, page 56: Changed "rising" to "falling" edge with respect to DOUT. • Table 8, page 24 and Table 10, page 25: Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Section BUFGMUX, page 50: Corrected the definition of the "presently selected clock" to be I0 or I1. Corrected signal names in Figure 61 and associated text from CLK0 and CLK1 to I0 and I1.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
04/22/04	3.2	• Section Clock De-skew, page 52: Removed reference to CLK2X as an option for DCM clock feedback.
06/30/04	4.0	Merged in DS110-2 (Module 2 of Virtex-II Pro X data sheet). Separate RocketIO and RocketIO X sections created.
11/17/04	4.1	• Figure 11, page 12: Corrected figure by removing coupling capacitors from input. • Section Rules for Combining I/O Standards in the Same Bank, page 29: Corrected I/O standard in the first example from LVDS_25_DCI to LVDS_25.
03/01/05	4.2	• Reassigned heading hierarchies for better agreement with content. • Table 7: Corrected VCCAUXTX and VCCAUXRX to AVCCAUXTX and AVCCAUXRX respectively. • Table 9: Corrected V_{OD} (output voltage) range for LVDSEXT_25. • Table 25: Corrected SelectRAM+ memory available for XC2VPX70 device. • Table 33: Updated configuration default bitstream lengths.
06/20/05	4.3	*No changes in Module 2 for this revision.*
09/15/05	4.4	• Table 1: Deleted SONET OC-192 protocol. • Table 3: Deleted RocketIO X primitives for SONET OC-192, 10 Gbit Ethernet, and Xilinx 10G (Aurora) protocols. • Changed all instances of 10.3125 Gb/s to 6.25 Gb/s. • Table 7: Changed RocketIO X VCCAUXRX from 1.5V globally to 1.5V for 8B/10B encoding, 1.8V for all other encoding protocols.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Virtex-II Pro X			Virtex-II Pro			Units
		Min	Typ	Max	Min	Typ	Max	
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	1.25			1.25			V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0			2.0			V
I_{REF}	V_{REF} current per pin			10			10	µA
I_L	Input or output leakage current per pin (sample-tested)			10			10	µA
C_{IN}	Input capacitance (sample-tested)			10			10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0V, V_{CCO} = 2.5V (sample tested)			150			150	µA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 2.5V (sample-tested)			150			150	µA
I_{BATT} (1)	Battery supply current	Note (2)			Note (2)			nA
$I_{CCAUXTX}$	Operating AVCCAUXTX supply current		115			60	105	mA
$I_{CCAUXRX}$	Operating AVCCAUXRX supply current		85			35	75	mA
I_{TTX}	Operating I_{TTX} supply current when transmitter is AC-coupled		55			30		mA
	Operating I_{TTX} supply current when transmitter is DC-coupled	N/A	N/A	N/A		15		mA
I_{TRX}	Operating I_{TRX} supply current when receiver is AC-coupled		15			0		mA
	Operating I_{TRX} supply current when receiver is DC-coupled	N/A	N/A	N/A		15		
P_{CPU}	Power dissipation of PowerPC™ 405 processor block		0.9			0.9		mW/ MHz
P_{RXTX} (3)	Power dissipation of MGT @ 1.25 Gb/s per channel	N/A	N/A	N/A		230		mW
	Power dissipation of MGT @ 2.5 Gb/s per channel		290			310		mW
	Power dissipation of MGT @ 3.125 Gb/s per channel		310			350		mW
	Power dissipation of MGT @ 4.25 Gb/s per channel		450		N/A	N/A	N/A	mW
	Power dissipation of MGT @ 6.25 Gb/s per channel		525		N/A	N/A	N/A	mW

Notes:

1. Characterized, not tested.
2. Battery supply current (I_{BATT}):

	Device Unpowered	Device Powered	Units
25°C:	< 50	< 10	nA
85°C:	N/A	< 10	nA

3. Total dissipation of fully operational PMA and PCS combined. This power is the average power supply dissipation per MGT. The averaging was done by simultaneously turning on all eight transceivers and dividing the total power supply dissipation by eight.

IOB Input Switching Characteristics Standard Adjustments

Table 36 gives all standard-specific data input delay adjustments.

Table 36: **IOB Input Switching Characteristics Standard Adjustments**

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-7	-6	-5	
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	T_{ILVTTL}	0.07	0.08	0.09	ns
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	$T_{ILVCMOS33}$	0.04	0.05	0.05	ns
LVCMOS, 2.5V	LVCMOS25	$T_{ILVCMOS25}$	0.00	0.00	0.00	ns
LVCMOS, 1.8V	LVCMOS18	$T_{ILVCMOS18}$	0.29	0.33	0.36	ns
LVCMOS, 1.5V	LVCMOS15	$T_{ILVCMOS15}$	0.36	0.41	0.45	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{ILVDS_25}	0.31	0.36	0.40	ns
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	$T_{ILVDSEXT\_25}$	0.33	0.37	0.41	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{IULVDS_25}	0.31	0.36	0.40	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{IBLVDS_25}	0.00	0.00	0.00	ns
LDT (HyperTransport), 2.5V	LDT_25	T_{ILDT_25}	0.31	0.36	0.40	ns
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	$T_{ILVPECL\_25}$	0.69	0.80	0.88	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{IPCI33_3}	0.14	0.16	0.18	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{IPCI66_3}	0.15	0.17	0.19	ns
PCI-X, 133 MHz, 3.3V	PCIX	T_{IPCIX}	0.12	0.13	0.15	ns
GTL (Gunning Transceiver Logic)	GTL	T_{IGTL}	0.59	0.68	0.74	ns
GTL Plus	GTLP	T_{IGTLP}	0.63	0.72	0.79	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{IHSTL_I}	0.59	0.68	0.75	ns
HSTL, Class II	HSTL_II	T_{IHSTL_II}	0.59	0.68	0.75	ns
HSTL, Class III	HSTL_III	T_{IHSTL_III}	0.57	0.66	0.72	ns
HSTL, Class IV	HSTL_IV	T_{IHSTL_IV}	0.58	0.67	0.74	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{IHSTL\_I\_18}$	0.57	0.65	0.72	ns
HSTL, Class II, 1.8V	HSTL_II_18	$T_{IHSTL\_II\_18}$	0.55	0.63	0.69	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{IHSTL\_III\_18}$	0.56	0.64	0.70	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{IHSTL\_IV\_18}$	0.57	0.65	0.71	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{ISSTL18\_I}$	0.62	0.72	0.79	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{ISSTL18\_II}$	0.64	0.73	0.81	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{ISSTL2_I}	0.62	0.72	0.79	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{ISSTL2_II}	0.64	0.73	0.81	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{ILVDCI_33}	–0.05	–0.05	–0.06	ns
LVDCI, 2.5V	LVDCI_25	T_{ILVDCI_25}	0.00	0.00	0.00	ns
LVDCI, 1.8V	LVDCI_18	T_{ILVDCI_18}	0.07	0.09	0.09	ns
LVDCI, 1.5V	LVDCI_15	T_{ILVDCI_15}	0.13	0.15	0.17	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{ILVDCI\_DV2\_25}$	0.00	0.00	0.00	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{ILVDCI\_DV2\_18}$	0.07	0.09	0.09	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{ILVDCI\_DV2\_15}$	0.13	0.15	0.17	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{IHSLVDCI\_15}$	0.59	0.68	0.75	ns

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. (See ***Virtex-II Pro Platform FPGA User Guide*** for details.) The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in Figure 6.

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. (IBIS models can be found on the web at **http://support.xilinx.com/support/sw_ibis.htm**.) Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 40.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Output Standard Adjustment value (Table 38) to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.

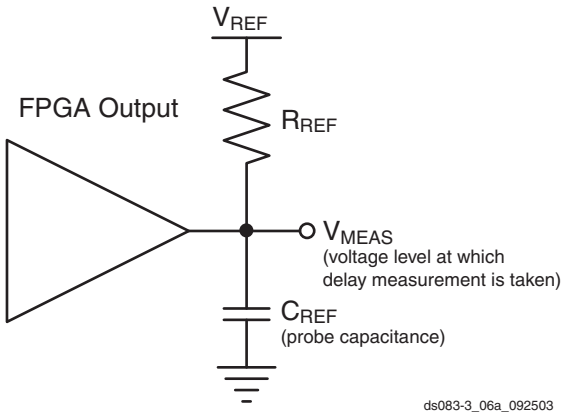

Figure 6: **Generalized Test Setup**

Table 40: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF} (1) (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.65	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	10 (2)	0.94	0
	PCI33_3 (falling edge)	25	10 (2)	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	10 (2)	0.94	0
	PCI66_3 (falling edge)	25	10 (2)	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	10 (3)	0.94	0
	PCIX (falling edge	25	10 (3)	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8

Virtex-II Pro Receiver Data-Valid Window (R_X)

R_X is the required minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$R_X = [TSAMP^{(1)} + TCKSKEW^{(2)} + TPKGSKEW^{(3)}]$$

Notes:

1. This parameter indicates the total sampling error of Virtex-II Pro DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter in a quiet system
   - Worst-case duty-cycle distortion
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
3. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/17/02	2.0	• Added new Virtex-II Pro family members. • Added timing parameters from speedsfile **v1.62**. • Added Table 46, Pipelined Multiplier Switching Characteristics. • Added 3.3V-vs-2.5V table entries for some parameters.
09/03/02	2.1	• Added Source-Synchronous Switching Characteristics section. • Added absolute max ratings for 3.3V-vs-2.5V parameters in Table 1. • Added recommended operating conditions for V_{IN} and RocketIO footnote to Table 2. • Updated SSTL2 values in Table 6. Added SSTL18 values: Table 6, Table 39, Table 32. [Table 32 removed in v2.8.] • Added Table 10, which contains LVPECL DC specifications.
09/27/02	2.2	Added section General Power Supply Requirements.
11/20/02	2.3	Updated parametric information in: • Table 1: Increase Absolute Max Rating for V_{CCO}, V_{REF}, V_{IN}, and V_{TS} from 3.6V to 3.75V. Delete cautionary footnotes related to voltage overshoot/undershoot. • Table 2: Delete V_{CCO} specifications for 2.5V and below operation. Delete footnote referencing special information for 3.3V operation. Add footnote for PCI/PCI-X. • Table 3: Add I_{BATT}. Delete I_L specifications for 2.5V and below operation. • Table 4: Add Typical Quiescent Supply Currents for XC2VP4 and XC2VP7 only • Table 6: Correct I_{OL} and I_{OH} for SSTL2 I. Add rows for LVTTL, LVCMOS33, and PCI-X. Correct max V_{IH} from V_{CCO} to 3.6V. • Table 7: Correct Min/Max V_{OD}, V_{OCM}, and V_{ICM} • Table 10: Reformat LVPECL DC Specifications to match Virtex-II data sheet format • Table 12: Correct parameter name from Differential Output Voltage to Single-Ended Output Voltage Swing. • Table 16: Add CPMC405CLOCK max frequencies • Table 27: Add footnote regarding serial data rate limitation in -5 part. • Table 39: Add rows for LVTTL, LVCMOS33, and PCI-X. • Table 32: Add LVTTL, LVCMOS33, and PCI-X. Correct all capacitive load values (except PCI/PCI-X) to 0 pF. [Table 32 removed in v2.8.] • Table 51: Correct CCLK max frequencies
11/25/02	2.4	Table 1: Correct lower limit of voltage range of V_{IN} and V_{TS} from –0.3V to –0.5V for 3.3V.

Date	Version	Revision
12/05/03 (cont'd)	3.0 (cont'd)	• Non-speedsfile parameter values added or updated: • Table 3: I_{BATT}. • Table 4: For XC2VP100, I_{CCINTQ}, I_{CCOQ}, and I_{CCAUXQ}. • Table 5: For XC2VP100, $I_{CCINTMIN}$. • Table 17: T_{CPWL} and T_{CPWH}. • Table 25: Added explanatory footnote to T_{RXLAT} (MGT receiver latency) max value. • Table 57: Added Footnote (3) regarding use of CLKIN_DIVIDE_BY_2 attribute.
02/19/04	3.1	• Updated time and frequency parameters as per speedsfile **v1.85**. • Table 2, Recommended Operating Conditions: Revised Footnotes (4) and (6). • Table 4, Quiescent Supply Current: Added Footnote (1) and updated Typical parameters. • Table 10, LVPECL DC Specifications: Added parameter values for Maximum Differential Input Voltage (LVPECL). • Table 14, Register-to-Register Performance: Removed reference to a number of designs for which test data is no longer provided. • Table 16, Processor Clocks Absolute AC Characteristics: Added Footnote (1) referring to XAPP755. • Added Table 41, Clock Distribution Switching Characteristics. • Revised section Configuration Timing, page 39 through page 41, and JTAG Test Access Port Switching Characteristics, page 42, with improved timing diagrams, parameter tables, and organization. • Table 50, Master/Slave Serial Mode Timing Characteristics, and Table 51, SelectMAP Mode Write Timing Characteristics: Added parameter $F_{CC\_STARTUP}$. • Table 51, SelectMAP Mode Write Timing Characteristics: Broke out T_{SMDCC}/T_{SMCCD}, DATA[0:7] setup/hold time, by device, and added new parameter specifications for XC2VP70 and XC2VP100 devices. • Table 57, Operating Frequency Ranges: Added callouts for existing Footnote (3) to the four CLKIN parameters. Added new Footnote (4) to the four CLKIN parameters. Added new Footnote (5) to CLK2X, CLK2X180. Added new Footnote (6) to CLK2X, CLK2X180; CLK0, CLK180; and CLKIN (using DLL outputs).
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
04/22/04	3.2	• Table 2, Recommended Operating Conditions: Corrected VTTX/VTRX lower voltage limit from 1.8V to 1.6V. • Table 5, Power-On Current for Virtex-II Pro Devices: Added Footnote (2) stating that listed I_{CCOMIN} values apply to the entire device (all banks). • Table 40, Output Delay Measurement Methodology: Corrected V_{MEAS} for LVTTL from 1.4V to 1.65V. • Table 57, Operating Frequency Ranges: Corrected CLKOUT_FREQ_1X_LF_MAX and CLKIN_FREQ_DLL_LF_MAX for -7 devices from 210 MHz to 270 MHz. • Table 65, Package Skew: Removed XC2VP40FF1517.
06/30/04	4.0	Merged in DS110-3 (Module 3 of Virtex-II Pro X data sheet). This merge added numerous previously unpublished RocketIO X MGT parameters. Specifications in this revision are from speedsfile **v1.86**.

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
N/A	VCCINT	U10			
N/A	VCCINT	U11			
N/A	VCCINT	U16			
N/A	VCCINT	U17			
N/A	VCCINT	U20			
N/A	VCCINT	V9			
N/A	VCCINT	V18			
N/A	VCCINT	Y10			
N/A	VCCINT	Y13			
N/A	VCCINT	Y14			
N/A	VCCINT	Y17			
N/A	VCCAUX	A2			
N/A	VCCAUX	A13			
N/A	VCCAUX	A14			
N/A	VCCAUX	A25			
N/A	VCCAUX	N1			
N/A	VCCAUX	N26			
N/A	VCCAUX	P1			
N/A	VCCAUX	P26			
N/A	VCCAUX	AF2			
N/A	VCCAUX	AF13			
N/A	VCCAUX	AF14			
N/A	VCCAUX	AF25			
N/A	GND	A1			
N/A	GND	A26			
N/A	GND	B2			
N/A	GND	B25			
N/A	GND	C3			
N/A	GND	C24			
N/A	GND	D4			
N/A	GND	D8			
N/A	GND	D19			
N/A	GND	D23			
N/A	GND	F10			
N/A	GND	F17			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	IO_L87N_7	M25			
7	IO_L86P_7	M24			
7	IO_L86N_7	M23			
7	IO_L85P_7	M22			
7	IO_L85N_7	M21			
7	IO_L60P_7	N19	NC		
7	IO_L60N_7	M19	NC		
7	IO_L59P_7	L26	NC		
7	IO_L59N_7	L25	NC		
7	IO_L58P_7	L24	NC		
7	IO_L58N_7/VREF_7	L23	NC		
7	IO_L57P_7	L22	NC		
7	IO_L57N_7	L21	NC		
7	IO_L56P_7	M20	NC		
7	IO_L56N_7	L20	NC		
7	IO_L55P_7	L19	NC		
7	IO_L55N_7	K20	NC		
7	IO_L54P_7	K26	NC		
7	IO_L54N_7	J26	NC		
7	IO_L53P_7	K24	NC		
7	IO_L53N_7	K23	NC		
7	IO_L52P_7	K22	NC		
7	IO_L52N_7/VREF_7	K21	NC		
7	IO_L51P_7	J25	NC		
7	IO_L51N_7	J24	NC		
7	IO_L50P_7	J23	NC		
7	IO_L50N_7	J22	NC		
7	IO_L49P_7	J21	NC		
7	IO_L49N_7	J20	NC		
7	IO_L48P_7	H26	NC		
7	IO_L48N_7	H25	NC		
7	IO_L47P_7	H24	NC		
7	IO_L47N_7	H23	NC		
7	IO_L46P_7	H22	NC		
7	IO_L46N_7/VREF_7	H21	NC		
7	IO_L45P_7	G26	NC		
7	IO_L45N_7	F26	NC		

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
1	IO_L75N_1/GCLK3P	C17		
1	IO_L75P_1/GCLK2S	B17		
1	IO_L74N_1/GCLK1P	L17		
1	IO_L74P_1/GCLK0S	K17		
1	IO_L73N_1	E17		
1	IO_L73P_1	D17		
1	IO_L69N_1/VREF_1	G17		
1	IO_L69P_1	F17		
1	IO_L68N_1	J17		
1	IO_L68P_1	H17		
1	IO_L67N_1	C16		
1	IO_L67P_1	B16		
1	IO_L66N_1/VREF_1	G16	NC	
1	IO_L66P_1	F16	NC	
1	IO_L57N_1/VREF_1	B15		
1	IO_L57P_1	A15		
1	IO_L56N_1	L16		
1	IO_L56P_1	K16		
1	IO_L55N_1	D16		
1	IO_L55P_1	C15		
1	IO_L54N_1	F15		
1	IO_L54P_1	E15		
1	IO_L53_1/No_Pair	H16		
1	IO_L50_1/No_Pair	G15		
1	IO_L49N_1	B14		
1	IO_L49P_1	A14		
1	IO_L48N_1	D14		
1	IO_L48P_1	C14		
1	IO_L47N_1	L15		
1	IO_L47P_1	K15		
1	IO_L46N_1	F14		
1	IO_L46P_1	E14		
1	IO_L45N_1/VREF_1	H14		
1	IO_L45P_1	G14		
1	IO_L44N_1	L14		
1	IO_L44P_1	K14		
1	IO_L43N_1	C13		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
0	IO_L34P_0	E27	NC	
0	IO_L35N_0	L26	NC	
0	IO_L35P_0	L25	NC	
0	IO_L36N_0	G26	NC	
0	IO_L36P_0/VREF_0	H26	NC	
0	IO_L37N_0	E26		
0	IO_L37P_0	F26		
0	IO_L38N_0	K25		
0	IO_L38P_0	K24		
0	IO_L39N_0	C26		
0	IO_L39P_0	D26		
0	IO_L43N_0	H25		
0	IO_L43P_0	J25		
0	IO_L44N_0	M25		
0	IO_L44P_0	M24		
0	IO_L45N_0	F25		
0	IO_L45P_0/VREF_0	G25		
0	IO_L46N_0	C25		
0	IO_L46P_0	D25		
0	IO_L47N_0	L23		
0	IO_L47P_0	M22		
0	IO_L48N_0	H24		
0	IO_L48P_0	J24		
0	IO_L49N_0	E25		
0	IO_L49P_0	E24		
0	IO_L50_0/No_Pair	N23		
0	IO_L53_0/No_Pair	M23		
0	IO_L54N_0	H23		
0	IO_L54P_0	J23		
0	IO_L55N_0	F24		
0	IO_L55P_0	G23		
0	IO_L56N_0	K22		
0	IO_L56P_0	L22		
0	IO_L57N_0	C23		
0	IO_L57P_0/VREF_0	D23		
0	IO_L58N_0	H22		
0	IO_L58P_0	J22		
0	IO_L59N_0	N22		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L30N_2	N6		
2	IO_L30P_2	N7		
2	IO_L31N_2	M4		
2	IO_L31P_2	N5		
2	IO_L32N_2	R11		
2	IO_L32P_2	R12		
2	IO_L33N_2	N1		
2	IO_L33P_2	N2		
2	IO_L34N_2/VREF_2	P6		
2	IO_L34P_2	P7		
2	IO_L35N_2	R13		
2	IO_L35P_2	T13		
2	IO_L36N_2	P4		
2	IO_L36P_2	P5		
2	IO_L37N_2	P3		
2	IO_L37P_2	N3		
2	IO_L38N_2	T10		
2	IO_L38P_2	T11		
2	IO_L39N_2	P1		
2	IO_L39P_2	P2		
2	IO_L40N_2/VREF_2	R7		
2	IO_L40P_2	R8		
2	IO_L41N_2	T12		
2	IO_L41P_2	U12		
2	IO_L42N_2	R5		
2	IO_L42P_2	R6		
2	IO_L43N_2	R3		
2	IO_L43P_2	R4		
2	IO_L44N_2	U8		
2	IO_L44P_2	T8		
2	IO_L45N_2	R1		
2	IO_L45P_2	R2		
2	IO_L46N_2/VREF_2	T6		
2	IO_L46P_2	T7		
2	IO_L47N_2	U9		
2	IO_L47P_2	U10		
2	IO_L48N_2	T2		
2	IO_L48P_2	T3		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
7	IO_L86N_7	W28		
7	IO_L85P_7	W34		
7	IO_L85N_7	W35		
7	IO_L60P_7	W32		
7	IO_L60N_7	W33		
7	IO_L59P_7	W29		
7	IO_L59N_7	W30		
7	IO_L58P_7	V38		
7	IO_L58N_7/VREF_7	V39		
7	IO_L57P_7	V36		
7	IO_L57N_7	V37		
7	IO_L56P_7	V28		
7	IO_L56N_7	V29		
7	IO_L55P_7	V34		
7	IO_L55N_7	V35		
7	IO_L54P_7	V32		
7	IO_L54N_7	V33		
7	IO_L53P_7	V30		
7	IO_L53N_7	V31		
7	IO_L52P_7	U38		
7	IO_L52N_7/VREF_7	U39		
7	IO_L51P_7	T36		
7	IO_L51N_7	U36		
7	IO_L50P_7	V27		
7	IO_L50N_7	U27		
7	IO_L49P_7	U34		
7	IO_L49N_7	U35		
7	IO_L48P_7	T37		
7	IO_L48N_7	T38		
7	IO_L47P_7	U30		
7	IO_L47N_7	U31		
7	IO_L46P_7	T33		
7	IO_L46N_7/VREF_7	T34		
7	IO_L45P_7	R38		
7	IO_L45N_7	R39		
7	IO_L44P_7	T32		
7	IO_L44N_7	U32		
7	IO_L43P_7	R36		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	VCCAUX	AP6		
N/A	VCCAUX	F6		
N/A	VCCAUX	AR5		
N/A	VCCAUX	E5		
N/A	VCCAUX	AW2		
N/A	VCCAUX	Y2		
N/A	VCCAUX	A2		
N/A	VCCAUX	AV1		
N/A	VCCAUX	AA1		
N/A	VCCAUX	Y1		
N/A	VCCAUX	W1		
N/A	VCCAUX	B1		
N/A	GND	A3		
N/A	GND	AV2		
N/A	GND	AU2		
N/A	GND	AA2		
N/A	GND	W2		
N/A	GND	C2		
N/A	GND	B2		
N/A	GND	AU1		
N/A	GND	AM1		
N/A	GND	AH1		
N/A	GND	AD1		
N/A	GND	T1		
N/A	GND	M1		
N/A	GND	H1		
N/A	GND	C1		
N/A	GND	AD5		
N/A	GND	T5		
N/A	GND	M5		
N/A	GND	H5		
N/A	GND	AU4		
N/A	GND	AT4		
N/A	GND	D4		
N/A	GND	C4		
N/A	GND	AW3		
N/A	GND	AV3		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		V6		
N/A	GND		U25		
N/A	GND		U24		
N/A	GND		U23		
N/A	GND		U22		
N/A	GND		U21		
N/A	GND		U20		
N/A	GND		U19		
N/A	GND		U18		
N/A	GND		T42		
N/A	GND		T1		
N/A	GND		R39		
N/A	GND		R36		
N/A	GND		R7		
N/A	GND		R4		
N/A	GND		M42		
N/A	GND		M1		
N/A	GND		L22		
N/A	GND		L21		
N/A	GND		K39		
N/A	GND		K4		
N/A	GND		J34		
N/A	GND		J9		
N/A	GND		H42		
N/A	GND		H35		
N/A	GND		H22		
N/A	GND		H21		
N/A	GND		H8		
N/A	GND		H1		
N/A	GND		G36		
N/A	GND		G7		
N/A	GND		F37		
N/A	GND		F25		
N/A	GND		F18		
N/A	GND		F6		
N/A	GND		E38		

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
5	IO_L10N_5	AW27	NC
5	IO_L10P_5	AW26	NC
5	IO_L45N_5/VREF_5	AN27	
5	IO_L45P_5	AP27	
5	IO_L44N_5	AU27	
5	IO_L44P_5	AV27	
5	IO_L43N_5	AR27	
5	IO_L43P_5	AR26	
5	IO_L39N_5	AL27	
5	IO_L39P_5	AM27	
5	IO_L38N_5	BA28	
5	IO_L38P_5	BB28	
5	IO_L37N_5	AY28	
5	IO_L37P_5	AY27	
5	IO_L87N_5/VREF_5	AN28	
5	IO_L87P_5	AP28	
5	IO_L86N_5	AU28	
5	IO_L86P_5	AV28	
5	IO_L85N_5	AT28	
5	IO_L85P_5	AT27	
5	IO_L84N_5	AL28	
5	IO_L84P_5	AM28	
5	IO_L83_5/No_Pair	BA29	
5	IO_L80_5/No_Pair	BB29	
5	IO_L79N_5	AY29	
5	IO_L79P_5	AW28	
5	IO_L78N_5	AN29	
5	IO_L78P_5	AP29	
5	IO_L77N_5	AU29	
5	IO_L77P_5	AV29	
5	IO_L76N_5	AT29	
5	IO_L76P_5	AR28	
5	IO_L36N_5/VREF_5	AL29	
5	IO_L36P_5	AM29	
5	IO_L35N_5	AY30	
5	IO_L35P_5	BA30	
5	IO_L34N_5	AT30	

Table 14: **FF1696 — XC2VP100**

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
N/A	GND	AD19	
N/A	GND	AC19	
N/A	GND	AB19	
N/A	GND	AA19	
N/A	GND	Y19	
N/A	GND	W19	
N/A	GND	V19	
N/A	GND	U19	
N/A	GND	M19	
N/A	GND	AF18	
N/A	GND	AE18	
N/A	GND	AD18	
N/A	GND	AC18	
N/A	GND	AB18	
N/A	GND	AA18	
N/A	GND	Y18	
N/A	GND	W18	
N/A	GND	V18	
N/A	GND	U18	
N/A	GND	BB17	
N/A	GND	AV17	
N/A	GND	AP17	
N/A	GND	AE17	
N/A	GND	AD17	
N/A	GND	AC17	
N/A	GND	AB17	
N/A	GND	AA17	
N/A	GND	Y17	
N/A	GND	W17	
N/A	GND	V17	
N/A	GND	J17	
N/A	GND	E17	
N/A	GND	A17	
N/A	GND	BB13	
N/A	GND	AV13	
N/A	GND	AP13	
N/A	GND	J13	