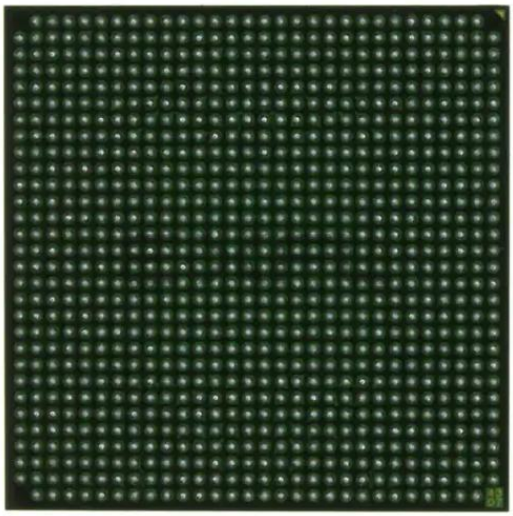


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3424
Number of Logic Elements/Cells	30816
Total RAM Bits	2506752
Number of I/O	556
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp30-6ff896i

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/13/02	2.0	New Virtex-II Pro family members. New timing parameters per speedsfile **v1.62**.
09/03/02	2.1	Updates to Table 1 and Table 3. Processor Block information added to Table 4.
09/27/02	2.2	In Table 1, correct max number of XC2VP30 I/Os to 644.
11/20/02	2.3	Add bullet items for 3.3V I/O features.
01/20/03	2.4	• In Table 3, add FG676 package option for XC2VP20, XC2VP30, and XC2VP40. • Remove FF1517 package option for XC2VP40.
03/24/03	2.4.1	• Correct number of single-ended I/O standards from 19 to 22. • Correct minimum RocketIO serial speed from 622 Mbps to 600 Mbps.
08/25/03	2.4.2	• Add footnote referring to XAPP659 to callout for 3.3V I/O standards on page 4.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Table 1: Corrected number of RocketIO transceiver blocks for XC2VP40. • Section Virtex-II Pro Platform FPGA Technology (All Devices): Updated number of differential standards supported from six to ten. • Section Input/Output Blocks (IOBs): Added text stating that differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards. • Figure 1: Added note stating that -7 devices are not available in Industrial grade.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/30/04	4.0	Merged in DS110-1 (Module 1 of Virtex-II Pro X data sheet). Added information on available Pb-free packages.
11/17/04	4.1	*No changes in Module 1 for this revision.*
03/01/05	4.2	Table 3: Corrected number of RocketIO transceivers for XC2VP7-FG456.
06/20/05	4.3	*No changes in Module 1 for this revision.*
09/15/05	4.4	• Changed all instances of 10.3125 Gb/s (RocketIO transceiver maximum bit rate) to 6.25 Gb/s. • Changed all instances of 412.5 Gb/s (RocketIO X transceiver maximum multi-channel raw data transfer rate) to 250 Gb/s.
10/10/05	4.5	• Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s. • Changed maximum performance for -7 Virtex-II Pro X MGT (Table 4) to N/A.
03/05/07	4.6	*No changes in Module 1 for this revision.*
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added *Product Not Recommended for New Designs* banner.

Table 11: **LVCMOS Programmable Currents (Sink and Source)**

SelectIO-Ultra	Programmable Current (Worst-Case Guaranteed Minimum)						
LVTTL	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS33	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS25	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVCMOS18	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a
LVCMOS15	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a

Figure 23 shows the SSTL2, SSTL18, and HSTL configurations. HSTL can sink current up to 48 mA. (HSTL IV)

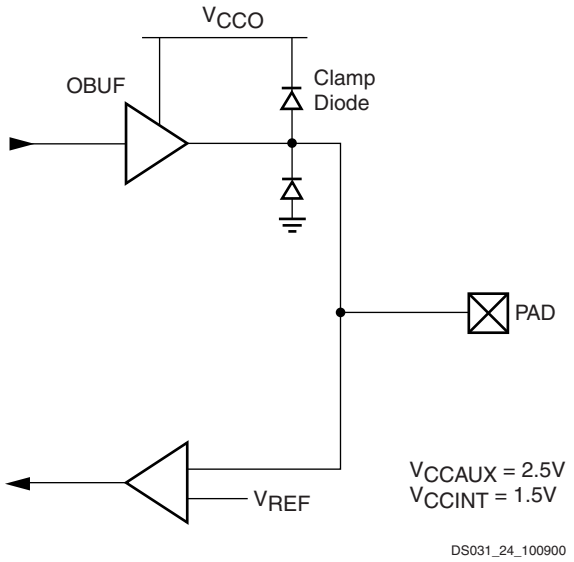


Figure 23: **SSTL or HSTL SelectIO-Ultra Standards**

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Virtex-II Pro uses two memory cells to control the configuration of an I/O as an input. This is to reduce the probability of an I/O configured as an input from flipping to an output when subjected to a single event upset (SEU) in space applications.

Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP_EN controls the pull-up resistors prior to configuration. By default, HSWAP_EN is set High, which disables the pull-up resistors on user I/O pins. When HSWAP_EN is set Low, the pull-up resistors are activated on user I/O pins.

All Virtex-II Pro IOBs (except RocketIO transceiver pins) support IEEE 1149.1 and IEEE 1532 compatible Boundary-Scan testing.

Input Path

The Virtex-II Pro IOB input path routes input signals directly to internal logic and / or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II Pro device, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in the same bank. See I/O banking description.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and / or the 3-state signal can be routed to the buffer directly from the internal logic or through an output / 3-state flip-flop or latch, or through the DDR output / 3-state registers.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in the same bank. See I/O banking description.

I/O Banking

Some of the I/O standards described above require V_{CCO} and V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOB blocks, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 24 and Figure 25. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 39. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous; however, the storage element or flip-flop is available to implement a synchronous read. Any of the 16 bits can be read out asynchronously by varying the address. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

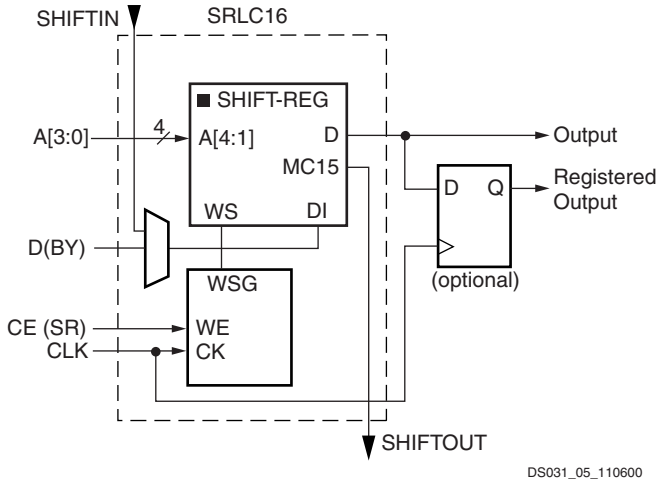


Figure 39: **Shift Register Configurations**

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See Figure 40.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

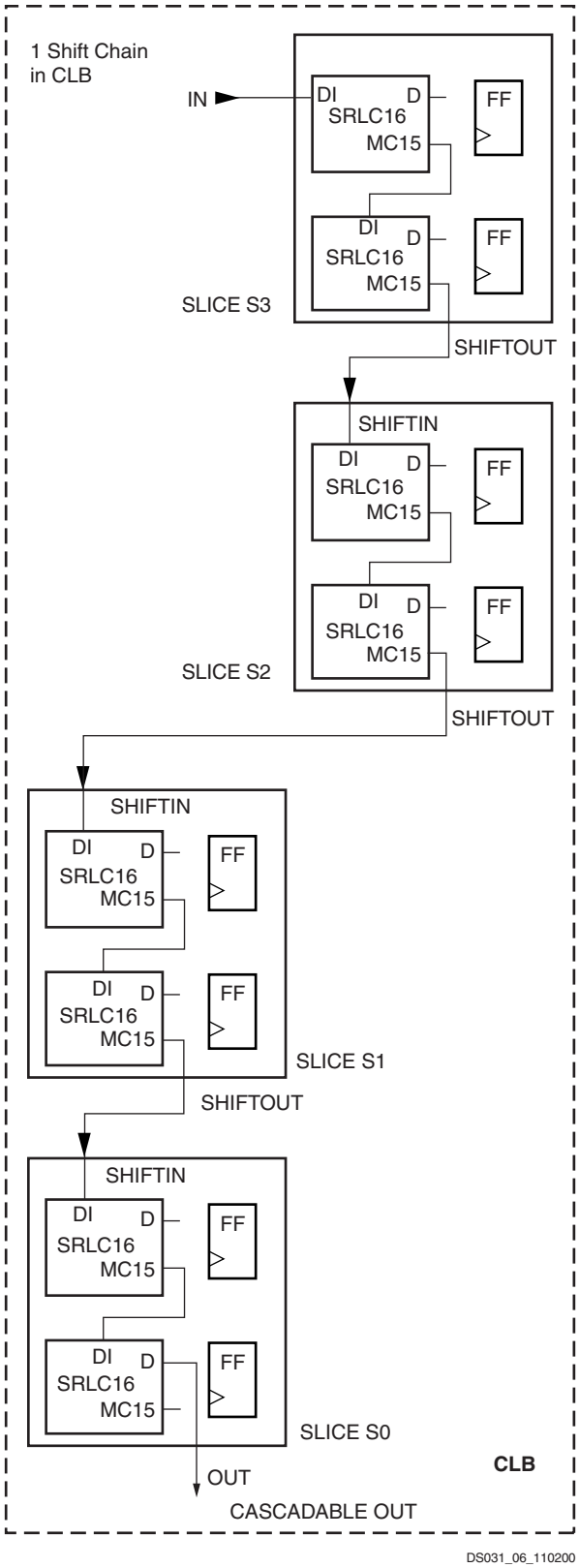


Figure 40: **Cascadable Shift Register**

Multiplexers

Virtex-II Pro function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II Pro slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in Figure 41. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II Pro Platform FPGA User Guide*. Any LUT can implement a 2:1 multiplexer.

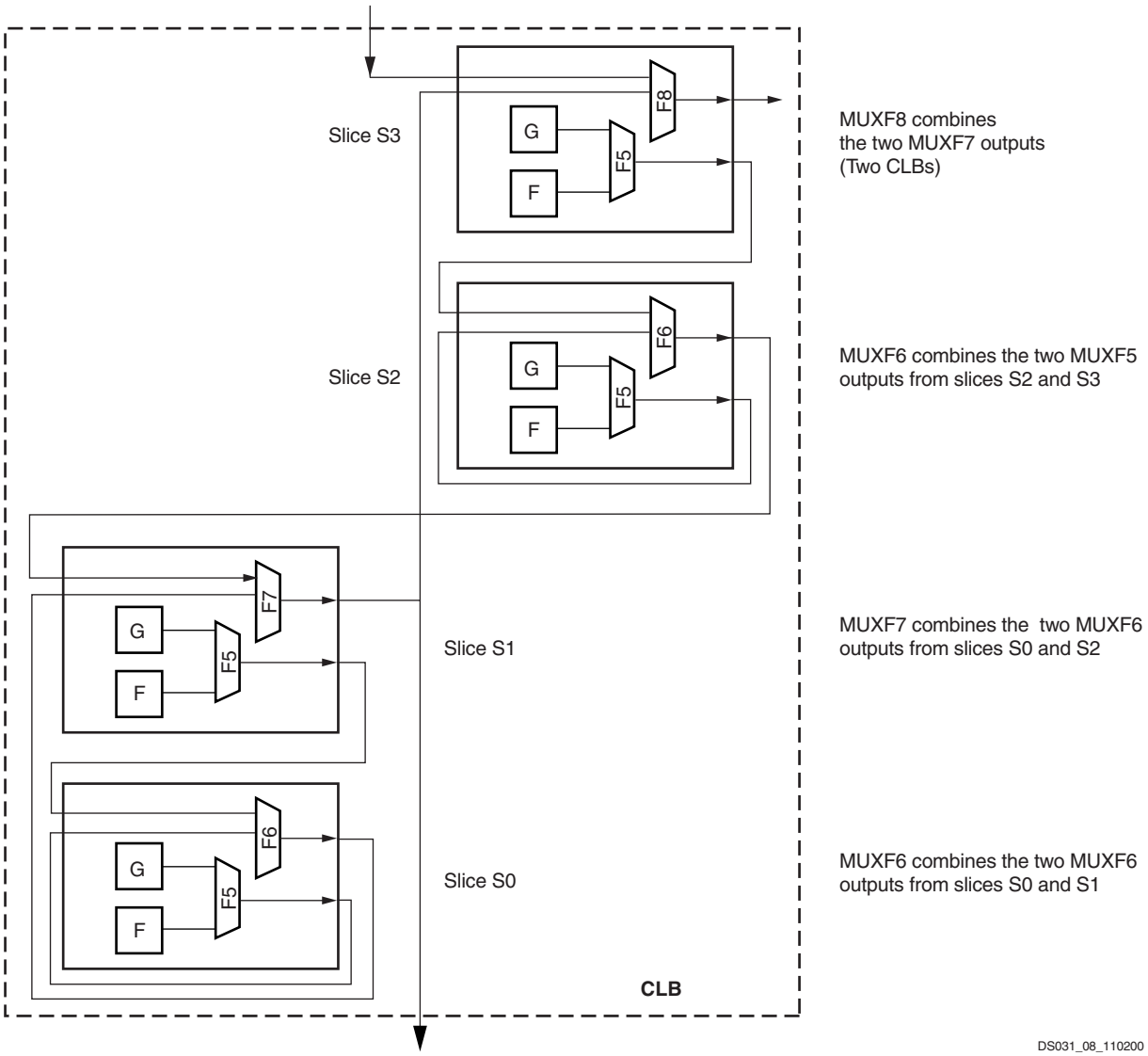


Figure 41: **MUXF5 and MUXFX multiplexers**

Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II Pro CLB has two separate carry chains, as shown in the Figure 42.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II Pro device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 34) improves the efficiency of multiplier implementation.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVCMOS 2.5V levels. For other standards, adjust the delays with the values shown in IOB Input Switching Characteristics Standard Adjustments.

Table 35: **IOB Input Switching Characteristics**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Propagation Delays						
Pad to I output, no delay	T_{IOPI}	All	0.84	0.87	0.91	ns, max
Pad to I output, with delay	T_{IOPID}	XC2VP2	1.84	1.94	2.06	ns, max
		XC2VP4	1.84	1.94	2.06	ns, max
		XC2VP7	1.84	1.94	2.06	ns, max
		XC2VP20	2.14	2.23	2.37	ns, max
		XC2VPX20	2.14	2.23	2.37	ns, max
		XC2VP30	2.14	2.26	2.46	ns, max
		XC2VP40	2.54	2.67	2.81	ns, max
		XC2VP50	2.54	2.68	2.87	ns, max
		XC2VP70	2.54	2.72	2.91	ns, max
		XC2VPX70	2.54	2.72	2.91	ns, max
		XC2VP100	N/A	4.71	4.80	ns, max
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.86	0.89	0.93	ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XC2VP2	2.30	2.62	2.97	ns, max
		XC2VP4	2.57	2.89	3.23	ns, max
		XC2VP7	2.50	2.84	3.17	ns, max
		XC2VP20	2.65	3.04	3.42	ns, max
		XC2VPX20	2.65	3.04	3.42	ns, max
		XC2VP30	2.69	3.12	3.51	ns, max
		XC2VP40	3.30	3.63	4.03	ns, max
		XC2VP50	3.86	4.10	4.45	ns, max
		XC2VP70	4.00	4.25	4.57	ns, max
		XC2VPX70	4.00	4.25	4.57	ns, max
		XC2VP100	N/A	6.50	7.06	ns, max
Clock CLK to output IQ	T_{IOCKIQ}	All	0.60	0.60	0.67	ns, max

Virtex-II Pro Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM

Table 55: **Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**-7**	**-6**	**-5**	**Units**
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1) For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 25.						
No Delay Global Clock and IFF(2) with DCM	T_{PSDCM}/T_{PHDCM}	XC2VP2	1.54/–0.58	1.54/–0.57	1.54/–0.56	ns
		XC2VP4	1.59/–0.59	1.59/–0.58	1.59/–0.57	ns
		XC2VP7	1.66/–0.61	1.66/–0.59	1.66/–0.57	ns
		XC2VP20	1.68/–0.53	1.68/–0.53	1.68/–0.50	ns
		XC2VPX20	1.68/–0.53	1.68/–0.53	1.68/–0.50	ns
		XC2VP30	1.81/–0.74	1.81/–0.74	1.81/–0.71	ns
		XC2VP40	1.85/–0.65	1.85/–0.64	1.85/–0.60	ns
		XC2VP50	1.85/–0.57	1.85/–0.54	1.85/–0.50	ns
		XC2VP70	1.86/–0.45	1.86/–0.39	1.86/–0.30	ns
		XC2VPX70	1.86/–0.45	1.86/–0.39	1.86/–0.30	ns
		XC2VP100	N/A	1.86/–0.35	1.87/–0.28	ns

Notes:

1. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case duty-cycle distortion using CLK0 and CLK180, T_{DCD_CLK180}.
3. IFF = Input Flip-Flop or Latch

Input Clock Tolerances

Table 58: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			–7		–6		–5		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/High Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz	25.00		25.00		25.00		ns
PSCLK and CLKIN(3)	PSCLK_PULSE and CLKIN_PULSE	1 – 10 MHz	25.00		25.00		25.00		ns
		10 – 25 MHz	10.00		10.00		10.00		ns
		25 – 50 MHz	5.00		5.00		5.00		ns
		50 – 100 MHz	3.00		3.00		3.00		ns
		100 – 150 MHz	2.40		2.40		2.40		ns
		150 – 200 MHz	2.00		2.00		2.00		ns
		200 – 250 MHz	1.80		1.80		1.80		ns
		250 – 300 MHz	1.50		1.50		1.50		ns
		300 – 350 MHz	1.30		1.30		1.30		ns
		350 – 400 MHz	1.15		1.15		1.15		ns
		> 400 MHz	1.05		1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_LF			±300		±300		±300	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_LF			±300		±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_HF			±150		±150		±150	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_HF			±150		±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_LF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_LF			±1		±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_HF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_HF			±1		±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT			±1		±1		±1	ns

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	AVCCAUXTX18	AA14			
N/A	AVCCAUXRX19	AA10			
N/A	VTRXPAD19	AA9			
N/A	RXNPAD19	AB10			
N/A	RXPPAD19	AB9			
N/A	GNDA19	Y9			
N/A	TXPPAD19	AB8			
N/A	TXNPAD19	AB7			
N/A	VTTXPAD19	AA7			
N/A	AVCCAUXTX19	AA8			
N/A	AVCCAUXRX21	AA6	NC	NC	
N/A	VTRXPAD21	AA5	NC	NC	
N/A	RXNPAD21	AB6	NC	NC	
N/A	RXPPAD21	AB5	NC	NC	
N/A	GNDA21	Y6	NC	NC	
N/A	TXPPAD21	AB4	NC	NC	
N/A	TXNPAD21	AB3	NC	NC	
N/A	VTTXPAD21	AA3	NC	NC	
N/A	AVCCAUXTX21	AA4	NC	NC	
N/A	VCCINT	U6			
N/A	VCCINT	U17			
N/A	VCCINT	T8			
N/A	VCCINT	T7			
N/A	VCCINT	T16			
N/A	VCCINT	T15			
N/A	VCCINT	R7			
N/A	VCCINT	R16			
N/A	VCCINT	H7			
N/A	VCCINT	H16			
N/A	VCCINT	G8			
N/A	VCCINT	G7			
N/A	VCCINT	G16			
N/A	VCCINT	G15			
N/A	VCCINT	F6			
N/A	VCCINT	F17			
N/A	VCCAUX	M22			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	VCCO_7	L18			
7	VCCO_7	M18			
7	VCCO_7	N18			
N/A	CCLK	W7			
N/A	PROG_B	D22			
N/A	DONE	AB6			
N/A	M0	AC22			
N/A	M1	W20			
N/A	M2	AB21			
N/A	TCK	G8			
N/A	TDI	H20			
N/A	TDO	H7			
N/A	TMS	F7			
N/A	PWRDWN_B	AC5			
N/A	HSWAP_EN	E21			
N/A	RSVD	D5			
N/A	VBATT	E6			
N/A	DXP	F20			
N/A	DXN	G19			
N/A	AVCCAUXTX7	B11			
N/A	VTTXPAD7	B12			
N/A	TXNPAD7	A12			
N/A	TXPPAD7	A11			
N/A	GNDA7	C11			
N/A	RXPPAD7	A10			
N/A	RXNPAD7	A9			
N/A	VTRXPAD7	B10			
N/A	AVCCAUXRX7	B9			
N/A	AVCCAUXTX9	B6	NC	NC	
N/A	VTTXPAD9	B7	NC	NC	
N/A	TXNPAD9	A7	NC	NC	
N/A	TXPPAD9	A6	NC	NC	
N/A	GNDA9	C5	NC	NC	
N/A	RXPPAD9	A5	NC	NC	
N/A	RXNPAD9	A4	NC	NC	
N/A	VTRXPAD9	B5	NC	NC	

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
7	IO_L54N_7		L26			
7	IO_L53P_7		N26			
7	IO_L53N_7		N25			
7	IO_L52P_7		M30			
7	IO_L52N_7/VREF_7		L30			
7	IO_L51P_7		K28			
7	IO_L51N_7		K27			
7	IO_L50P_7		N24			
7	IO_L50N_7		N23			
7	IO_L49P_7		L29			
7	IO_L49N_7		K29			
7	IO_L48P_7		J28			
7	IO_L48N_7		J27			
7	IO_L47P_7		M26			
7	IO_L47N_7		M25			
7	IO_L46P_7		K30			
7	IO_L46N_7/VREF_7		J30			
7	IO_L45P_7		K26			
7	IO_L45N_7		K25			
7	IO_L44P_7		M24			
7	IO_L44N_7		M23			
7	IO_L43P_7		J29			
7	IO_L43N_7		H29			
7	IO_L42P_7		H28	NC		
7	IO_L42N_7		H27	NC		
7	IO_L41P_7		L24	NC		
7	IO_L41N_7		L23	NC		
7	IO_L40P_7		G30	NC		
7	IO_L40N_7/VREF_7		G29	NC		
7	IO_L39P_7		G28	NC		
7	IO_L39N_7		G27	NC		
7	IO_L38P_7		J26	NC		
7	IO_L38N_7		J25	NC		
7	IO_L37P_7		F30	NC		
7	IO_L37N_7		F29	NC		
7	IO_L36P_7		F28	NC		

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	GND		N17			
N/A	GND		N16			
N/A	GND		N15			
N/A	GND		N14			
N/A	GND		N13			
N/A	GND		N12			
N/A	GND		M19			
N/A	GND		M18			
N/A	GND		M17			
N/A	GND		M16			
N/A	GND		M15			
N/A	GND		M14			
N/A	GND		M13			
N/A	GND		M12			
N/A	GND		L28			
N/A	GND		L25			
N/A	GND		L20			
N/A	GND		L11			
N/A	GND		L6			
N/A	GND		L3			
N/A	GND		H30			
N/A	GND		H1			
N/A	GND		F25			
N/A	GND		F18			
N/A	GND		F13			
N/A	GND		F6			
N/A	GND		E26			
N/A	GND		E5			
N/A	GND		D27			
N/A	GND		D22			
N/A	GND		D19			
N/A	GND		D12			
N/A	GND		D9			
N/A	GND		D4			
N/A	GND		C28			
N/A	GND		C17			

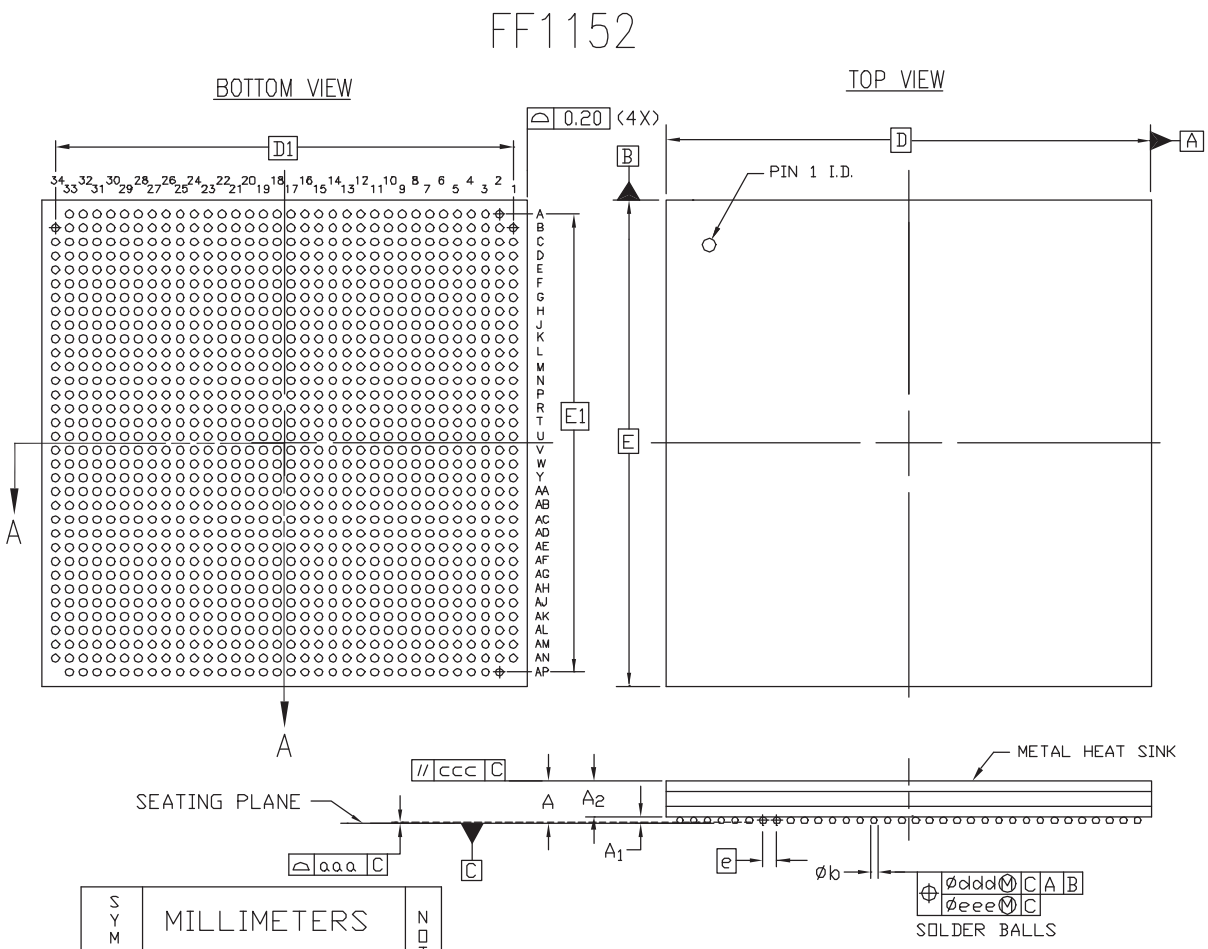
Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
7	IO_L86N_7	U25				
7	IO_L85P_7	T32				
7	IO_L85N_7	T31				
7	IO_L60P_7	T30				
7	IO_L60N_7	T29				
7	IO_L59P_7	T28				
7	IO_L59N_7	T27				
7	IO_L58P_7	T33				
7	IO_L58N_7/VREF_7	R33				
7	IO_L57P_7	R32				
7	IO_L57N_7	R31				
7	IO_L56P_7	T26				
7	IO_L56N_7	T25				
7	IO_L55P_7	R34				
7	IO_L55N_7	P34				
7	IO_L54P_7	R29				
7	IO_L54N_7	R28				
7	IO_L53P_7	U24				
7	IO_L53N_7	T24				
7	IO_L52P_7	P32				
7	IO_L52N_7/VREF_7	P31				
7	IO_L51P_7	P30				
7	IO_L51N_7	P29				
7	IO_L50P_7	R26				
7	IO_L50N_7	R25				
7	IO_L49P_7	P33				
7	IO_L49N_7	N33				
7	IO_L48P_7	N32				
7	IO_L48N_7	N31				
7	IO_L47P_7	P28				
7	IO_L47N_7	P27				
7	IO_L46P_7	N34				
7	IO_L46N_7/VREF_7	M34				
7	IO_L45P_7	N30				
7	IO_L45N_7	N29				
7	IO_L44P_7	P26				
7	IO_L44N_7	P25				
7	IO_L43P_7	M32				

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	TXPPAD9	A8				
N/A	GNDA9	C8				
N/A	RXPPAD9	A7				
N/A	RXNPAD9	A6				
N/A	VTRXPAD9	B7				
N/A	AVCCAUXRX9	B6				
N/A	AVCCAUXTX11	B4	NC	NC		
N/A	VTTXPAD11	B5	NC	NC		
N/A	TXNPAD11	A5	NC	NC		
N/A	TXPPAD11	A4	NC	NC		
N/A	GNDA11	C5	NC	NC		
N/A	RXPPAD11	A3	NC	NC		
N/A	RXNPAD11	A2	NC	NC		
N/A	VTRXPAD11	B3	NC	NC		
N/A	AVCCAUXRX11	B2	NC	NC		
N/A	AVCCAUXRX14	AN2	NC	NC		
N/A	VTRXPAD14	AN3	NC	NC		
N/A	RXNPAD14	AP2	NC	NC		
N/A	RXPPAD14	AP3	NC	NC		
N/A	GNDA14	AM5	NC	NC		
N/A	TXPPAD14	AP4	NC	NC		
N/A	TXNPAD14	AP5	NC	NC		
N/A	VTTXPAD14	AN5	NC	NC		
N/A	AVCCAUXTX14	AN4	NC	NC		
N/A	AVCCAUXRX16	AN6				
N/A	VTRXPAD16	AN7				
N/A	RXNPAD16	AP6				
N/A	RXPPAD16	AP7				
N/A	GNDA16	AM8				
N/A	TXPPAD16	AP8				
N/A	TXNPAD16	AP9				
N/A	VTTXPAD16	AN9				
N/A	AVCCAUXTX16	AN8				
N/A	AVCCAUXRX17	AN10	NC	NC	NC	
N/A	VTRXPAD17	AN11	NC	NC	NC	
N/A	RXNPAD17	AP10	NC	NC	NC	
N/A	RXPPAD17	AP11	NC	NC	NC	
N/A	GNDA17	AM12	NC	NC	NC	

FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	---	3.20	3.40	
A_1	0.40	0.50	0.60	
A_2	---	---	2.80	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	---	---	0.20	
ccc	---	---	0.35	
ddd	---	---	0.30	
eee	---	---	0.10	
M	34			2

NOTES:
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

Figure 6: **FF1152 Flip-Chip Fine-Pitch BGA Package Specifications**

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
6	IO_L25N_6	AH29		
6	IO_L26P_6	AE28		
6	IO_L26N_6	AD28		
6	IO_L27P_6	AG32		
6	IO_L27N_6/VREF_6	AG33		
6	IO_L28P_6	AH32		
6	IO_L28N_6	AG31		
6	IO_L29P_6	AE26		
6	IO_L29N_6	AD26		
6	IO_L30P_6	AG29		
6	IO_L30N_6	AG30		
6	IO_L31P_6	AF32		
6	IO_L31N_6	AF33		
6	IO_L32P_6	AC26		
6	IO_L32N_6	AC27		
6	IO_L33P_6	AF28		
6	IO_L33N_6/VREF_6	AF29		
6	IO_L34P_6	AE33		
6	IO_L34N_6	AE34		
6	IO_L35P_6	AD25		
6	IO_L35N_6	AC25		
6	IO_L36P_6	AF31		
6	IO_L36N_6	AE31		
6	IO_L37P_6	AE29		
6	IO_L37N_6	AE30		
6	IO_L38P_6	AC28		
6	IO_L38N_6	AB27		
6	IO_L39P_6	AD33		
6	IO_L39N_6/VREF_6	AD34		
6	IO_L40P_6	AE32		
6	IO_L40N_6	AD32		
6	IO_L41P_6	AB24		
6	IO_L41N_6	AB25		
6	IO_L42P_6	AD29		
6	IO_L42N_6	AD30		
6	IO_L43P_6	AC33		
6	IO_L43N_6	AC34		
6	IO_L44P_6	AA27		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
2	IO_L11N_2	L9		
2	IO_L11P_2	M10		
2	IO_L12N_2	H4		
2	IO_L12P_2	J5		
2	IO_L13N_2	J1		
2	IO_L13P_2	J2		
2	IO_L14N_2	M8		
2	IO_L14P_2	N9		
2	IO_L15N_2	K6		
2	IO_L15P_2	K7		
2	IO_L16N_2/VREF_2	K4		
2	IO_L16P_2	K5		
2	IO_L17N_2	P10		
2	IO_L17P_2	N10		
2	IO_L18N_2	K3		
2	IO_L18P_2	J3		
2	IO_L19N_2	K1		
2	IO_L19P_2	K2		
2	IO_L20N_2	M11		
2	IO_L20P_2	N11		
2	IO_L21N_2	L7		
2	IO_L21P_2	L8		
2	IO_L22N_2/VREF_2	L5		
2	IO_L22P_2	L6		
2	IO_L23N_2	P8		
2	IO_L23P_2	P9		
2	IO_L24N_2	L3		
2	IO_L24P_2	L4		
2	IO_L25N_2	L1		
2	IO_L25P_2	L2		
2	IO_L26N_2	P11		
2	IO_L26P_2	P12		
2	IO_L27N_2	M6		
2	IO_L27P_2	M7		
2	IO_L28N_2/VREF_2	M2		
2	IO_L28P_2	M3		
2	IO_L29N_2	R9		
2	IO_L29P_2	R10		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
3	IO_L47P_3	AC10		
3	IO_L46N_3	AE7		
3	IO_L46P_3	AE8		
3	IO_L45N_3/VREF_3	AE5		
3	IO_L45P_3	AE6		
3	IO_L44N_3	AB13		
3	IO_L44P_3	AC13		
3	IO_L43N_3	AE3		
3	IO_L43P_3	AE4		
3	IO_L42N_3	AE1		
3	IO_L42P_3	AE2		
3	IO_L41N_3	AD10		
3	IO_L41P_3	AD11		
3	IO_L40N_3	AF6		
3	IO_L40P_3	AF7		
3	IO_L39N_3/VREF_3	AF4		
3	IO_L39P_3	AF5		
3	IO_L38N_3	AC12		
3	IO_L38P_3	AD12		
3	IO_L37N_3	AF1		
3	IO_L37P_3	AF2		
3	IO_L36N_3	AG6		
3	IO_L36P_3	AG7		
3	IO_L35N_3	AE9		
3	IO_L35P_3	AE10		
3	IO_L34N_3	AF3		
3	IO_L34P_3	AG3		
3	IO_L33N_3/VREF_3	AG1		
3	IO_L33P_3	AG2		
3	IO_L32N_3	AE11		
3	IO_L32P_3	AE12		
3	IO_L31N_3	AH6		
3	IO_L31P_3	AH7		
3	IO_L30N_3	AG5		
3	IO_L30P_3	AH4		
3	IO_L29N_3	AD13		
3	IO_L29P_3	AE13		
3	IO_L28N_3	AH2		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
N/A	TXNPAD23	AW36		
N/A	VTTXPAD23	AV36		
N/A	AVCCAUXTX23	AV35		
N/A	VCCINT	AH28		
N/A	VCCINT	M28		
N/A	VCCINT	AG27		
N/A	VCCINT	N27		
N/A	VCCINT	AF26		
N/A	VCCINT	P26		
N/A	VCCINT	AE25		
N/A	VCCINT	AD25		
N/A	VCCINT	AC25		
N/A	VCCINT	AB25		
N/A	VCCINT	AA25		
N/A	VCCINT	Y25		
N/A	VCCINT	W25		
N/A	VCCINT	V25		
N/A	VCCINT	U25		
N/A	VCCINT	T25		
N/A	VCCINT	R25		
N/A	VCCINT	AE24		
N/A	VCCINT	AD24		
N/A	VCCINT	T24		
N/A	VCCINT	R24		
N/A	VCCINT	AE23		
N/A	VCCINT	R23		
N/A	VCCINT	AE22		
N/A	VCCINT	R22		
N/A	VCCINT	AE21		
N/A	VCCINT	R21		
N/A	VCCINT	AE20		
N/A	VCCINT	R20		
N/A	VCCINT	AE19		
N/A	VCCINT	R19		
N/A	VCCINT	AE18		
N/A	VCCINT	R18		
N/A	VCCINT	AE17		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L87P_7		AA33		
7	IO_L87N_7		AA34		
7	IO_L86P_7		Y31		
7	IO_L86N_7		Y32		
7	IO_L85P_7		Y39		
7	IO_L85N_7		Y40		
7	IO_L60P_7		Y36		
7	IO_L60N_7		Y37		
7	IO_L59P_7		Y33		
7	IO_L59N_7		Y34		
7	IO_L58P_7		W41		
7	IO_L58N_7/VREF_7		W42		
7	IO_L57P_7		W39		
7	IO_L57N_7		W40		
7	IO_L56P_7		W31		
7	IO_L56N_7		W32		
7	IO_L55P_7		W37		
7	IO_L55N_7		W38		
7	IO_L54P_7		W35		
7	IO_L54N_7		W36		
7	IO_L53P_7		W33		
7	IO_L53N_7		W34		
7	IO_L52P_7		V41		
7	IO_L52N_7/VREF_7		V42		
7	IO_L51P_7		V38		
7	IO_L51N_7		V39		
7	IO_L50P_7		V31		
7	IO_L50N_7		U32		
7	IO_L49P_7		V35		
7	IO_L49N_7		V36		
7	IO_L48P_7		V32		
7	IO_L48N_7		V33		
7	IO_L47P_7		U31		
7	IO_L47N_7		T31		
7	IO_L46P_7		U41		
7	IO_L46N_7/VREF_7		U42		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	GND		V6		
N/A	GND		U25		
N/A	GND		U24		
N/A	GND		U23		
N/A	GND		U22		
N/A	GND		U21		
N/A	GND		U20		
N/A	GND		U19		
N/A	GND		U18		
N/A	GND		T42		
N/A	GND		T1		
N/A	GND		R39		
N/A	GND		R36		
N/A	GND		R7		
N/A	GND		R4		
N/A	GND		M42		
N/A	GND		M1		
N/A	GND		L22		
N/A	GND		L21		
N/A	GND		K39		
N/A	GND		K4		
N/A	GND		J34		
N/A	GND		J9		
N/A	GND		H42		
N/A	GND		H35		
N/A	GND		H22		
N/A	GND		H21		
N/A	GND		H8		
N/A	GND		H1		
N/A	GND		G36		
N/A	GND		G7		
N/A	GND		F37		
N/A	GND		F25		
N/A	GND		F18		
N/A	GND		F6		
N/A	GND		E38		