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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	3424
Number of Logic Elements/Cells	30816
Total RAM Bits	2506752
Number of I/O	644
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp30-6ffg1152c

implemented. In system mode, a Virtex-II Pro device will continue to function while executing non-test Boundary-Scan instructions. In test mode, Boundary-Scan test instructions control the I/O pins for testing purposes. The Virtex-II Pro Test Access Port (TAP) supports BYPASS, PRELOAD, SAMPLE, IDCODE, and USERCODE non-test instructions. The EXTEST, INTEST, and HIGHZ test instructions are also supported.

Configuration

Virtex-II Pro / Virtex-II Pro devices are configured by loading the bitstream into internal configuration memory using one of the following modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532)

A Data Encryption Standard (DES) decryptor is available on-chip to secure the bitstreams. One or two triple-DES key sets can be used to optionally encrypt the configuration data.

The Xilinx System Advanced Configuration Environment (System ACE) family offers high-capacity and flexible solution for FPGA configuration as well as program/data storage for the processor. See [DS080](#), *System ACE CompactFlash Solution* for more information.

Readback and Integrated Logic Analyzer

Configuration data stored in Virtex-II Pro / Virtex-II Pro configuration memory can be read back for verification. Along with the configuration data, the contents of all flip-flops and latches, distributed SelectRAM+, and block SelectRAM+ memory resources can be read back. This capability is useful for real-time debugging.

The Xilinx ChipScope Integrated Logic Analyzer (ILA) cores and Integrated Bus Analyzer (IBA) cores, along with the ChipScope Pro Analyzer software, provide a complete solution for accessing and verifying user designs within Virtex-II Pro devices.

IP Core and Reference Support

Intellectual Property is part of the Platform FPGA solution. In addition to the existing FPGA fabric cores, the list below shows some of the currently available hardware and software intellectual properties specially developed for Virtex-II Pro / Virtex-II Pro X by Xilinx. Each IP core is modular, portable, Real-Time Operating System (RTOS) independent, and CoreConnect compatible for ease of design migration. Refer to www.xilinx.com/ipcenter for the latest and most complete list of cores.

Hardware Cores

- Bus Infrastructure cores (arbiters, bridges, and more)
- Memory cores (DDR, Flash, and more)
- Peripheral cores (UART, IIC, and more)
- Networking cores (ATM, Ethernet, and more)

Software Cores

- Boot code
- Test code
- Device drivers
- Protocol stacks
- RTOS integration
- Customized board support package

Functional Description: Processor Block

This section briefly describes the interfaces and components of the Processor Block. The subsequent section, **Functional Description: Embedded PowerPC 405 Core** beginning on [page 20](#), offers a summary of major PPC405 core features. For an in-depth discussion on both the Processor Block and PPC405, see the [PowerPC Processor Reference Guide](#) and the [PowerPC 405 Processor Block Reference Guide](#) available on the Xilinx website at <http://www.xilinx.com>.

Processor Block Overview

Figure 14 shows the internal architecture of the Processor Block.

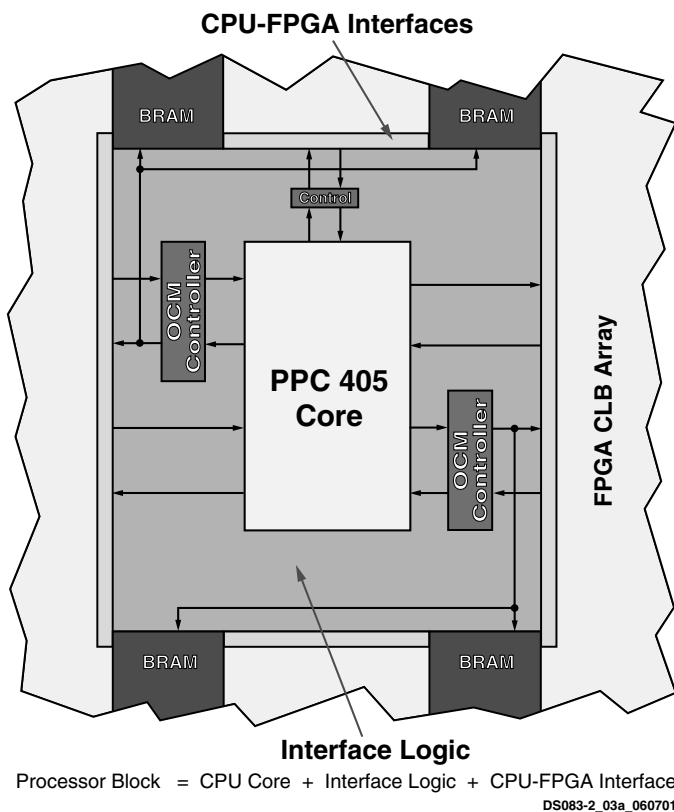


Figure 14: Processor Block Architecture

Within the Virtex-II Pro Processor Block, there are four components:

- Embedded IBM PowerPC 405-D5 RISC CPU core
- On-Chip Memory (OCM) controllers and interfaces
- Clock/control interface logic
- CPU-FPGA Interfaces

Embedded PowerPC 405 RISC Core

The PowerPC 405D5 core is a 0.13 μm implementation of the IBM PowerPC 405D4 core. The advanced process technology enables the embedded PowerPC 405 (PPC405)

core to operate at 300+ MHz while maintaining low power consumption. Specially designed interface logic integrates the core with the surrounding CLBs, block RAMs, and general routing resources. Up to four Processor Blocks can be available in a single Virtex-II Pro device.

The embedded PPC405 core implements the PowerPC User Instruction Set Architecture (UISA), user-level registers, programming model, data types, and addressing modes for 32-bit fixed-point operations. 64-bit operations, auxiliary processor operations, and floating-point operations are trapped and can be emulated in software.

Most of the PPC405 core features are compatible with the specifications for the PowerPC Virtual Environment Architecture (VEA) and Operating Environment Architecture (OEA). They also provide a number of optimizations and extensions to the lower layers of the PowerPC Architecture. The full architecture of the PPC405 is defined by the PowerPC Embedded Environment and PowerPC UISA documentation, available from IBM.

On-Chip Memory (OCM) Controllers

Introduction

The OCM controllers serve as dedicated interfaces between the block RAMs in the FPGA fabric (see [18 Kb Block SelectRAM+ Resources, page 44](#)) and OCM signals available on the embedded PPC405 core. The OCM signals on the PPC405 core are designed to provide very quick access to a fixed amount of instruction and data memory space. The OCM controller provides an interface to both the 64-bit Instruction-Side Block RAM (ISBRAM) and the 32-bit Data-Side Block RAM (DSBRAM). The designer can choose to implement:

- ISBRAM only
- DSBRAM only
- Both ISBRAM and DSBRAM
- No ISBRAM and no DSBRAM

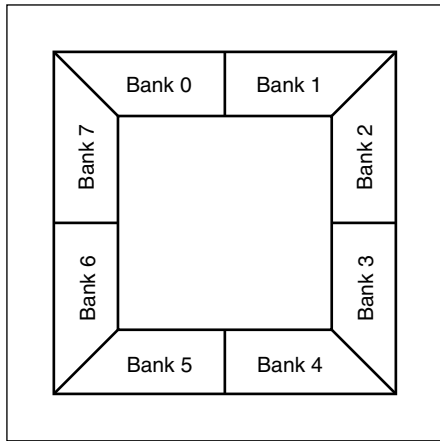
One of OCM's primary advantages is that it guarantees a fixed latency of execution for a higher level of determinism. Additionally, it reduces cache pollution and thrashing, since the cache remains available for caching code from other memory resources.

Typical applications for DSOCM include scratch-pad memory, as well as use of the dual-port feature of block RAM to enable bidirectional data transfer between processor and FPGA. Typical applications for ISOCM include storage of interrupt service routines.

Functional Features

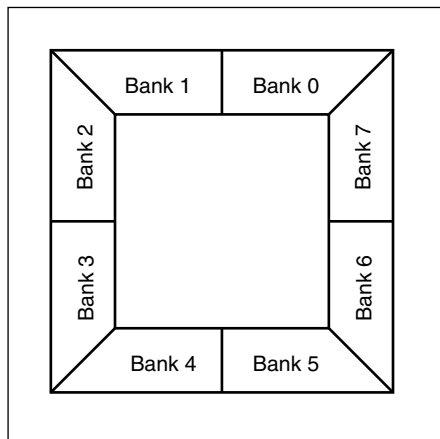
Common Features

- Separate Instruction and Data memory interface between processor core and BRAMs in FPGA
- Dedicated interface to Device Control Register (DCR) bus for ISOCM and DSOCM



ug002_c2_014_041403

Figure 24: I/O Banks: Wire-Bond Packages (FG)
Top View



ds031_66_041403

Figure 25: I/O Banks: Flip-Chip Packages (FF)
Top View

Some input standards require a user-supplied threshold voltage (V_{REF}), and certain user-I/O pins are automatically configured as V_{REF} inputs. Approximately one in six of the I/O pins in the bank assume this role.

V_{REF} pins within a bank are interconnected internally, thus only one V_{REF} voltage can be used within each bank. However, for correct operation, all V_{REF} pins in the bank must be connected to the external reference voltage source.

The V_{CCO} and the V_{REF} pins for each bank appear in the device pinout tables. Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage and not used for I/O. In smaller devices, some V_{CCO} pins used in larger devices do not con-

nect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to V_{CCO} to permit migration to a larger device.

Rules for Combining I/O Standards in the Same Bank

The following rules must be obeyed to combine different input, output, and bi-directional standards in the same bank:

1. **Combining output standards only.** Output standards with the same output V_{CCO} requirement can be combined in the same bank.

Compatible example:

SSTL2_I and LVDS_25 outputs

Incompatible example:

SSTL2_I (output $V_{CCO} = 2.5V$) and
LVCMOS33 (output $V_{CCO} = 3.3V$) outputs

2. **Combining input standards only.** Input standards with the same input V_{CCO} and input V_{REF} requirements can be combined in the same bank.

Compatible example:

LVCMOS15 and HSTL_IV inputs

Incompatible example:

LVCMOS15 (input $V_{CCO} = 1.5V$) and
LVCMOS18 (input $V_{CCO} = 1.8V$) inputs

Incompatible example:

HSTL_I_DCI_18 ($V_{REF} = 0.9V$) and
HSTL_IV_DCI_18 ($V_{REF} = 1.1V$) inputs

3. **Combining input standards and output standards.** Input standards and output standards with the same input V_{CCO} and output V_{CCO} requirement can be combined in the same bank.

Compatible example:

LVDS_25 output and HSTL_I input

Incompatible example:

LVDS_25 output (output $V_{CCO} = 2.5V$) and
HSTL_I_DCI_18 input (input $V_{CCO} = 1.8V$)

4. **Combining bi-directional standards with input or output standards.** When combining bi-directional I/O with other standards, make sure the bi-directional standard can meet rules 1 through 3 above.

5. **Additional rules for combining DCI I/O standards.**

- a. No more than one Single Termination type (input or output) is allowed in the same bank.

Incompatible example:

HSTL_IV_DCI input and HSTL_III_DCI input

- b. No more than one Split Termination type (input or output) is allowed in the same bank.

Incompatible example:

HSTL_I_DCI input and HSTL_II_DCI input

The implementation tools will enforce the above design rules.

Table 12, page 30, summarizes all standards and voltage supplies.

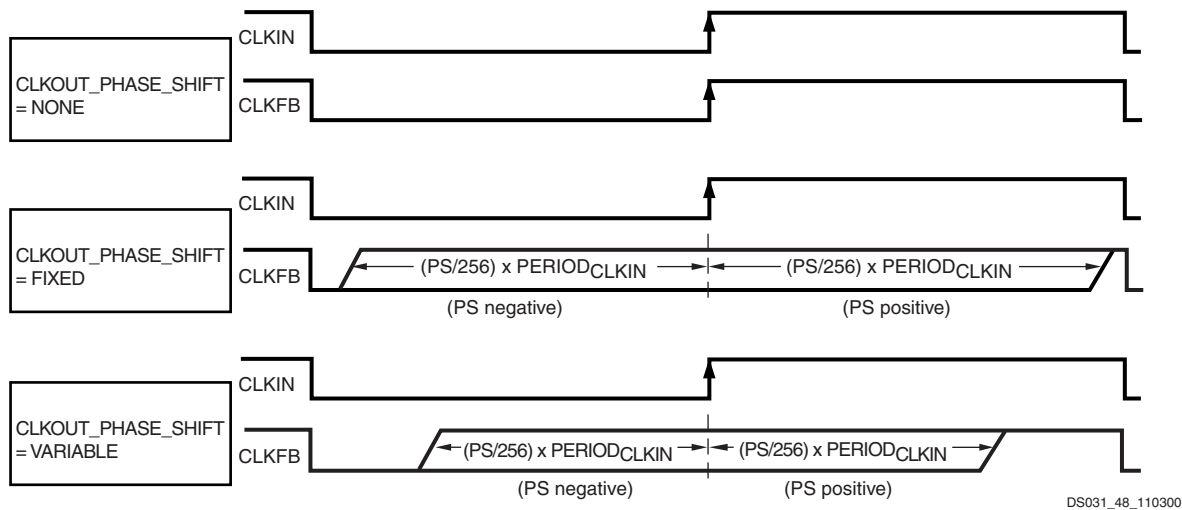


Figure 63: Fine-Phase Shifting Effects

Two separate components of the phase shift range must be understood:

- PHASE_SHIFT attribute range
- FINE_SHIFT_RANGE DCM timing parameter range

The PHASE_SHIFT attribute is the numerator in the following equation:

$$\text{Phase Shift (ns)} = (\text{PHASE_SHIFT}/256) * \text{PERIOD}_{\text{CLKIN}}$$

The full range of this attribute is always -255 to +255, but its practical range varies with CLKIN frequency, as constrained by the FINE_SHIFT_RANGE component, which represents the total delay achievable by the phase shift delay line. Total delay is a function of the number of delay taps used in the circuit. Across process, voltage, and temperature, this absolute range is guaranteed to be as specified under **DCM Timing Parameters** in *Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics*.

Absolute range (fixed mode) = $\pm \text{FINE_SHIFT_RANGE}$

Absolute range (variable mode) = $\pm \text{FINE_SHIFT_RANGE}/2$

The reason for the difference between fixed and variable modes is as follows. For variable mode to allow symmetric, dynamic sweeps from -255/256 to +255/256, the DCM sets the "zero phase skew" point as the middle of the delay line, thus dividing the total delay line range in half. In fixed mode,

since the PHASE_SHIFT value never changes after configuration, the entire delay line is available for insertion into either the CLKIN or CLKFB path (to create either positive or negative skew).

Taking both of these components into consideration, the following are some usage examples:

- If $\text{PERIOD}_{\text{CLKIN}} = 2 * \text{FINE_SHIFT_RANGE}$, then PHASE_SHIFT in fixed mode is limited to ± 128 , and in variable mode it is limited to ± 64 .
- If $\text{PERIOD}_{\text{CLKIN}} = \text{FINE_SHIFT_RANGE}$, then PHASE_SHIFT in fixed mode is limited to ± 255 , and in variable mode it is limited to ± 128 .
- If $\text{PERIOD}_{\text{CLKIN}} \leq 0.5 * \text{FINE_SHIFT_RANGE}$, then PHASE_SHIFT is limited to ± 255 in either mode.

Operating Modes

The frequency ranges of DCM input and output clocks depend on the operating mode specified, either low-frequency mode or high-frequency mode, according to Table 30. For actual values, see *Virtex-II Pro and Virtex-II Pro X Platform FPGAs: DC and Switching Characteristics*. The CLK2X, CLK2X180, CLK90, and CLK270 outputs are not available in high-frequency mode.

High or low-frequency mode is selected by an attribute.

Table 30: DCM Frequency Ranges

Output Clock	Low-Frequency Mode		High-Frequency Mode	
	CLKIN Input	CLK Output	CLKIN Input	CLK Output
CLK0, CLK180	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_1X_LF	CLKIN_FREQ_DLL_HF	CLKOUT_FREQ_1X_HF
CLK90, CLK270	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_1X_LF	NA	NA
CLK2X, CLK2X180	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_2X_LF	NA	NA
CLKDV	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_DV_LF	CLKIN_FREQ_DLL_HF	CLKOUT_FREQ_DV_HF
CLKFX, CLKFX180	CLKIN_FREQ_FX_LF	CLKOUT_FREQ_FX_LF	CLKIN_FREQ_FX_HF	CLKOUT_FREQ_FX_HF

Routing

DCM and MGT Locations/Organization

Virtex-II Pro DCMs and serial transceivers (MGTS) are placed on the top and bottom of each block RAM and multiplier column in some combination, as shown in Table 31. The number of DCMs and RocketIO transceivers total twice the number of block RAM columns in the device. Refer to Figure 52, page 47 for an illustration of this in the XC2VP4 device.

Table 31: DCM and MGT Organization

Device	Block RAM Columns	DCMs	MGTS
XC2VP2	4	4	4
XC2VP4	4	4	4
XC2VP7	6	4	8
XC2VP20	8	8	8
XC2VPX20	8	8	8
XC2VP30	8	8	8
XC2VP40	10	8	12
XC2VP50	12	8	16
XC2VP70	14	8	20
XC2VPX70	14	8	20
XC2VP100	16	12	20

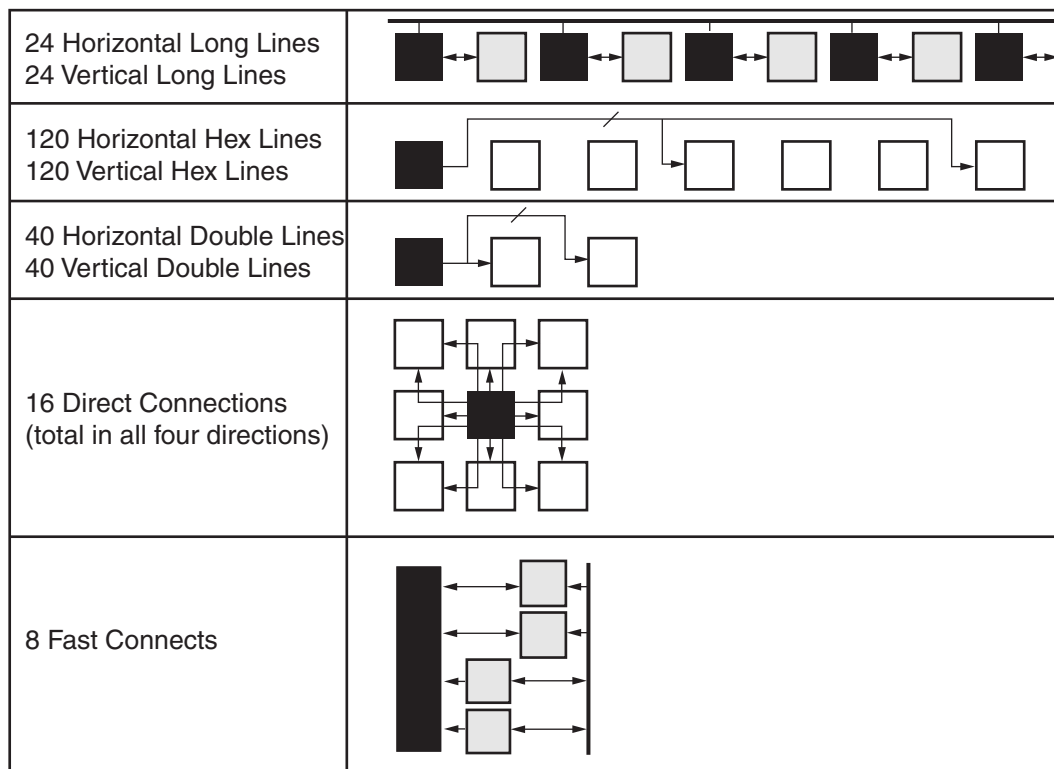
Place-and-route software takes advantage of this regular array to deliver optimum system performance and fast compile times. The segmented routing resources are essential to guarantee IP cores portability and to efficiently handle an incremental design flow that is based on modular implementations. Total design time is reduced due to fewer and shorter design iterations.

Hierarchical Routing Resources

Most Virtex-II Pro signals are routed using the global routing resources, which are located in horizontal and vertical routing channels between each switch matrix.

As shown in Figure 64, page 54, Virtex-II Pro has fully buffered programmable interconnections, with a number of resources counted between any two adjacent switch matrix rows or columns. Fanout has minimal impact on the performance of each net.

- The long lines are bidirectional wires that distribute signals across the device. Vertical and horizontal long lines span the full height and width of the device.
- The hex lines route signals to every third or sixth block away in all four directions. Organized in a staggered pattern, hex lines can only be driven from one end. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source).



DS031_60_110200

Figure 64: Hierarchical Routing Resources

Table 6: FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
7	IO_L88N_7/VREF_7	L5			
7	IO_L86P_7	L6			
7	IO_L86N_7	K6			
7	IO_L85P_7	K1			
7	IO_L85N_7	K2			
7	IO_L60P_7	K3	NC		
7	IO_L60N_7	K4	NC		
7	IO_L58P_7	K5	NC		
7	IO_L58N_7/VREF_7	J5	NC		
7	IO_L56P_7	J1	NC		
7	IO_L56N_7	J2	NC		
7	IO_L55P_7	J3	NC		
7	IO_L55N_7	J4	NC		
7	IO_L54P_7	J6	NC		
7	IO_L54N_7	H5	NC		
7	IO_L52P_7	H1	NC		
7	IO_L52N_7/VREF_7	H2	NC		
7	IO_L50P_7	H3	NC		
7	IO_L50N_7	H4	NC		
7	IO_L49P_7	G1	NC		
7	IO_L49N_7	G2	NC		
7	IO_L48P_7	G3	NC		
7	IO_L48N_7	G4	NC		
7	IO_L46P_7	G5	NC		
7	IO_L46N_7/VREF_7	F5	NC		
7	IO_L43P_7	F1	NC		
7	IO_L43N_7	F2	NC		
7	IO_L06P_7	F3			
7	IO_L06N_7	F4			
7	IO_L04P_7	E1			
7	IO_L04N_7/VREF_7	E2			
7	IO_L03P_7	E3			
7	IO_L03N_7	E4			
7	IO_L02P_7	D1			
7	IO_L02N_7	D2			
7	IO_L01P_7/VRN_7	C1			
7	IO_L01N_7/VRP_7	C2			

Table 7: FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
7	IO_L04N_7/VREF_7	E2			
7	IO_L03P_7	F5			
7	IO_L03N_7	E4			
7	IO_L02P_7	D1			
7	IO_L02N_7	D2			
7	IO_L01P_7/VRN_7	C1			
7	IO_L01N_7/VRP_7	C2			
0	VCCO_0	C5			
0	VCCO_0	C8			
0	VCCO_0	D11			
0	VCCO_0	J10			
0	VCCO_0	J11			
0	VCCO_0	K12			
0	VCCO_0	K13			
1	VCCO_1	C19			
1	VCCO_1	C22			
1	VCCO_1	D16			
1	VCCO_1	J16			
1	VCCO_1	J17			
1	VCCO_1	K14			
1	VCCO_1	K15			
2	VCCO_2	E24			
2	VCCO_2	H24			
2	VCCO_2	K18			
2	VCCO_2	L18			
2	VCCO_2	L23			
2	VCCO_2	M17			
2	VCCO_2	N17			
3	VCCO_3	P17			
3	VCCO_3	R17			
3	VCCO_3	T18			
3	VCCO_3	T23			
3	VCCO_3	U18			
3	VCCO_3	W24			

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
5	IO_L48N_5		AH20	NC		
5	IO_L48P_5		AH21	NC		
5	IO_L47N_5		AE19	NC		
5	IO_L47P_5		AE20	NC		
5	IO_L46N_5		AD18	NC		
5	IO_L46P_5		AC18	NC		
5	IO_L45N_5/VREF_5		AJ22			
5	IO_L45P_5		AH22			
5	IO_L44N_5		AE21			
5	IO_L44P_5		AE22			
5	IO_L43N_5		AD19			
5	IO_L43P_5		AC19			
5	IO_L39N_5		AG21			
5	IO_L39P_5		AF21			
5	IO_L38N_5		AF22			
5	IO_L38P_5		AF23			
5	IO_L37N_5		AD20			
5	IO_L37P_5		AC20			
5	IO_L09N_5/VREF_5		AK23			
5	IO_L09P_5		AJ23			
5	IO_L08N_5		AE23			
5	IO_L08P_5		AE24			
5	IO_L07N_5/VREF_5		AD21			
5	IO_L07P_5		AC21			
5	IO_L06N_5/VRP_5		AH23			
5	IO_L06P_5/VRN_5		AG23			
5	IO_L05_5/No_Pair		AD23			
5	IO_L03N_5/D4		AH24			
5	IO_L03P_5/D5		AG24			
5	IO_L02N_5/D6		AD22			
5	IO_L02P_5/D7		AC22			
5	IO_L01N_5/RDWR_B		AF24			
5	IO_L01P_5/CS_B		AG25			
6	IO_L01P_6/VRN_6		AK28			
6	IO_L01N_6/VRP_6		AJ28			

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
4	IO_L27P_4/VREF_4	AL10	NC	NC		
4	IO_L37N_4	AE13				
4	IO_L37P_4	AF13				
4	IO_L38N_4	AG13				
4	IO_L38P_4	AH13				
4	IO_L39N_4	AJ11				
4	IO_L39P_4	AK11				
4	IO_L43N_4	AE14				
4	IO_L43P_4	AF14				
4	IO_L44N_4	AJ13				
4	IO_L44P_4	AK13				
4	IO_L45N_4	AL11				
4	IO_L45P_4/VREF_4	AM11				
4	IO_L46N_4	AE15				
4	IO_L46P_4	AF15				
4	IO_L47N_4	AG14				
4	IO_L47P_4	AH14				
4	IO_L48N_4	AL13				
4	IO_L48P_4	AL12				
4	IO_L49N_4	AD16				
4	IO_L49P_4	AE16				
4	IO_L50_4/No_Pair	AJ14				
4	IO_L53_4/No_Pair	AK14				
4	IO_L54N_4	AM14				
4	IO_L54P_4	AM13				
4	IO_L55N_4	AF16				
4	IO_L55P_4	AG16				
4	IO_L56N_4	AH15				
4	IO_L56P_4	AJ15				
4	IO_L57N_4	AL14				
4	IO_L57P_4/VREF_4	AL15				
4	IO_L67N_4	AD17				
4	IO_L67P_4	AE17				
4	IO_L68N_4	AH16				
4	IO_L68P_4	AJ16				
4	IO_L69N_4	AK16				
4	IO_L69P_4/VREF_4	AL16				
4	IO_L73N_4	AF17				

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	GND	V19				
N/A	GND	V20				
N/A	GND	V21				
N/A	GND	W1				
N/A	GND	W14				
N/A	GND	W15				
N/A	GND	W16				
N/A	GND	W17				
N/A	GND	W18				
N/A	GND	W19				
N/A	GND	W20				
N/A	GND	W21				
N/A	GND	W34				
N/A	GND	Y8				
N/A	GND	Y14				
N/A	GND	Y15				
N/A	GND	Y16				
N/A	GND	Y17				
N/A	GND	Y18				
N/A	GND	Y19				
N/A	GND	Y20				
N/A	GND	Y21				
N/A	GND	Y27				
N/A	GND	AA14				
N/A	GND	AA15				
N/A	GND	AA16				
N/A	GND	AA17				
N/A	GND	AA18				
N/A	GND	AA19				
N/A	GND	AA20				
N/A	GND	AA21				
N/A	GND	AC5				
N/A	GND	AC8				
N/A	GND	AC27				
N/A	GND	AC30				
N/A	GND	AE3				
N/A	GND	AE32				
N/A	GND	H23				

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L43N_0	B22		
0	IO_L43P_0	C22		
0	IO_L44N_0	K21		
0	IO_L44P_0	L21		
0	IO_L45N_0	G21		
0	IO_L45P_0/VREF_0	H21		
0	IO_L46N_0	E21		
0	IO_L46P_0	F21		
0	IO_L47N_0	K20		
0	IO_L47P_0	L20		
0	IO_L48N_0	C21		
0	IO_L48P_0	D21		
0	IO_L49N_0	A21		
0	IO_L49P_0	B21		
0	IO_L50_0/No_Pair	G20		
0	IO_L53_0/No_Pair	H19		
0	IO_L54N_0	E20		
0	IO_L54P_0	F20		
0	IO_L55N_0	C20		
0	IO_L55P_0	D19		
0	IO_L56N_0	K19		
0	IO_L56P_0	L19		
0	IO_L57N_0	A20		
0	IO_L57P_0/VREF_0	B20		
0	IO_L66N_0	F19	NC	
0	IO_L66P_0/VREF_0	G19	NC	
0	IO_L67N_0	B19		
0	IO_L67P_0	C19		
0	IO_L68N_0	H18		
0	IO_L68P_0	J18		
0	IO_L69N_0	F18		
0	IO_L69P_0/VREF_0	G18		
0	IO_L73N_0	D18		
0	IO_L73P_0	E18		
0	IO_L74N_0/GCLK7P	K18		
0	IO_L74P_0/GCLK6S	L18		
0	IO_L75N_0/GCLK5P	B18		
0	IO_L75P_0/GCLK4S	C18		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
3	IO_L90P_3	AA8		
3	IO_L89N_3	Y11		
3	IO_L89P_3	Y12		
3	IO_L88N_3	AA5		
3	IO_L88P_3	AA6		
3	IO_L87N_3/VREF_3	AA3		
3	IO_L87P_3	AA4		
3	IO_L86N_3	Y13		
3	IO_L86P_3	AA13		
3	IO_L85N_3	AB7		
3	IO_L85P_3	AB8		
3	IO_L60N_3	AB5		
3	IO_L60P_3	AB6		
3	IO_L59N_3	AA9		
3	IO_L59P_3	AA10		
3	IO_L58N_3	AB3		
3	IO_L58P_3	AB4		
3	IO_L57N_3/VREF_3	AB1		
3	IO_L57P_3	AB2		
3	IO_L56N_3	AA11		
3	IO_L56P_3	AA12		
3	IO_L55N_3	AC5		
3	IO_L55P_3	AC6		
3	IO_L54N_3	AC1		
3	IO_L54P_3	AC2		
3	IO_L53N_3	AB9		
3	IO_L53P_3	AB10		
3	IO_L52N_3	AC8		
3	IO_L52P_3	AD8		
3	IO_L51N_3/VREF_3	AC4		
3	IO_L51P_3	AD4		
3	IO_L50N_3	AB11		
3	IO_L50P_3	AB12		
3	IO_L49N_3	AD6		
3	IO_L49P_3	AD7		
3	IO_L48N_3	AD2		
3	IO_L48P_3	AD3		
3	IO_L47N_3	AC9		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L86P_2		Y12		
2	IO_L87N_2		AA9		
2	IO_L87P_2		AA10		
2	IO_L88N_2/VREF_2		AA6		
2	IO_L88P_2		AA7		
2	IO_L89N_2		AA12		
2	IO_L89P_2		AB12		
2	IO_L90N_2		AA3		
2	IO_L90P_2		AA4		
3	IO_L90N_3		AB3		
3	IO_L90P_3		AB4		
3	IO_L89N_3		AB6		
3	IO_L89P_3		AB7		
3	IO_L88N_3		AB9		
3	IO_L88P_3		AB10		
3	IO_L87N_3/VREF_3		AC3		
3	IO_L87P_3		AC4		
3	IO_L86N_3		AC11		
3	IO_L86P_3		AC12		
3	IO_L85N_3		AC6		
3	IO_L85P_3		AC7		
3	IO_L60N_3		AC9		
3	IO_L60P_3		AC10		
3	IO_L59N_3		AD9		
3	IO_L59P_3		AD10		
3	IO_L58N_3		AD1		
3	IO_L58P_3		AD2		
3	IO_L57N_3/VREF_3		AD3		
3	IO_L57P_3		AD4		
3	IO_L56N_3		AD11		
3	IO_L56P_3		AD12		
3	IO_L55N_3		AD5		
3	IO_L55P_3		AD6		
3	IO_L54N_3		AD7		
3	IO_L54P_3		AD8		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
7	IO_L09P_7		K36		
7	IO_L09N_7		K35		
7	IO_L08P_7		K38		
7	IO_L08N_7		K37		
7	IO_L07P_7		L33		
7	IO_L07N_7		K34		
7	IO_L84P_7		J41		
7	IO_L84N_7		J42		
7	IO_L83P_7		J39		
7	IO_L83N_7		J38		
7	IO_L82P_7		J36		
7	IO_L82N_7/VREF_7		J37		
7	IO_L81P_7		J35		
7	IO_L81N_7		H36		
7	IO_L80P_7		H41		
7	IO_L80N_7		H40		
7	IO_L79P_7		H38		
7	IO_L79N_7		H39		
7	IO_L78P_7		H37		
7	IO_L78N_7		G38		
7	IO_L77P_7		G42		
7	IO_L77N_7		G41		
7	IO_L76P_7		G39		
7	IO_L76N_7/VREF_7		G40		
7	IO_L75P_7		F41		
7	IO_L75N_7		F42		
7	IO_L74P_7		F40		
7	IO_L74N_7		F39		
7	IO_L73P_7		E41		
7	IO_L73N_7		E42		
7	IO_L06P_7		D41		
7	IO_L06N_7		D42		
7	IO_L05P_7		E40		
7	IO_L05N_7		D40		
7	IO_L04P_7		F36		
7	IO_L04N_7/VREF_7		G37		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
5	VCCO_5		AH22		
6	VCCO_6		AU38		
6	VCCO_6		AP40		
6	VCCO_6		AL37		
6	VCCO_6		AJ39		
6	VCCO_6		AH29		
6	VCCO_6		AG34		
6	VCCO_6		AG29		
6	VCCO_6		AG28		
6	VCCO_6		AF29		
6	VCCO_6		AF28		
6	VCCO_6		AE40		
6	VCCO_6		AE29		
6	VCCO_6		AE28		
6	VCCO_6		AD29		
6	VCCO_6		AD28		
6	VCCO_6		AC38		
6	VCCO_6		AC35		
6	VCCO_6		AC29		
6	VCCO_6		AC28		
6	VCCO_6		AB29		
6	VCCO_6		AB28		
7	VCCO_7		AA29		
7	VCCO_7		AA28		
7	VCCO_7		Y38		
7	VCCO_7		Y35		
7	VCCO_7		Y29		
7	VCCO_7		Y28		
7	VCCO_7		W29		
7	VCCO_7		W28		
7	VCCO_7		V40		
7	VCCO_7		V29		
7	VCCO_7		V28		
7	VCCO_7		U29		
7	VCCO_7		U28		
7	VCCO_7		T34		

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
1	IO_L21P_1	H13	
1	IO_L20N_1	L12	
1	IO_L20P_1	K12	
1	IO_L19N_1	B11	
1	IO_L19P_1	A11	
1	IO_L09N_1/VREF_1	E11	
1	IO_L09P_1	D11	
1	IO_L08N_1	J11	
1	IO_L08P_1	H11	
1	IO_L07N_1	G11	
1	IO_L07P_1	F11	
1	IO_L06N_1	B10	
1	IO_L06P_1	A10	
1	IO_L05_1/No_Pair	G10	
1	IO_L03N_1/VREF_1	C10	
1	IO_L03P_1	C11	
1	IO_L02N_1	L11	
1	IO_L02P_1	K11	
1	IO_L01N_1/VRP_1	F10	
1	IO_L01P_1/VRN_1	E10	
2	IO_L01N_2/VRP_2	B8	
2	IO_L01P_2/VRN_2	A8	
2	IO_L02N_2	C9	
2	IO_L02P_2	B9	
2	IO_L03N_2	B7	
2	IO_L03P_2	A7	
2	IO_L04N_2/VREF_2	B6	
2	IO_L04P_2	A6	
2	IO_L05N_2	D8	
2	IO_L05P_2	D9	
2	IO_L06N_2	B4	
2	IO_L06P_2	A4	
2	IO_L73N_2	C7	
2	IO_L73P_2	C8	
2	IO_L74N_2	G9	
2	IO_L74P_2	F9	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
2	IO_L59N_2	AA11	
2	IO_L59P_2	AA12	
2	IO_L60N_2	W1	
2	IO_L60P_2	W2	
2	IO_L85N_2	Y2	
2	IO_L85P_2	Y3	
2	IO_L86N_2	AA9	
2	IO_L86P_2	AA10	
2	IO_L87N_2	AA5	
2	IO_L87P_2	AA6	
2	IO_L88N_2/VREF_2	AA4	
2	IO_L88P_2	Y4	
2	IO_L89N_2	AA7	
2	IO_L89P_2	AA8	
2	IO_L90N_2	AA2	
2	IO_L90P_2	AA3	
3	IO_L90N_3	AB5	
3	IO_L90P_3	AB6	
3	IO_L89N_3	AB11	
3	IO_L89P_3	AB12	
3	IO_L88N_3	AB2	
3	IO_L88P_3	AB3	
3	IO_L87N_3/VREF_3	AB4	
3	IO_L87P_3	AC4	
3	IO_L86N_3	AB9	
3	IO_L86P_3	AB10	
3	IO_L85N_3	AC2	
3	IO_L85P_3	AC3	
3	IO_L60N_3	AD5	
3	IO_L60P_3	AD6	
3	IO_L59N_3	AB7	
3	IO_L59P_3	AB8	
3	IO_L58N_3	AD1	
3	IO_L58P_3	AD2	
3	IO_L57N_3/VREF_3	AE4	
3	IO_L57P_3	AE5	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L62N_6	AL35	
6	IO_L63P_6	AV36	
6	IO_L63N_6/VREF_6	AU36	
6	IO_L64P_6	AV35	
6	IO_L64N_6	AU35	
6	IO_L65P_6	AK35	
6	IO_L65N_6	AJ34	
6	IO_L66P_6	AU41	
6	IO_L66N_6	AU42	
6	IO_L67P_6	AU38	
6	IO_L67N_6	AT38	
6	IO_L68P_6	AK32	
6	IO_L68N_6	AK33	
6	IO_L69P_6	AU37	
6	IO_L69N_6/VREF_6	AT37	
6	IO_L70P_6	AT41	
6	IO_L70N_6	AT42	
6	IO_L71P_6	AK31	
6	IO_L71N_6	AJ31	
6	IO_L72P_6	AT39	
6	IO_L72N_6	AT40	
6	IO_L07P_6	AT35	
6	IO_L07N_6	AT36	
6	IO_L08P_6	AJ32	
6	IO_L08N_6	AJ33	
6	IO_L09P_6	AR42	
6	IO_L09N_6/VREF_6	AP41	
6	IO_L10P_6	AR40	
6	IO_L10N_6	AR41	
6	IO_L11P_6	AH34	
6	IO_L11N_6	AH35	
6	IO_L12P_6	AR38	
6	IO_L12N_6	AR39	
6	IO_L13P_6	AR36	
6	IO_L13N_6	AR37	
6	IO_L14P_6	AH32	
6	IO_L14N_6	AH33	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L15P_6	AP39	
6	IO_L15N_6/VREF_6	AP40	
6	IO_L16P_6	AP36	
6	IO_L16N_6	AP37	
6	IO_L17P_6	AH31	
6	IO_L17N_6	AG31	
6	IO_L18P_6	AN41	
6	IO_L18N_6	AN42	
6	IO_L19P_6	AN40	
6	IO_L19N_6	AM40	
6	IO_L20P_6	AG34	
6	IO_L20N_6	AG35	
6	IO_L21P_6	AN37	
6	IO_L21N_6/VREF_6	AN38	
6	IO_L22P_6	AN36	
6	IO_L22N_6	AM36	
6	IO_L23P_6	AG32	
6	IO_L23N_6	AG33	
6	IO_L24P_6	AM41	
6	IO_L24N_6	AM42	
6	IO_L25P_6	AM38	
6	IO_L25N_6	AM39	
6	IO_L26P_6	AF35	
6	IO_L26N_6	AF36	
6	IO_L27P_6	AM37	
6	IO_L27N_6/VREF_6	AL36	
6	IO_L28P_6	AL41	
6	IO_L28N_6	AK41	
6	IO_L29P_6	AF32	
6	IO_L29N_6	AF33	
6	IO_L30P_6	AL39	
6	IO_L30N_6	AL40	
6	IO_L31P_6	AL37	
6	IO_L31N_6	AL38	
6	IO_L32P_6	AF31	
6	IO_L32N_6	AE31	
6	IO_L33P_6	AK39	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
5	VCCO_5	AL30	
5	VCCO_5	AW29	
5	VCCO_5	AR29	
5	VCCO_5	AJ26	
5	VCCO_5	AW25	
5	VCCO_5	AR25	
5	VCCO_5	AJ25	
5	VCCO_5	AH25	
5	VCCO_5	AJ24	
5	VCCO_5	AH24	
5	VCCO_5	AJ23	
5	VCCO_5	AH23	
5	VCCO_5	AJ22	
5	VCCO_5	AH22	
4	VCCO_4	AJ21	
4	VCCO_4	AH21	
4	VCCO_4	AJ20	
4	VCCO_4	AH20	
4	VCCO_4	AJ19	
4	VCCO_4	AH19	
4	VCCO_4	AW18	
4	VCCO_4	AR18	
4	VCCO_4	AJ18	
4	VCCO_4	AH18	
4	VCCO_4	AJ17	
4	VCCO_4	AW14	
4	VCCO_4	AR14	
4	VCCO_4	AL13	
4	VCCO_4	AW10	
3	VCCO_3	AG15	
3	VCCO_3	AF15	
3	VCCO_3	AE15	
3	VCCO_3	AD15	
3	VCCO_3	AC15	
3	VCCO_3	AB15	
3	VCCO_3	AH14	
3	VCCO_3	AG14	