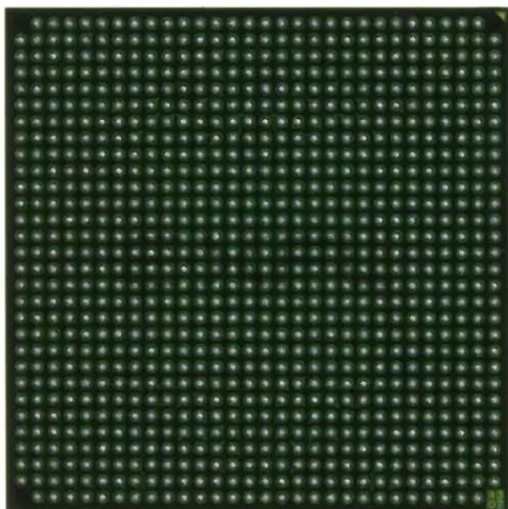




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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                         |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                                |
| Number of LABs/CLBs            | 3424                                                                                                                                    |
| Number of Logic Elements/Cells | 30816                                                                                                                                   |
| Total RAM Bits                 | 2506752                                                                                                                                 |
| Number of I/O                  | 556                                                                                                                                     |
| Number of Gates                | -                                                                                                                                       |
| Voltage - Supply               | 1.425V ~ 1.575V                                                                                                                         |
| Mounting Type                  | Surface Mount                                                                                                                           |
| Operating Temperature          | -40°C ~ 100°C (TJ)                                                                                                                      |
| Package / Case                 | 896-BBGA, FCBGA                                                                                                                         |
| Supplier Device Package        | 896-FCBGA (31x31)                                                                                                                       |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/xilinx/xc2vp30-6ffg896i">https://www.e-xfl.com/product-detail/xilinx/xc2vp30-6ffg896i</a> |

**Table 12: Summary of Voltage Supply Requirements for All Input and Output Standards**

| I/O Standard             | V <sub>CCO</sub> |          | V <sub>REF</sub> | Termination Type |       |
|--------------------------|------------------|----------|------------------|------------------|-------|
|                          | Output           | Input    | Input            | Output           | Input |
| LVTTTL <sup>(1)</sup>    | 3.3              | 3.3      | N/R              | N/R              | N/R   |
| LVC MOS33 <sup>(1)</sup> |                  |          | N/R              | N/R              | N/R   |
| LVDCI_33 <sup>(1)</sup>  |                  |          | N/R              | Series           | N/R   |
| PCIX <sup>(2)</sup>      |                  |          | N/R              | N/R              | N/R   |
| PCI33_3 <sup>(2)</sup>   |                  |          | N/R              | N/R              | N/R   |
| PCI66_3 <sup>(2)</sup>   |                  |          | N/R              | N/R              | N/R   |
| LVDS_25                  | 2.5              | Note (3) | N/R              | N/R              | N/R   |
| LVDSEXT_25               |                  |          | N/R              | N/R              | N/R   |
| LDT_25                   |                  |          | N/R              | N/R              | N/R   |
| ULVDS_25                 |                  |          | N/R              | N/R              | N/R   |
| BLVDS_25                 |                  |          | N/R              | N/R              | N/R   |
| LVPECL_25                |                  |          | N/R              | N/R              | N/R   |
| SSTL2_I                  |                  |          | 1.25             | N/R              | N/R   |
| SSTL2_II                 |                  |          | 1.25             | N/R              | N/R   |
| LVC MOS25                |                  | 2.5      | N/R              | N/R              | N/R   |
| LVDCI_25                 |                  |          | N/R              | Series           | N/R   |
| LVDCI_DV2_25             |                  |          | N/R              | Series           | N/R   |
| LVDS_25_DCI              |                  |          | N/R              | N/R              | Split |
| LVDSEXT_25_DCI           |                  |          | N/R              | N/R              | Split |
| SSTL2_I_DCI              |                  |          | 1.25             | N/R              | Split |
| SSTL2_II_DCI             |                  |          | 1.25             | Split            | Split |
| LVDS_25_DT               |                  |          | N/R              | N/R              | N/R   |
| LVDSEXT_25_DT            |                  |          | N/R              | N/R              | N/R   |
| LDT_25_DT                |                  |          | N/R              | N/R              | N/R   |
| ULVDS_25_DT              |                  |          | N/R              | N/R              | N/R   |

**Table 12: Summary of Voltage Supply Requirements for All Input and Output Standards (Continued)**

| I/O Standard    | V <sub>CCO</sub> |          | V <sub>REF</sub> | Termination Type |        |
|-----------------|------------------|----------|------------------|------------------|--------|
|                 | Output           | Input    | Input            | Output           | Input  |
| HSTL_III_18     | 1.8              | Note (3) | 1.1              | N/R              | N/R    |
| HSTL_IV_18      |                  |          | 1.1              | N/R              | N/R    |
| HSTL_I_18       |                  |          | 0.9              | N/R              | N/R    |
| HSTL_II_18      |                  |          | 0.9              | N/R              | N/R    |
| SSTL18_I        |                  |          | 0.9              | N/R              | N/R    |
| SSTL18_II       |                  |          | 0.9              | N/R              | N/R    |
| LVC MOS18       |                  | 1.8      | N/R              | N/R              | N/R    |
| LVDCI_18        |                  |          | N/R              | Series           | N/R    |
| LVDCI_DV2_18    |                  |          | N/R              | Series           | N/R    |
| HSTL_III_DCI_18 |                  |          | 1.1              | N/R              | Single |
| HSTL_IV_DCI_18  |                  |          | 1.1              | Single           | Single |
| HSTL_I_DCI_18   |                  |          | 0.9              | N/R              | Split  |
| HSTL_II_DCI_18  |                  |          | 0.9              | Split            | Split  |
| SSTL18_I_DCI    |                  |          | 0.9              | N/R              | Split  |
| SSTL18_II_DCI   |                  |          | 0.9              | Split            | Split  |
| HSTL_III        | 1.5              | Note (3) | 0.9              | N/R              | N/R    |
| HSTL_IV         |                  |          | 0.9              | N/R              | N/R    |
| HSTL_I          |                  |          | 0.75             | N/R              | N/R    |
| HSTL_II         |                  |          | 0.75             | N/R              | N/R    |
| LVC MOS15       |                  | 1.5      | N/R              | N/R              | N/R    |
| LVDCI_15        |                  |          | N/R              | Series           | N/R    |
| LVDCI_DV2_15    |                  |          | N/R              | Series           | N/R    |
| GTL_P_DCI       |                  |          | 1                | Single           | Single |
| HSTL_III_DCI    |                  |          | 0.9              | N/R              | Single |
| HSTL_IV_DCI     |                  |          | 0.9              | Single           | Single |
| HSTL_I_DCI      |                  |          | 0.75             | N/R              | Split  |
| HSTL_II_DCI     |                  |          | 0.75             | Split            | Split  |
| GTL_DCI         | 1.2              | 1.2      | 0.8              | Single           | Single |
| GTL_P           | N/R              | Note (3) | 1                | N/R              | N/R    |
| GTL             |                  |          | 0.8              | N/R              | N/R    |

**Notes:**

1. See application note [XAPP659](#) for more detailed information.
2. See application note [XAPP653](#) for more detailed information.
3. Pin voltage must not exceed V<sub>CCO</sub>.
4. N/R = no requirement.

Figure 30 provides examples illustrating the use of the LVDS\_25\_DCI and LVDSEXT\_25\_DCI I/O standards. For a complete list, see the [Virtex-II Pro Platform FPGA User Guide](#).

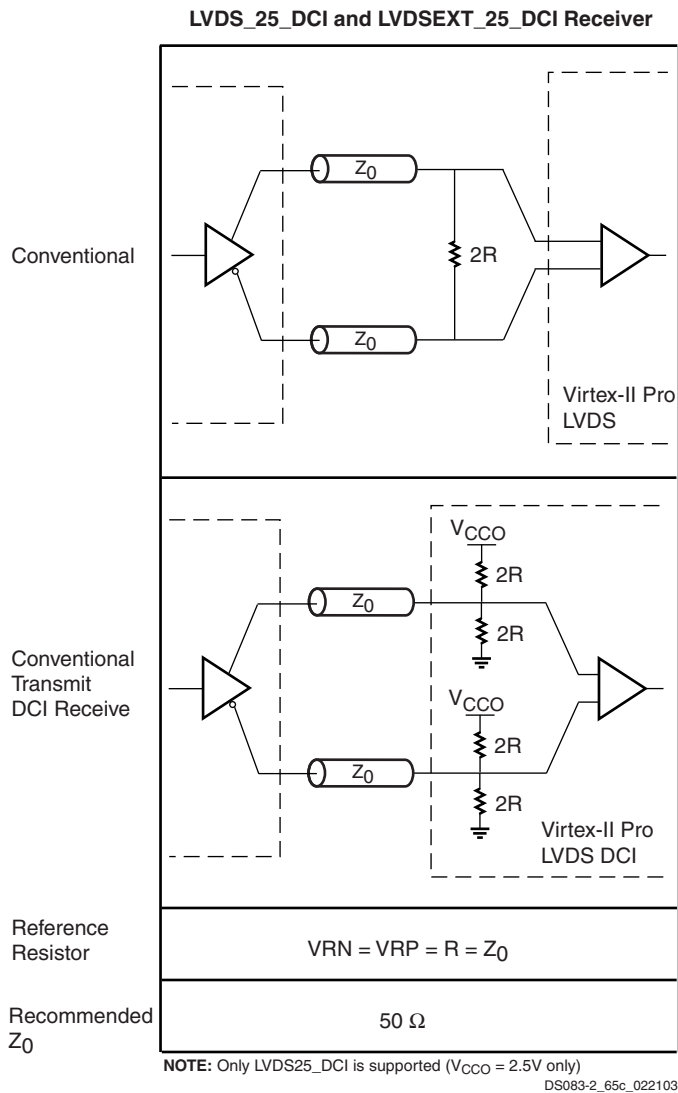


Figure 30: LVDS DCI Usage Examples

### On-Chip Differential Termination

Virtex-II Pro provides a true  $100\ \Omega$  differential termination (DT) across the input differential receiver terminals. The LVDS\_25\_DT, LVDSEXT\_25\_DT, LDT\_25\_DT, and ULVDS\_25\_DT standards support on-chip differential termination.

The on-chip input differential termination in Virtex-II Pro provides major advantages over the external resistor or the DCI termination solution:

- Eliminates the stub at the receiver completely and therefore greatly improve signal integrity
- Consumes less power than DCI termination
- Supports LDT (not supported by DCI termination)
- Frees up VRP/VRN pins

Figure 31 provides examples illustrating the use of the LVDS\_25\_DT, LVDSEXT\_25\_DT, LDT\_25\_DT, and ULVDS\_25\_DT I/O standards. For further details, refer to [Solution Record 17244](#). Also see the [Virtex-II Pro Platform FPGA User Guide](#) for more design information.

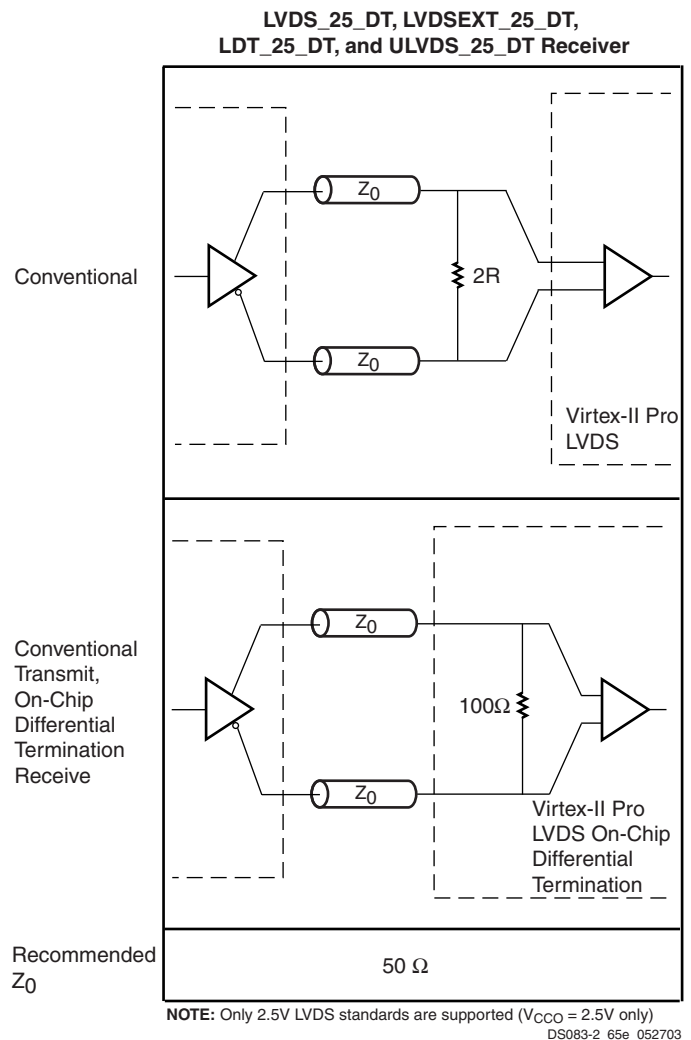


Figure 31: LVDS Differential Termination Usage Examples

### Master SelectMAP Mode

This mode is a master version of the SelectMAP mode. The device is configured byte-wide on a CCLK supplied by the Virtex-II Pro FPGA device. Timing is similar to the Slave SerialMAP mode except that CCLK is supplied by the Virtex-II Pro FPGA.

### Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II Pro device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP).

Virtex-II Pro device configuration using Boundary-Scan is compatible with IEEE 1149.1-1993 standard and the new IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol. Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

**Table 32: Virtex-II Pro Configuration Mode Pin Settings**

| Configuration Mode <sup>(1)</sup> | M2 | M1 | M0 | CCLK Direction | Data Width | Serial D <sub>OUT</sub> <sup>(2)</sup> |
|-----------------------------------|----|----|----|----------------|------------|----------------------------------------|
| Master Serial                     | 0  | 0  | 0  | Out            | 1          | Yes                                    |
| Slave Serial                      | 1  | 1  | 1  | In             | 1          | Yes                                    |
| Master SelectMAP                  | 0  | 1  | 1  | Out            | 8          | No                                     |
| Slave SelectMAP                   | 1  | 1  | 0  | In             | 8          | No                                     |
| Boundary-Scan                     | 1  | 0  | 1  | N/A            | 1          | No                                     |

#### Notes:

1. The HSWAP\_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP\_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D<sub>OUT</sub> is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

**Table 33** lists the default total number of bits required to configure each device.

**Table 33: Virtex-II Pro Default Bitstream Lengths**

| Device   | Number of Configuration Bits |
|----------|------------------------------|
| XC2VP2   | 1,305,376                    |
| XC2VP4   | 3,006,496                    |
| XC2VP7   | 4,485,408                    |
| XC2VP20  | 8,214,560                    |
| XC2VPX20 | 8,214,560                    |
| XC2VP30  | 11,589,920                   |
| XC2VP40  | 15,868,192                   |
| XC2VP50  | 19,021,344                   |
| XC2VP70  | 26,098,976                   |
| XC2VPX70 | 26,098,976                   |
| XC2VP100 | 34,292,768                   |

### Configuration Sequence

The configuration of Virtex-II Pro devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT\_B pin can be held Low using an open-drain driver. An open-drain is required since INIT\_B is a bidirectional open-drain pin that is held Low by a Virtex-II Pro FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG\_B pin. The end of the memory-clearing phase is signaled by the INIT\_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed via configuration options in software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start

Table 38: IOB Output Switching Characteristics Standard Adjustments (Continued)

| Description                                                  | IOSTANDARD Attribute | Timing Parameter              | Speed Grade |      |      | Units |
|--------------------------------------------------------------|----------------------|-------------------------------|-------------|------|------|-------|
|                                                              |                      |                               | -7          | -6   | -5   |       |
| HSTL, Class II                                               | HSTL_II              | T <sub>OHSTL_II</sub>         | 0.30        | 0.35 | 0.38 | ns    |
| HSTL, Class III                                              | HSTL_III             | T <sub>OHSTL_III</sub>        | 0.31        | 0.35 | 0.39 | ns    |
| HSTL, Class IV                                               | HSTL_IV              | T <sub>OHSTL_IV</sub>         | 0.15        | 0.17 | 0.19 | ns    |
| HSTL, Class I, 1.8V                                          | HSTL_I_18            | T <sub>OHSTL_I_18</sub>       | 0.56        | 0.64 | 0.70 | ns    |
| HSTL, Class II, 1.8V                                         | HSTL_II_18           | T <sub>OHSTL_II_18</sub>      | 0.30        | 0.35 | 0.38 | ns    |
| HSTL, Class III, 1.8V                                        | HSTL_III_18          | T <sub>OHSTL_III_18</sub>     | 0.36        | 0.41 | 0.45 | ns    |
| HSTL, Class IV, 1.8V                                         | HSTL_IV_18           | T <sub>OHSTL_IV_18</sub>      | 0.19        | 0.22 | 0.24 | ns    |
| SSTL (Stub Series Terminated Logic), Class I, 1.8V           | SSTL18_I             | T <sub>OSSTL18_I</sub>        | 0.80        | 0.92 | 1.01 | ns    |
| SSTL, Class II, 1.8V                                         | SSTL18_II            | T <sub>OSSTL18_II</sub>       | 0.45        | 0.51 | 0.56 | ns    |
| SSTL, Class I, 2.5V                                          | SSTL2_I              | T <sub>OSSTL2_I</sub>         | 0.63        | 0.72 | 0.79 | ns    |
| SSTL, Class II, 2.5V                                         | SSTL2_II             | T <sub>OSSTL2_II</sub>        | 0.22        | 0.25 | 0.27 | ns    |
| LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V     | LVDCI_33             | T <sub>OLVDCI_33</sub>        | 0.72        | 0.83 | 0.91 | ns    |
| LVDCI, 2.5V                                                  | LVDCI_25             | T <sub>OLVDCI_25</sub>        | 0.56        | 0.64 | 0.71 | ns    |
| LVDCI, 1.8V                                                  | LVDCI_18             | T <sub>OLVDCI_18</sub>        | 0.65        | 0.75 | 0.82 | ns    |
| LVDCI, 1.5V                                                  | LVDCI_15             | T <sub>OLVDCI_15</sub>        | 1.00        | 1.15 | 1.26 | ns    |
| LVDCI, 2.5V, Half-Impedance                                  | LVDCI_DV2_25         | T <sub>OLVDCI_DV2_25</sub>    | 0.06        | 0.07 | 0.08 | ns    |
| LVDCI, 1.8V, Half-Impedance                                  | LVDCI_DV2_18         | T <sub>OLVDCI_DV2_18</sub>    | 0.30        | 0.34 | 0.38 | ns    |
| LVDCI, 1.5V, Half-Impedance                                  | LVDCI_DV2_15         | T <sub>OLVDCI_DV2_15</sub>    | 0.60        | 0.69 | 0.76 | ns    |
| HSLVDCI (High-Speed Low-Voltage DCI), 1.5V                   | HSLVDCI_15           | T <sub>OHSLVDCI_15</sub>      | 1.00        | 1.15 | 1.26 | ns    |
| HSLVDCI, 1.8V                                                | HSLVDCI_18           | T <sub>OHSLVDCI_18</sub>      | 0.65        | 0.75 | 0.82 | ns    |
| HSLVDCI, 2.5V                                                | HSLVDCI_25           | T <sub>OHSLVDCI_25</sub>      | 0.56        | 0.64 | 0.71 | ns    |
| HSLVDCI, 3.3V                                                | HSLVDCI_33           | T <sub>OHSLVDCI_33</sub>      | 0.72        | 0.83 | 0.91 | ns    |
| GTL (Gunning Transceiver Logic) with DCI                     | GTL_DCI              | T <sub>OGTL_DCI</sub>         | 1.21        | 1.39 | 1.53 | ns    |
| GTL Plus with DCI                                            | GTL_P_DCI            | T <sub>OGTL_P_DCI</sub>       | 0.05        | 0.06 | 0.07 | ns    |
| HSTL (High-Speed Transceiver Logic), Class I, with DCI       | HSTL_I_DCI           | T <sub>OHSTL_I_DCI</sub>      | 0.55        | 0.63 | 0.69 | ns    |
| HSTL, Class II, with DCI                                     | HSTL_II_DCI          | T <sub>OHSTL_II_DCI</sub>     | 0.47        | 0.54 | 0.60 | ns    |
| HSTL, Class III, with DCI                                    | HSTL_III_DCI         | T <sub>OHSTL_III_DCI</sub>    | 0.31        | 0.36 | 0.40 | ns    |
| HSTL, Class IV, with DCI                                     | HSTL_IV_DCI          | T <sub>OHSTL_IV_DCI</sub>     | 1.81        | 2.08 | 2.29 | ns    |
| HSTL, Class I, 1.8V, with DCI                                | HSTL_I_DCI_18        | T <sub>OHSTL_I_DCI_18</sub>   | 0.55        | 0.63 | 0.70 | ns    |
| HSTL, Class II, 1.8V, with DCI                               | HSTL_II_DCI_18       | T <sub>OHSTL_II_DCI_18</sub>  | 0.24        | 0.28 | 0.31 | ns    |
| HSTL, Class III, 1.8V, with DCI                              | HSTL_III_DCI_18      | T <sub>OHSTL_III_DCI_18</sub> | 0.35        | 0.40 | 0.44 | ns    |
| HSTL, Class IV, 1.8V, with DCI                               | HSTL_IV_DCI_18       | T <sub>OHSTL_IV_DCI_18</sub>  | 1.48        | 1.70 | 1.87 | ns    |
| SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI | SSTL18_I_DCI         | T <sub>OSSTL18_I_DCI</sub>    | 0.54        | 0.62 | 0.68 | ns    |
| SSTL, Class II, 1.8V, with DCI                               | SSTL18_II_DCI        | T <sub>OSSTL18_II_DCI</sub>   | 0.24        | 0.28 | 0.31 | ns    |
| SSTL, Class I, 2.5V, with DCI                                | SSTL2_I_DCI          | T <sub>OSSTL2_I_DCI</sub>     | 0.48        | 0.56 | 0.61 | ns    |
| SSTL, Class II, 2.5V, with DCI                               | SSTL2_II_DCI         | T <sub>OSSTL2_II_DCI</sub>    | 0.48        | 0.56 | 0.61 | ns    |

## DCM Timing Parameters

All devices are 100% functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values

across the recommended operating conditions. All output jitter and phase specifications are determined through statistical measurement at the package pins.

## Operating Frequency Ranges

Table 57: Operating Frequency Ranges

|                                                |                       |             | Speed Grade |        |        |       |
|------------------------------------------------|-----------------------|-------------|-------------|--------|--------|-------|
| Description                                    | Symbol                | Constraints | -7          | -6     | -5     | Units |
| Output Clocks (Low Frequency Mode)             |                       |             |             |        |        |       |
| CLK0, CLK90, CLK180, CLK270                    | CLKOUT_FREQ_1X_LF_MIN |             | 24.00       | 24.00  | 24.00  | MHz   |
|                                                | CLKOUT_FREQ_1X_LF_MAX |             | 270.00      | 210.00 | 180.00 | MHz   |
| CLK2X, CLK2X180 <sup>(5,6)</sup>               | CLKOUT_FREQ_2X_LF_MIN |             | 48.00       | 48.00  | 48.00  | MHz   |
|                                                | CLKOUT_FREQ_2X_LF_MAX |             | 450.00      | 420.00 | 360.00 | MHz   |
| CLKDV                                          | CLKOUT_FREQ_DV_LF_MIN |             | 1.50        | 1.50   | 1.50   | MHz   |
|                                                | CLKOUT_FREQ_DV_LF_MAX |             | 140.00      | 140.00 | 120.00 | MHz   |
| CLKFX, CLKFX180                                | CLKOUT_FREQ_FX_LF_MIN |             | 24.00       | 24.00  | 24.00  | MHz   |
|                                                | CLKOUT_FREQ_FX_LF_MAX |             | 240.00      | 240.00 | 210.00 | MHz   |
| Input Clocks (Low Frequency Mode)              |                       |             |             |        |        |       |
| CLKIN (using DLL outputs) <sup>(1,3,4)</sup>   | CLKIN_FREQ_DLL_LF_MIN |             | 24.00       | 24.00  | 24.00  | MHz   |
|                                                | CLKIN_FREQ_DLL_LF_MAX |             | 270.00      | 210.00 | 180.00 | MHz   |
| CLKIN (using CLKFX outputs) <sup>(2,3,4)</sup> | CLKIN_FREQ_FX_LF_MIN  |             | 1.00        | 1.00   | 1.00   | MHz   |
|                                                | CLKIN_FREQ_FX_LF_MAX  |             | 240.00      | 240.00 | 210.00 | MHz   |
| PSCLK                                          | PSCLK_FREQ_LF_MIN     |             | 0.01        | 0.01   | 0.01   | MHz   |
|                                                | PSCLK_FREQ_LF_MAX     |             | 450.00      | 420.00 | 360.00 | MHz   |
| Output Clocks (High Frequency Mode)            |                       |             |             |        |        |       |
| CLK0, CLK180 <sup>(6)</sup>                    | CLKOUT_FREQ_1X_HF_MIN |             | 48.00       | 48.00  | 48.00  | MHz   |
|                                                | CLKOUT_FREQ_1X_HF_MAX |             | 450.00      | 420.00 | 360.00 | MHz   |
| CLKDV                                          | CLKOUT_FREQ_DV_HF_MIN |             | 3.00        | 3.00   | 3.00   | MHz   |
|                                                | CLKOUT_FREQ_DV_HF_MAX |             | 280.00      | 280.00 | 240.00 | MHz   |
| CLKFX, CLKFX180                                | CLKOUT_FREQ_FX_HF_MIN |             | 210.00      | 210.00 | 210.00 | MHz   |
|                                                | CLKOUT_FREQ_FX_HF_MAX |             | 320.00      | 320.00 | 270.00 | MHz   |
| Input Clocks (High Frequency Mode)             |                       |             |             |        |        |       |
| CLKIN (using DLL outputs) <sup>(1,3,4,6)</sup> | CLKIN_FREQ_DLL_HF_MIN |             | 48.00       | 48.00  | 48.00  | MHz   |
|                                                | CLKIN_FREQ_DLL_HF_MAX |             | 450.00      | 420.00 | 360.00 | MHz   |
| CLKIN (using CLKFX outputs) <sup>(2,3,4)</sup> | CLKIN_FREQ_FX_HF_MIN  |             | 50.00       | 50.00  | 50.00  | MHz   |
|                                                | CLKIN_FREQ_FX_HF_MAX  |             | 320.00      | 320.00 | 270.00 | MHz   |
| PSCLK                                          | PSCLK_FREQ_HF_MIN     |             | 0.01        | 0.01   | 0.01   | MHz   |
|                                                | PSCLK_FREQ_HF_MAX     |             | 450.00      | 420.00 | 360.00 | MHz   |

### Notes:

1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If the CLKIN\_DIVIDE\_BY\_2 attribute of the DCM is used, then double these values.
4. If the CLKIN\_DIVIDE\_BY\_2 attribute of the DCM is used and CLKIN frequency > 400 MHz, CLKIN duty cycle must be within  $\pm 5\%$  (45/55 to 55/45).
5. CLK2X and CLK2X180 may not be used as the input to the CLKFB pin. See the [Virtex-II Pro Platform FPGA User Guide](#) for more information.
6. For the XC2VP100 -6 device only, clock macros for corner DCMS (X0Y0, X5Y0, X0Y1, X5Y1) are required to operate at maximum clock frequency. See [XAPP685](#) for implementation examples.

Table 3: Virtex-II Pro Available I/Os and RocketIO MGT Pins per Device/Package Combination

| Virtex-II Pro Device | User I/Os & RocketIO MGT Pins | Virtex-II Pro Package <sup>(1)</sup> |               |               |       |       |        |        |        |        |        |
|----------------------|-------------------------------|--------------------------------------|---------------|---------------|-------|-------|--------|--------|--------|--------|--------|
|                      |                               | FG256/ FGG256                        | FG456/ FGG456 | FG676/ FGG456 | FF672 | FF896 | FF1152 | FF1148 | FF1517 | FF1704 | FF1696 |
| XC2VP2               | Available User I/Os           | 140                                  | 156           | -             | 204   | -     | -      | -      | -      | -      | -      |
|                      | RocketIO MGT Pins             | 36                                   | 36            | -             | 36    | -     | -      | -      | -      | -      | -      |
|                      | Differential I/O Pairs        | 68                                   | 76            | -             | 100   | -     | -      | -      | -      | -      | -      |
| XC2VP4               | Available User I/Os           | 140                                  | 248           | -             | 348   | -     | -      | -      | -      | -      | -      |
|                      | RocketIO MGT Pins             | 36                                   | 36            | -             | 36    | -     | -      | -      | -      | -      | -      |
|                      | Differential I/O Pairs        | 68                                   | 122           | -             | 172   | -     | -      | -      | -      | -      | -      |
| XC2VP7               | Available User I/Os           | -                                    | 248           | -             | 396   | 396   | -      | -      | -      | -      | -      |
|                      | RocketIO MGT Pins             | -                                    | 72            | -             | 72    | 72    | -      | -      | -      | -      | -      |
|                      | Differential I/O Pairs        | -                                    | 122           | -             | 196   | 196   | -      | -      | -      | -      | -      |
| XC2VP20              | Available User I/Os           | -                                    | -             | 404           | -     | 556   | 564    | -      | -      | -      | -      |
|                      | RocketIO MGT Pins             | -                                    | -             | 72            | -     | 72    | 72     | -      | -      | -      | -      |
|                      | Differential I/O Pairs        | -                                    | -             | 196           | -     | 272   | 276    | -      | -      | -      | -      |
| XC2VPX20             | Available User I/Os           | -                                    | -             | -             | -     | 552   | -      | -      | -      | -      | -      |
|                      | RocketIO X MGT Pins           | -                                    | -             | -             | -     | 72    | -      | -      | -      | -      | -      |
|                      | Differential I/O Pairs        | -                                    | -             | -             | -     | 270   | -      | -      | -      | -      | -      |
| XC2VP30              | Available User I/Os           | -                                    | -             | 416           | -     | 556   | 644    | -      | -      | -      | -      |
|                      | RocketIO MGT Pins             | -                                    | -             | 72            | -     | 72    | 72     | -      | -      | -      | -      |
|                      | Differential I/O Pairs        | -                                    | -             | 202           | -     | 272   | 316    | -      | -      | -      | -      |
| XC2VP40              | Available User I/Os           | -                                    | -             | 416           | -     | -     | 692    | 804    | -      | -      | -      |
|                      | RocketIO MGT Pins             | -                                    | -             | 72            | -     | -     | 108    | 0      | -      | -      | -      |
|                      | Differential I/O Pairs        | -                                    | -             | 202           | -     | -     | 340    | 396    | -      | -      | -      |
| XC2VP50              | Available User I/Os           | -                                    | -             | -             | -     | -     | 692    | 812    | 852    | -      | -      |
|                      | RocketIO MGT Pins             | -                                    | -             | -             | -     | -     | 144    | 0      | 144    | -      | -      |
|                      | Differential I/O Pairs        | -                                    | -             | -             | -     | -     | 340    | 400    | 420    | -      | -      |

## FG456/FGG456 Fine-Pitch BGA Package

As shown in Table 6, XC2VP2, XC2VP4, and XC2VP7 Virtex-II Pro devices are available in the FG456/FGG456 fine-pitch BGA package. The pins in these devices are same, except for the differences shown in the "No Connects" column. Following this table are the **FG456/FGG456 Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 6: FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7

| Bank | Pin Description  | Pin Number | No Connects |        |        |
|------|------------------|------------|-------------|--------|--------|
|      |                  |            | XC2VP2      | XC2VP4 | XC2VP7 |
| 0    | IO_L01N_0/VRP_0  | D5         |             |        |        |
| 0    | IO_L01P_0/VRN_0  | D6         |             |        |        |
| 0    | IO_L02N_0        | E6         |             |        |        |
| 0    | IO_L02P_0        | E7         |             |        |        |
| 0    | IO_L03N_0        | D7         |             |        |        |
| 0    | IO_L03P_0/VREF_0 | C7         |             |        |        |
| 0    | IO_L05_0/No_Pair | E8         |             |        |        |
| 0    | IO_L06N_0        | D8         |             |        |        |
| 0    | IO_L06P_0        | C8         |             |        |        |
| 0    | IO_L07N_0        | F9         |             |        |        |
| 0    | IO_L07P_0        | E9         |             |        |        |
| 0    | IO_L09N_0        | D9         |             |        |        |
| 0    | IO_L09P_0/VREF_0 | D10        |             |        |        |
| 0    | IO_L67N_0        | F10        |             |        |        |
| 0    | IO_L67P_0        | E10        |             |        |        |
| 0    | IO_L69N_0        | C10        |             |        |        |
| 0    | IO_L69P_0/VREF_0 | B11        |             |        |        |
| 0    | IO_L74N_0/GCLK7P | F11        |             |        |        |
| 0    | IO_L74P_0/GCLK6S | E11        |             |        |        |
| 0    | IO_L75N_0/GCLK5P | D11        |             |        |        |
| 0    | IO_L75P_0/GCLK4S | C11        |             |        |        |
|      |                  |            |             |        |        |
| 1    | IO_L75N_1/GCLK3P | C12        |             |        |        |
| 1    | IO_L75P_1/GCLK2S | D12        |             |        |        |
| 1    | IO_L74N_1/GCLK1P | E12        |             |        |        |
| 1    | IO_L74P_1/GCLK0S | F12        |             |        |        |
| 1    | IO_L69N_1/VREF_1 | B12        |             |        |        |
| 1    | IO_L69P_1        | C13        |             |        |        |
| 1    | IO_L67N_1        | E13        |             |        |        |
| 1    | IO_L67P_1        | F13        |             |        |        |
| 1    | IO_L09N_1/VREF_1 | D13        |             |        |        |
| 1    | IO_L09P_1        | D14        |             |        |        |
| 1    | IO_L07N_1        | E14        |             |        |        |

Table 7: FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40

| Bank | Pin Description  | Pin Number | No Connects |         |         |
|------|------------------|------------|-------------|---------|---------|
|      |                  |            | XC2VP20     | XC2VP30 | XC2VP40 |
| 6    | IO_L55P_6        | T2         |             |         |         |
| 6    | IO_L55N_6        | T1         |             |         |         |
| 6    | IO_L57P_6        | R9         |             |         |         |
| 6    | IO_L57N_6/VREF_6 | R8         |             |         |         |
| 6    | IO_L59P_6        | R6         |             |         |         |
| 6    | IO_L59N_6        | P6         |             |         |         |
| 6    | IO_L60P_6        | R5         |             |         |         |
| 6    | IO_L60N_6        | R4         |             |         |         |
| 6    | IO_L85P_6        | R2         |             |         |         |
| 6    | IO_L85N_6        | R1         |             |         |         |
| 6    | IO_L87P_6        | P9         |             |         |         |
| 6    | IO_L87N_6/VREF_6 | P8         |             |         |         |
| 6    | IO_L89P_6        | P5         |             |         |         |
| 6    | IO_L89N_6        | P4         |             |         |         |
| 6    | IO_L90P_6        | P3         |             |         |         |
| 6    | IO_L90N_6        | P2         |             |         |         |
|      |                  |            |             |         |         |
| 7    | IO_L90P_7        | N2         |             |         |         |
| 7    | IO_L90N_7        | N3         |             |         |         |
| 7    | IO_L88P_7        | N4         |             |         |         |
| 7    | IO_L88N_7/VREF_7 | N5         |             |         |         |
| 7    | IO_L86P_7        | N8         |             |         |         |
| 7    | IO_L86N_7        | N9         |             |         |         |
| 7    | IO_L85P_7        | M1         |             |         |         |
| 7    | IO_L85N_7        | M2         |             |         |         |
| 7    | IO_L60P_7        | M4         |             |         |         |
| 7    | IO_L60N_7        | M5         |             |         |         |
| 7    | IO_L58P_7        | N6         |             |         |         |
| 7    | IO_L58N_7/VREF_7 | M6         |             |         |         |
| 7    | IO_L56P_7        | M8         |             |         |         |
| 7    | IO_L56N_7        | M9         |             |         |         |
| 7    | IO_L55P_7        | L1         |             |         |         |
| 7    | IO_L55N_7        | L2         |             |         |         |
| 7    | IO_L54P_7        | L5         |             |         |         |
| 7    | IO_L54N_7        | L6         |             |         |         |

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

| Bank | Pin Description                    |                         | Pin Number | No Connects |                   |         |
|------|------------------------------------|-------------------------|------------|-------------|-------------------|---------|
|      | Virtex-II Pro devices              | XC2VPX20 (if Different) |            | XC2VP7      | XC2VP20, XC2VPX20 | XC2VP30 |
| 3    | IO_L39P_3                          |                         | AE2        | NC          |                   |         |
| 3    | IO_L38N_3                          |                         | AA7        | NC          |                   |         |
| 3    | IO_L38P_3                          |                         | AA8        | NC          |                   |         |
| 3    | IO_L37N_3                          |                         | AD3        | NC          |                   |         |
| 3    | IO_L37P_3                          |                         | AD4        | NC          |                   |         |
| 3    | IO_L36N_3                          |                         | AF1        | NC          |                   |         |
| 3    | IO_L36P_3                          |                         | AF2        | NC          |                   |         |
| 3    | IO_L35N_3                          |                         | AC5        | NC          |                   |         |
| 3    | IO_L35P_3                          |                         | AC6        | NC          |                   |         |
| 3    | IO_L34N_3                          |                         | AF3        | NC          |                   |         |
| 3    | IO_L34P_3                          |                         | AF4        | NC          |                   |         |
| 3    | IO_L33N_3/VREF_3                   |                         | AE3        | NC          |                   |         |
| 3    | IO_L33P_3                          |                         | AE4        | NC          |                   |         |
| 3    | IO_L32N_3                          |                         | AB7        | NC          |                   |         |
| 3    | IO_L32P_3                          |                         | AB8        | NC          |                   |         |
| 3    | IO_L31N_3                          |                         | AE5        | NC          |                   |         |
| 3    | IO_L31P_3                          |                         | AF6        | NC          |                   |         |
| 3    | IO_L06N_3                          |                         | AG1        |             |                   |         |
| 3    | IO_L06P_3                          |                         | AG2        |             |                   |         |
| 3    | IO_L05N_3                          |                         | AD5        |             |                   |         |
| 3    | IO_L05P_3                          |                         | AD6        |             |                   |         |
| 3    | IO_L04N_3                          |                         | AG3        |             |                   |         |
| 3    | IO_L04P_3                          |                         | AH4        |             |                   |         |
| 3    | IO_L03N_3/VREF_3                   |                         | AH1        |             |                   |         |
| 3    | IO_L03P_3                          |                         | AH2        |             |                   |         |
| 3    | IO_L02N_3                          |                         | AG5        |             |                   |         |
| 3    | IO_L02P_3                          |                         | AH5        |             |                   |         |
| 3    | IO_L01N_3/VRP_3                    |                         | AJ3        |             |                   |         |
| 3    | IO_L01P_3/VRN_3                    |                         | AK3        |             |                   |         |
|      |                                    |                         |            |             |                   |         |
| 4    | IO_L01N_4/BUSY/DOUT <sup>(1)</sup> |                         | AG6        |             |                   |         |
| 4    | IO_L01P_4/INIT_B                   |                         | AF7        |             |                   |         |
| 4    | IO_L02N_4/D0/DIN <sup>(1)</sup>    |                         | AC9        |             |                   |         |
| 4    | IO_L02P_4/D1                       |                         | AD9        |             |                   |         |
| 4    | IO_L03N_4/D2                       |                         | AG7        |             |                   |         |
| 4    | IO_L03P_4/D3                       |                         | AH7        |             |                   |         |

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

| Bank | Pin Description  | Pin Number | No Connects |         |         |         |
|------|------------------|------------|-------------|---------|---------|---------|
|      |                  |            | XC2VP20     | XC2VP30 | XC2VP40 | XC2VP50 |
| 7    | IO_L18N_7        | L25        | NC          |         |         |         |
| 7    | IO_L17P_7        | F34        | NC          |         |         |         |
| 7    | IO_L17N_7        | F33        | NC          |         |         |         |
| 7    | IO_L16P_7        | G30        | NC          |         |         |         |
| 7    | IO_L16N_7/VREF_7 | G29        | NC          |         |         |         |
| 7    | IO_L15P_7        | G32        | NC          |         |         |         |
| 7    | IO_L15N_7        | G31        | NC          |         |         |         |
| 7    | IO_L06P_7        | F31        |             |         |         |         |
| 7    | IO_L06N_7        | F30        |             |         |         |         |
| 7    | IO_L05P_7        | J28        |             |         |         |         |
| 7    | IO_L05N_7        | J27        |             |         |         |         |
| 7    | IO_L04P_7        | E34        |             |         |         |         |
| 7    | IO_L04N_7/VREF_7 | E33        |             |         |         |         |
| 7    | IO_L03P_7        | E32        |             |         |         |         |
| 7    | IO_L03N_7        | E31        |             |         |         |         |
| 7    | IO_L02P_7        | F28        |             |         |         |         |
| 7    | IO_L02N_7        | F27        |             |         |         |         |
| 7    | IO_L01P_7/VRN_7  | D34        |             |         |         |         |
| 7    | IO_L01N_7/VRP_7  | D33        |             |         |         |         |
|      |                  |            |             |         |         |         |
| 0    | VCCO_0           | C29        |             |         |         |         |
| 0    | VCCO_0           | E20        |             |         |         |         |
| 0    | VCCO_0           | F25        |             |         |         |         |
| 0    | VCCO_0           | L20        |             |         |         |         |
| 0    | VCCO_0           | L21        |             |         |         |         |
| 0    | VCCO_0           | L22        |             |         |         |         |
| 0    | VCCO_0           | L23        |             |         |         |         |
| 0    | VCCO_0           | M18        |             |         |         |         |
| 0    | VCCO_0           | M19        |             |         |         |         |
| 0    | VCCO_0           | M20        |             |         |         |         |
| 0    | VCCO_0           | M21        |             |         |         |         |
| 0    | VCCO_0           | M22        |             |         |         |         |
| 1    | VCCO_1           | C6         |             |         |         |         |
| 1    | VCCO_1           | E15        |             |         |         |         |
| 1    | VCCO_1           | F10        |             |         |         |         |
| 1    | VCCO_1           | L12        |             |         |         |         |
| 1    | VCCO_1           | L13        |             |         |         |         |
| 1    | VCCO_1           | L14        |             |         |         |         |

Table 11: FF1148 — XC2VP40 and XC2VP50

| Bank | Pin Description  | Pin Number | No Connects |         |
|------|------------------|------------|-------------|---------|
|      |                  |            | XC2VP40     | XC2VP50 |
| 2    | IO_L40P_2        | K3         |             |         |
| 2    | IO_L41N_2        | R9         |             |         |
| 2    | IO_L41P_2        | P9         |             |         |
| 2    | IO_L42N_2        | K1         |             |         |
| 2    | IO_L42P_2        | K2         |             |         |
| 2    | IO_L43N_2        | L5         |             |         |
| 2    | IO_L43P_2        | L6         |             |         |
| 2    | IO_L44N_2        | P7         |             |         |
| 2    | IO_L44P_2        | P8         |             |         |
| 2    | IO_L45N_2        | L1         |             |         |
| 2    | IO_L45P_2        | L2         |             |         |
| 2    | IO_L46N_2/VREF_2 | M5         |             |         |
| 2    | IO_L46P_2        | M6         |             |         |
| 2    | IO_L47N_2        | R10        |             |         |
| 2    | IO_L47P_2        | R11        |             |         |
| 2    | IO_L48N_2        | M3         |             |         |
| 2    | IO_L48P_2        | M4         |             |         |
| 2    | IO_L49N_2        | M1         |             |         |
| 2    | IO_L49P_2        | M2         |             |         |
| 2    | IO_L50N_2        | R7         |             |         |
| 2    | IO_L50P_2        | T8         |             |         |
| 2    | IO_L51N_2        | P4         |             |         |
| 2    | IO_L51P_2        | N4         |             |         |
| 2    | IO_L52N_2/VREF_2 | N2         |             |         |
| 2    | IO_L52P_2        | N3         |             |         |
| 2    | IO_L53N_2        | T10        |             |         |
| 2    | IO_L53P_2        | T11        |             |         |
| 2    | IO_L54N_2        | P5         |             |         |
| 2    | IO_L54P_2        | P6         |             |         |
| 2    | IO_L55N_2        | R3         |             |         |
| 2    | IO_L55P_2        | P3         |             |         |
| 2    | IO_L56N_2        | T6         |             |         |
| 2    | IO_L56P_2        | T7         |             |         |
| 2    | IO_L57N_2        | P1         |             |         |
| 2    | IO_L57P_2        | P2         |             |         |
| 2    | IO_L58N_2/VREF_2 | R5         |             |         |
| 2    | IO_L58P_2        | R6         |             |         |
| 2    | IO_L59N_2        | U10        |             |         |

Table 11: FF1148 — XC2VP40 and XC2VP50

| Bank | Pin Description  | Pin Number | No Connects |         |
|------|------------------|------------|-------------|---------|
|      |                  |            | XC2VP40     | XC2VP50 |
| 7    | IO_L32P_7        | N24        |             |         |
| 7    | IO_L32N_7        | N25        |             |         |
| 7    | IO_L31P_7        | G33        |             |         |
| 7    | IO_L31N_7        | G34        |             |         |
| 7    | IO_L30P_7        | H31        |             |         |
| 7    | IO_L30N_7        | G32        |             |         |
| 7    | IO_L29P_7        | N27        |             |         |
| 7    | IO_L29N_7        | M28        |             |         |
| 7    | IO_L28P_7        | G28        |             |         |
| 7    | IO_L28N_7/VREF_7 | G29        |             |         |
| 7    | IO_L27P_7        | F33        |             |         |
| 7    | IO_L27N_7        | F34        |             |         |
| 7    | IO_L26P_7        | M26        |             |         |
| 7    | IO_L26N_7        | M27        |             |         |
| 7    | IO_L25P_7        | F31        |             |         |
| 7    | IO_L25N_7        | F32        |             |         |
| 7    | IO_L24P_7        | F30        |             |         |
| 7    | IO_L24N_7        | G30        |             |         |
| 7    | IO_L23P_7        | L25        |             |         |
| 7    | IO_L23N_7        | M25        |             |         |
| 7    | IO_L22P_7        | F27        |             |         |
| 7    | IO_L22N_7/VREF_7 | F28        |             |         |
| 7    | IO_L21P_7        | E29        |             |         |
| 7    | IO_L21N_7        | F29        |             |         |
| 7    | IO_L20P_7        | L28        |             |         |
| 7    | IO_L20N_7        | K28        |             |         |
| 7    | IO_L19P_7        | D33        |             |         |
| 7    | IO_L19N_7        | D34        |             |         |
| 7    | IO_L18P_7        | D32        |             |         |
| 7    | IO_L18N_7        | E32        |             |         |
| 7    | IO_L17P_7        | K26        |             |         |
| 7    | IO_L17N_7        | L26        |             |         |
| 7    | IO_L16P_7        | D31        |             |         |
| 7    | IO_L16N_7/VREF_7 | E31        |             |         |
| 7    | IO_L15P_7        | D29        |             |         |
| 7    | IO_L15N_7        | D30        |             |         |
| 7    | IO_L14P_7        | J28        |             |         |
| 7    | IO_L14N_7        | J29        |             |         |

Table 12: FF1517 — XC2VP50 and XC2VP70

| Bank | Pin Description  | Pin Number | No Connects |         |
|------|------------------|------------|-------------|---------|
|      |                  |            | XC2VP50     | XC2VP70 |
| 3    | IO_L90P_3        | AA8        |             |         |
| 3    | IO_L89N_3        | Y11        |             |         |
| 3    | IO_L89P_3        | Y12        |             |         |
| 3    | IO_L88N_3        | AA5        |             |         |
| 3    | IO_L88P_3        | AA6        |             |         |
| 3    | IO_L87N_3/VREF_3 | AA3        |             |         |
| 3    | IO_L87P_3        | AA4        |             |         |
| 3    | IO_L86N_3        | Y13        |             |         |
| 3    | IO_L86P_3        | AA13       |             |         |
| 3    | IO_L85N_3        | AB7        |             |         |
| 3    | IO_L85P_3        | AB8        |             |         |
| 3    | IO_L60N_3        | AB5        |             |         |
| 3    | IO_L60P_3        | AB6        |             |         |
| 3    | IO_L59N_3        | AA9        |             |         |
| 3    | IO_L59P_3        | AA10       |             |         |
| 3    | IO_L58N_3        | AB3        |             |         |
| 3    | IO_L58P_3        | AB4        |             |         |
| 3    | IO_L57N_3/VREF_3 | AB1        |             |         |
| 3    | IO_L57P_3        | AB2        |             |         |
| 3    | IO_L56N_3        | AA11       |             |         |
| 3    | IO_L56P_3        | AA12       |             |         |
| 3    | IO_L55N_3        | AC5        |             |         |
| 3    | IO_L55P_3        | AC6        |             |         |
| 3    | IO_L54N_3        | AC1        |             |         |
| 3    | IO_L54P_3        | AC2        |             |         |
| 3    | IO_L53N_3        | AB9        |             |         |
| 3    | IO_L53P_3        | AB10       |             |         |
| 3    | IO_L52N_3        | AC8        |             |         |
| 3    | IO_L52P_3        | AD8        |             |         |
| 3    | IO_L51N_3/VREF_3 | AC4        |             |         |
| 3    | IO_L51P_3        | AD4        |             |         |
| 3    | IO_L50N_3        | AB11       |             |         |
| 3    | IO_L50P_3        | AB12       |             |         |
| 3    | IO_L49N_3        | AD6        |             |         |
| 3    | IO_L49P_3        | AD7        |             |         |
| 3    | IO_L48N_3        | AD2        |             |         |
| 3    | IO_L48P_3        | AD3        |             |         |
| 3    | IO_L47N_3        | AC9        |             |         |

Table 12: FF1517 — XC2VP50 and XC2VP70

| Bank | Pin Description  | Pin Number | No Connects |         |
|------|------------------|------------|-------------|---------|
|      |                  |            | XC2VP50     | XC2VP70 |
| 6    | IO_L04P_6        | AR33       |             |         |
| 6    | IO_L04N_6        | AP33       |             |         |
| 6    | IO_L05P_6        | AM32       |             |         |
| 6    | IO_L05N_6        | AL31       |             |         |
| 6    | IO_L06P_6        | AT34       |             |         |
| 6    | IO_L06N_6        | AR34       |             |         |
| 6    | IO_L73P_6        | AU35       | NC          |         |
| 6    | IO_L73N_6        | AT35       | NC          |         |
| 6    | IO_L75P_6        | AT38       | NC          |         |
| 6    | IO_L75N_6/VREF_6 | AT39       | NC          |         |
| 6    | IO_L76P_6        | AR37       | NC          |         |
| 6    | IO_L76N_6        | AR38       | NC          |         |
| 6    | IO_L78P_6        | AP38       | NC          |         |
| 6    | IO_L78N_6        | AP39       | NC          |         |
| 6    | IO_L79P_6        | AP36       | NC          |         |
| 6    | IO_L79N_6        | AP37       | NC          |         |
| 6    | IO_L81P_6        | AP35       | NC          |         |
| 6    | IO_L81N_6/VREF_6 | AN35       | NC          |         |
| 6    | IO_L82P_6        | AN38       | NC          |         |
| 6    | IO_L82N_6        | AN39       | NC          |         |
| 6    | IO_L84P_6        | AN36       | NC          |         |
| 6    | IO_L84N_6        | AN37       | NC          |         |
| 6    | IO_L07P_6        | AN33       |             |         |
| 6    | IO_L07N_6        | AN34       |             |         |
| 6    | IO_L08P_6        | AK31       |             |         |
| 6    | IO_L08N_6        | AK32       |             |         |
| 6    | IO_L09P_6        | AM37       |             |         |
| 6    | IO_L09N_6/VREF_6 | AM38       |             |         |
| 6    | IO_L10P_6        | AM36       |             |         |
| 6    | IO_L10N_6        | AL35       |             |         |
| 6    | IO_L11P_6        | AJ31       |             |         |
| 6    | IO_L11N_6        | AH30       |             |         |
| 6    | IO_L12P_6        | AM33       |             |         |
| 6    | IO_L12N_6        | AM34       |             |         |
| 6    | IO_L13P_6        | AL38       |             |         |
| 6    | IO_L13N_6        | AL39       |             |         |
| 6    | IO_L14P_6        | AH29       |             |         |
| 6    | IO_L14N_6        | AG29       |             |         |

Table 12: FF1517 — XC2VP50 and XC2VP70

| Bank | Pin Description | Pin Number | No Connects |         |
|------|-----------------|------------|-------------|---------|
|      |                 |            | XC2VP50     | XC2VP70 |
| N/A  | GND             | W18        |             |         |
| N/A  | GND             | V18        |             |         |
| N/A  | GND             | U18        |             |         |
| N/A  | GND             | T18        |             |         |
| N/A  | GND             | AD17       |             |         |
| N/A  | GND             | AC17       |             |         |
| N/A  | GND             | AB17       |             |         |
| N/A  | GND             | AA17       |             |         |
| N/A  | GND             | Y17        |             |         |
| N/A  | GND             | W17        |             |         |
| N/A  | GND             | V17        |             |         |
| N/A  | GND             | U17        |             |         |
| N/A  | GND             | P20        |             |         |
| N/A  | GND             | L20        |             |         |
| N/A  | GND             | G20        |             |         |
| N/A  | GND             | C20        |             |         |
| N/A  | GND             | AD19       |             |         |
| N/A  | GND             | AC19       |             |         |
| N/A  | GND             | AB19       |             |         |
| N/A  | GND             | AA19       |             |         |
| N/A  | GND             | Y19        |             |         |
| N/A  | GND             | W19        |             |         |
| N/A  | GND             | V19        |             |         |
| N/A  | GND             | U19        |             |         |
| N/A  | GND             | T19        |             |         |
| N/A  | GND             | AD18       |             |         |
| N/A  | GND             | AC18       |             |         |
| N/A  | GND             | U21        |             |         |
| N/A  | GND             | T21        |             |         |
| N/A  | GND             | AU20       |             |         |
| N/A  | GND             | AN20       |             |         |
| N/A  | GND             | AJ20       |             |         |
| N/A  | GND             | AF20       |             |         |
| N/A  | GND             | AD20       |             |         |
| N/A  | GND             | AC20       |             |         |
| N/A  | GND             | AB20       |             |         |
| N/A  | GND             | AA20       |             |         |
| N/A  | GND             | Y20        |             |         |

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

| Bank | Pin Description       |                            | Pin Number | No Connects          |          |
|------|-----------------------|----------------------------|------------|----------------------|----------|
|      | Virtex-II Pro Devices | XC2VPX70<br>(if Different) |            | XC2VP70,<br>XC2VPX70 | XC2VP100 |
| 1    | IO_L30P_1             |                            | G13        |                      |          |
| 1    | IO_L29N_1             |                            | K13        |                      |          |
| 1    | IO_L29P_1             |                            | J13        |                      |          |
| 1    | IO_L28N_1             |                            | M13        |                      |          |
| 1    | IO_L28P_1             |                            | L13        |                      |          |
| 1    | IO_L27N_1/VREF_1      |                            | E12        |                      |          |
| 1    | IO_L27P_1             |                            | D12        |                      |          |
| 1    | IO_L26N_1             |                            | F12        |                      |          |
| 1    | IO_L26P_1             |                            | G12        |                      |          |
| 1    | IO_L25N_1             |                            | J12        |                      |          |
| 1    | IO_L25P_1             |                            | H12        |                      |          |
| 1    | IO_L21N_1             |                            | L12        |                      |          |
| 1    | IO_L21P_1             |                            | K12        |                      |          |
| 1    | IO_L20N_1             |                            | C11        |                      |          |
| 1    | IO_L20P_1             |                            | C10        |                      |          |
| 1    | IO_L19N_1             |                            | F11        |                      |          |
| 1    | IO_L19P_1             |                            | E11        |                      |          |
| 1    | IO_L09N_1/VREF_1      |                            | J11        |                      |          |
| 1    | IO_L09P_1             |                            | H11        |                      |          |
| 1    | IO_L08N_1             |                            | D10        |                      |          |
| 1    | IO_L08P_1             |                            | E10        |                      |          |
| 1    | IO_L07N_1             |                            | G10        |                      |          |
| 1    | IO_L07P_1             |                            | F10        |                      |          |
| 1    | IO_L06N_1             |                            | J10        |                      |          |
| 1    | IO_L06P_1             |                            | H10        |                      |          |
| 1    | IO_L05_1/No_Pair      |                            | K11        |                      |          |
| 1    | IO_L03N_1/VREF_1      |                            | D9         |                      |          |
| 1    | IO_L03P_1             |                            | C9         |                      |          |
| 1    | IO_L02N_1             |                            | E9         |                      |          |
| 1    | IO_L02P_1             |                            | F9         |                      |          |
| 1    | IO_L01N_1/VRP_1       |                            | H9         |                      |          |
| 1    | IO_L01P_1/VRN_1       |                            | G9         |                      |          |
|      |                       |                            |            |                      |          |
| 2    | IO_L01N_2/VRP_2       |                            | C5         |                      |          |
| 2    | IO_L01P_2/VRN_2       |                            | C6         |                      |          |
| 2    | IO_L02N_2             |                            | E7         |                      |          |

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

| Bank | Pin Description                    |                            | Pin Number | No Connects          |          |
|------|------------------------------------|----------------------------|------------|----------------------|----------|
|      | Virtex-II Pro Devices              | XC2VPX70<br>(if Different) |            | XC2VP70,<br>XC2VPX70 | XC2VP100 |
| 3    | IO_L77N_3                          |                            | AT3        |                      |          |
| 3    | IO_L77P_3                          |                            | AT4        |                      |          |
| 3    | IO_L76N_3                          |                            | AU1        |                      |          |
| 3    | IO_L76P_3                          |                            | AU2        |                      |          |
| 3    | IO_L75N_3/VREF_3                   |                            | AU3        |                      |          |
| 3    | IO_L75P_3                          |                            | AU4        |                      |          |
| 3    | IO_L74N_3                          |                            | AV3        |                      |          |
| 3    | IO_L74P_3                          |                            | AW3        |                      |          |
| 3    | IO_L73N_3                          |                            | AV1        |                      |          |
| 3    | IO_L73P_3                          |                            | AV2        |                      |          |
| 3    | IO_L06N_3                          |                            | AW1        |                      |          |
| 3    | IO_L06P_3                          |                            | AW2        |                      |          |
| 3    | IO_L05N_3                          |                            | AT8        |                      |          |
| 3    | IO_L05P_3                          |                            | AU8        |                      |          |
| 3    | IO_L04N_3                          |                            | AT6        |                      |          |
| 3    | IO_L04P_3                          |                            | AU7        |                      |          |
| 3    | IO_L03N_3/VREF_3                   |                            | AY5        |                      |          |
| 3    | IO_L03P_3                          |                            | AY6        |                      |          |
| 3    | IO_L02N_3                          |                            | AV7        |                      |          |
| 3    | IO_L02P_3                          |                            | AW7        |                      |          |
| 3    | IO_L01N_3/VRP_3                    |                            | AV6        |                      |          |
| 3    | IO_L01P_3/VRN_3                    |                            | AW6        |                      |          |
|      |                                    |                            |            |                      |          |
| 4    | IO_L01N_4/BUSY/DOUT <sup>(1)</sup> |                            | AT9        |                      |          |
| 4    | IO_L01P_4/INIT_B                   |                            | AR9        |                      |          |
| 4    | IO_L02N_4/D0/DIN <sup>(1)</sup>    |                            | AU9        |                      |          |
| 4    | IO_L02P_4/D1                       |                            | AV9        |                      |          |
| 4    | IO_L03N_4/D2                       |                            | AY9        |                      |          |
| 4    | IO_L03P_4/D3                       |                            | AW9        |                      |          |
| 4    | IO_L05_4/No_Pair                   |                            | AN11       |                      |          |
| 4    | IO_L06N_4/VRP_4                    |                            | AR10       |                      |          |
| 4    | IO_L06P_4/VRN_4                    |                            | AP10       |                      |          |
| 4    | IO_L07N_4                          |                            | AU10       |                      |          |
| 4    | IO_L07P_4/VREF_4                   |                            | AT10       |                      |          |
| 4    | IO_L08N_4                          |                            | AV10       |                      |          |
| 4    | IO_L08P_4                          |                            | AW10       |                      |          |

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

| Bank | Pin Description       |                            | Pin Number | No Connects          |          |
|------|-----------------------|----------------------------|------------|----------------------|----------|
|      | Virtex-II Pro Devices | XC2VPX70<br>(if Different) |            | XC2VP70,<br>XC2VPX70 | XC2VP100 |
| 5    | IO_L37N_5             |                            | AU28       |                      |          |
| 5    | IO_L37P_5             |                            | AV28       |                      |          |
| 5    | IO_L87N_5/VREF_5      |                            | AP28       | NC                   |          |
| 5    | IO_L87P_5             |                            | AR28       | NC                   |          |
| 5    | IO_L86N_5             |                            | AN28       | NC                   |          |
| 5    | IO_L86P_5             |                            | AM28       | NC                   |          |
| 5    | IO_L85N_5             |                            | AV29       | NC                   |          |
| 5    | IO_L85P_5             |                            | AW29       | NC                   |          |
| 5    | IO_L84N_5             |                            | AT29       | NC                   |          |
| 5    | IO_L84P_5             |                            | AU29       | NC                   |          |
| 5    | IO_L83_5/No_Pair      |                            | AR29       | NC                   |          |
| 5    | IO_L78N_5             |                            | AM29       | NC                   |          |
| 5    | IO_L78P_5             |                            | AN29       | NC                   |          |
| 5    | IO_L36N_5/VREF_5      |                            | AL29       |                      |          |
| 5    | IO_L36P_5             |                            | AL28       |                      |          |
| 5    | IO_L35N_5             |                            | AY30       |                      |          |
| 5    | IO_L35P_5             |                            | AW30       |                      |          |
| 5    | IO_L34N_5             |                            | AU30       |                      |          |
| 5    | IO_L34P_5             |                            | AV30       |                      |          |
| 5    | IO_L30N_5             |                            | AR30       |                      |          |
| 5    | IO_L30P_5             |                            | AT30       |                      |          |
| 5    | IO_L29N_5             |                            | AN30       |                      |          |
| 5    | IO_L29P_5             |                            | AP30       |                      |          |
| 5    | IO_L28N_5             |                            | AL30       |                      |          |
| 5    | IO_L28P_5             |                            | AM30       |                      |          |
| 5    | IO_L27N_5/VREF_5      |                            | AV31       |                      |          |
| 5    | IO_L27P_5             |                            | AW31       |                      |          |
| 5    | IO_L26N_5             |                            | AU31       |                      |          |
| 5    | IO_L26P_5             |                            | AT31       |                      |          |
| 5    | IO_L25N_5             |                            | AP31       |                      |          |
| 5    | IO_L25P_5             |                            | AR31       |                      |          |
| 5    | IO_L21N_5             |                            | AM31       |                      |          |
| 5    | IO_L21P_5             |                            | AN31       |                      |          |
| 5    | IO_L20N_5             |                            | AY32       |                      |          |
| 5    | IO_L20P_5             |                            | AY33       |                      |          |
| 5    | IO_L19N_5             |                            | AU32       |                      |          |

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

| Bank | Pin Description       |                            | Pin Number | No Connects          |          |
|------|-----------------------|----------------------------|------------|----------------------|----------|
|      | Virtex-II Pro Devices | XC2VPX70<br>(if Different) |            | XC2VP70,<br>XC2VPX70 | XC2VP100 |
| 6    | IO_L76N_6             |                            | AU42       |                      |          |
| 6    | IO_L77P_6             |                            | AT39       |                      |          |
| 6    | IO_L77N_6             |                            | AT40       |                      |          |
| 6    | IO_L78P_6             |                            | AT41       |                      |          |
| 6    | IO_L78N_6             |                            | AT42       |                      |          |
| 6    | IO_L79P_6             |                            | AR38       |                      |          |
| 6    | IO_L79N_6             |                            | AR39       |                      |          |
| 6    | IO_L80P_6             |                            | AR37       |                      |          |
| 6    | IO_L80N_6             |                            | AT38       |                      |          |
| 6    | IO_L81P_6             |                            | AR40       |                      |          |
| 6    | IO_L81N_6/VREF_6      |                            | AR41       |                      |          |
| 6    | IO_L82P_6             |                            | AP36       |                      |          |
| 6    | IO_L82N_6             |                            | AP37       |                      |          |
| 6    | IO_L83P_6             |                            | AP35       |                      |          |
| 6    | IO_L83N_6             |                            | AR36       |                      |          |
| 6    | IO_L84P_6             |                            | AP38       |                      |          |
| 6    | IO_L84N_6             |                            | AP39       |                      |          |
| 6    | IO_L07P_6             |                            | AP41       |                      |          |
| 6    | IO_L07N_6             |                            | AP42       |                      |          |
| 6    | IO_L08P_6             |                            | AN35       |                      |          |
| 6    | IO_L08N_6             |                            | AN36       |                      |          |
| 6    | IO_L09P_6             |                            | AN37       |                      |          |
| 6    | IO_L09N_6/VREF_6      |                            | AN38       |                      |          |
| 6    | IO_L10P_6             |                            | AN41       |                      |          |
| 6    | IO_L10N_6             |                            | AN42       |                      |          |
| 6    | IO_L11P_6             |                            | AM33       |                      |          |
| 6    | IO_L11N_6             |                            | AN34       |                      |          |
| 6    | IO_L12P_6             |                            | AM36       |                      |          |
| 6    | IO_L12N_6             |                            | AM37       |                      |          |
| 6    | IO_L13P_6             |                            | AM38       |                      |          |
| 6    | IO_L13N_6             |                            | AM39       |                      |          |
| 6    | IO_L14P_6             |                            | AM34       |                      |          |
| 6    | IO_L14N_6             |                            | AM35       |                      |          |
| 6    | IO_L15P_6             |                            | AN40       |                      |          |
| 6    | IO_L15N_6/VREF_6      |                            | AM40       |                      |          |
| 6    | IO_L16P_6             |                            | AM41       |                      |          |

Table 14: FF1696 — XC2VP100

| Bank | Pin Description | Pin Number | No Connects |
|------|-----------------|------------|-------------|
|      |                 |            | XC2VP100    |
| N/A  | GND             | AF1        |             |
| N/A  | GND             | AC1        |             |
| N/A  | GND             | Y1         |             |
| N/A  | GND             | U1         |             |
| N/A  | GND             | N1         |             |
| N/A  | GND             | J1         |             |
| N/A  | GND             | E1         |             |

**Notes:**

1. See [Table 4](#) for an explanation of the signals available on this pin.