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Understanding Embedded - FPGAs (Field Programmable Gate Array)

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	3424
Number of Logic Elements/Cells	30816
Total RAM Bits	2506752
Number of I/O	644
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp30-7ff1152c



Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview

DS083 (v5.0) June 21, 2011

Product Specification

Summary of Virtex-II Pro™ / Virtex-II Pro X Features

- High-Performance Platform FPGA Solution, Including
 - Up to twenty RocketIO™ or RocketIO X embedded Multi-Gigabit Transceivers (MGTS)
 - Up to two IBM PowerPC™ RISC processor blocks
- Based on Virtex-II™ Platform FPGA Technology
 - Flexible logic resources
 - SRAM-based in-system configuration
 - Active Interconnect technology
- SelectRAM™+ memory hierarchy
- Dedicated 18-bit x 18-bit multiplier blocks
- High-performance clock management circuitry
- SelectIO™-Ultra technology
- XCITE Digitally Controlled Impedance (DCI) I/O

Virtex-II Pro / Virtex-II Pro X family members and resources are shown in [Table 1](#).

Table 1: Virtex-II Pro / Virtex-II Pro X FPGA Family Members

Device ⁽¹⁾	RocketIO Transceiver Blocks	PowerPC Processor Blocks	Logic Cells ⁽²⁾	CLB (1 = 4 slices = max 128 bits)		18 X 18 Bit Multiplier Blocks	Block SelectRAM+		DCMs	Maximum User I/O Pads
				Slices	Max Distr RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)		
XC2VP2	4	0	3,168	1,408	44	12	12	216	4	204
XC2VP4	4	1	6,768	3,008	94	28	28	504	4	348
XC2VP7	8	1	11,088	4,928	154	44	44	792	4	396
XC2VP20	8	2	20,880	9,280	290	88	88	1,584	8	564
XC2VPX20	8 ⁽⁴⁾	1	22,032	9,792	306	88	88	1,584	8	552
XC2VP30	8	2	30,816	13,696	428	136	136	2,448	8	644
XC2VP40	0 ⁽³⁾ , 8, or 12	2	43,632	19,392	606	192	192	3,456	8	804
XC2VP50	0 ⁽³⁾ or 16	2	53,136	23,616	738	232	232	4,176	8	852
XC2VP70	16 or 20	2	74,448	33,088	1,034	328	328	5,904	8	996
XC2VPX70	20 ⁽⁴⁾	2	74,448	33,088	1,034	308	308	5,544	8	992
XC2VP100	0 ⁽³⁾ or 20	2	99,216	44,096	1,378	444	444	7,992	12	1,164

Notes:

- 7 speed grade devices are not available in Industrial grade.
- Logic Cell ≈ (1) 4-input LUT + (1)FF + Carry Logic
- These devices can be ordered in a configuration without RocketIO transceivers. See [Table 3](#) for package configurations.
- Virtex-II Pro X devices equipped with RocketIO X transceiver cores.

RocketIO X Transceiver Features (XC2VPX20 and XC2VPX70 Only)

- Variable-Speed Full-Duplex Transceiver (XC2VPX20) Allowing 2.488 Gb/s to 6.25 Gb/s Baud Transfer Rates.
 - Includes specific baud rates used by various standards, as listed in [Table 4, Module 2](#).
- Fixed-Speed Full-Duplex Transceiver (XC2VPX70) Operating at 4.25 Gb/s Baud Transfer Rate.
- Eight or Twenty Transceiver Modules on an FPGA, Depending upon Device
- Monolithic Clock Synthesis and Clock Recovery
 - Eliminates the need for external components
- Automatic Lock-to-Reference Function
- Programmable Serial Output Differential Swing
 - 200 mV to 1600 mV, peak-peak
 - Allows compatibility with other serial system voltage levels
- Programmable Pre-emphasis Levels 0 to 500%
- Telecom/Datacom Support Modes
 - "x8" and "x10" clocking/data paths
 - 64B/66B clocking support

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.
06/13/02	2.0	New Virtex-II Pro family members. New timing parameters per speedsfile v1.62 .
09/03/02	2.1	Updates to Table 1 and Table 3 . Processor Block information added to Table 4 .
09/27/02	2.2	In Table 1 , correct max number of XC2VP30 I/Os to 644.
11/20/02	2.3	Add bullet items for 3.3V I/O features.
01/20/03	2.4	- In Table 3, add FG676 package option for XC2VP20, XC2VP30, and XC2VP40. - Remove FF1517 package option for XC2VP40.
03/24/03	2.4.1	- Correct number of single-ended I/O standards from 19 to 22. - Correct minimum RocketIO serial speed from 622 Mbps to 600 Mbps.
08/25/03	2.4.2	Add footnote referring to XAPP659 to callout for 3.3V I/O standards on page 4.
12/10/03	3.0	XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to Production status.
02/19/04	3.1	Table 1: Corrected number of RocketIO transceiver blocks for XC2VP40. - Section Virtex-II Pro Platform FPGA Technology (All Devices): Updated number of differential standards supported from six to ten. - Section Input/Output Blocks (IOBs): Added text stating that differential termination is available for LVDS, LVDS Extended, ULVDS, and LDT standards. Figure 1: Added note stating that -7 devices are not available in Industrial grade.
03/09/04	3.1.1	Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/30/04	4.0	Merged in DS110-1 (Module 1 of Virtex-II Pro X data sheet). Added information on available Pb-free packages.
11/17/04	4.1	<i>No changes in Module 1 for this revision.</i>
03/01/05	4.2	Table 3 : Corrected number of RocketIO transceivers for XC2VP7-FG456.
06/20/05	4.3	<i>No changes in Module 1 for this revision.</i>
09/15/05	4.4	- Changed all instances of 10.3125 Gb/s (RocketIO transceiver maximum bit rate) to 6.25 Gb/s. - Changed all instances of 412.5 Gb/s (RocketIO X transceiver maximum multi-channel raw data transfer rate) to 250 Gb/s.
10/10/05	4.5	- Changed XC2VPX70 variable baud rate specification to fixed-rate operation at 4.25 Gb/s. - Changed maximum performance for -7 Virtex-II Pro X MGT (Table 4) to N/A.
03/05/07	4.6	<i>No changes in Module 1 for this revision.</i>
11/05/07	4.7	Updated copyright notice and legal disclaimer.
06/21/11	5.0	Added <i>Product Not Recommended for New Designs</i> banner.

Disparity Control

The 8B/10B encoder is initialized with a negative running disparity. Unique control allows forcing the current running disparity state.

TXRUNDISP signals its current running disparity. This may be useful in those cases where there is a need to manipulate the initial running disparity value.

Bits TXCHARDISPMODE and TXCHARDISPVAL control the generation of running disparity before each byte.

For example, the transceiver can generate the sequence

```
K28.5+ K28.5+ K28.5- K28.5-
or
K28.5- K28.5- K28.5+ K28.5+
```

by specifying inverted running disparity for the second and fourth bytes.

Transmit FIFO

Proper operation of the circuit is only possible if the FPGA clock (TXUSRCLK) is frequency-locked to the reference clock (REFCLK). Phase variations up to one clock cycle are allowable. The FIFO has a depth of four. Overflow or underflow conditions are detected and signaled at the interface. Bypassing of this FIFO is programmable.

8B/10B Encoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

A bypassable 8B/10B encoder is included. The encoder uses the same 256 data characters and 12 control characters used by Gigabit Ethernet, Fibre Channel, and InfiniBand.

The encoder accepts 8 bits of data along with a K-character signal for a total of 9 bits per character applied, and generates a 10 bit character for transmission. If the K-character signal is High, the data is encoded into one of the twelve possible K-characters available in the 8B/10B code. If the K-character input is Low, the 8 bits are encoded as standard data. If the K-character input is High, and a user applies other than one of the twelve possible combinations, TXKERR indicates the error.

8B/10B Decoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

An optional 8B/10B decoder is included. A programmable option allows the decoder to be bypassed. When the 8B/10B decoder is bypassed, the 10-bit character order is, for example,

```
RXCHARISK[0]          (first bit received)
RXRUNDISP[0]
RXDATA[7:0]           (last bit received is RXDATA[0])
```

The decoder uses the same table that is used for Gigabit Ethernet, Fibre Channel, and InfiniBand. In addition to

decoding all data and K-characters, the decoder has several extra features. The decoder separately detects both "disparity errors" and "out-of-band" errors. A disparity error is the reception of 10-bit character that exists within the 8B/10B table but has an incorrect disparity. An out-of-band error is the reception of a 10-bit character that does not exist within the 8B/10B table. It is possible to obtain an out-of-band error without having a disparity error. The proper disparity is always computed for both legal and illegal characters. The current running disparity is available at the RXRUNDISP signal.

The 8B/10B decoder performs a unique operation if out-of-band data is detected. If out-of-band data is detected, the decoder signals the error and passes the illegal 10-bits through and places them on the outputs. This can be used for debugging purposes if desired.

The decoder also signals the reception of one of the 12 valid K-characters. In addition, a programmable comma detect is included. The comma detect signal registers a comma on the receipt of any comma+, comma-, or both. Since the comma is defined as a 7-bit character, this includes several out-of-band characters. Another option allows the decoder to detect only the three defined commas (K28.1, K28.5, and K28.7) as comma+, comma-, or both. In total, there are six possible options, three for valid commas and three for "any comma."

Note that all bytes (1, 2, 4, or 8) at the RX FPGA interface each have their own individual 8B/10B indicators (K-character, disparity error, out-of-band error, current running disparity, and comma detect).

Receiver Buffer

The receiver includes buffers (FIFOs) in the datapath. This section gives the reasons for including the buffers and outlines their operation.

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

The receiver uses an *elastic buffer*, where "elastic" refers to the ability to modify the read pointer for clock correction and channel bonding.

Comma Detection

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indi-

Table 12: Summary of Voltage Supply Requirements for All Input and Output Standards

I/O Standard	V _{CCO}		V _{REF}	Termination Type	
	Output	Input	Input	Output	Input
LVTTTL ⁽¹⁾	3.3	3.3	N/R	N/R	N/R
LVC MOS33 ⁽¹⁾			N/R	N/R	N/R
LVDCI_33 ⁽¹⁾			N/R	Series	N/R
PCIX ⁽²⁾			N/R	N/R	N/R
PCI33_3 ⁽²⁾			N/R	N/R	N/R
PCI66_3 ⁽²⁾			N/R	N/R	N/R
LVDS_25	2.5	Note (3)	N/R	N/R	N/R
LVDSEXT_25			N/R	N/R	N/R
LDT_25			N/R	N/R	N/R
ULVDS_25			N/R	N/R	N/R
BLVDS_25			N/R	N/R	N/R
LVPECL_25			N/R	N/R	N/R
SSTL2_I			1.25	N/R	N/R
SSTL2_II			1.25	N/R	N/R
LVC MOS25		2.5	N/R	N/R	N/R
LVDCI_25			N/R	Series	N/R
LVDCI_DV2_25			N/R	Series	N/R
LVDS_25_DCI			N/R	N/R	Split
LVDSEXT_25_DCI			N/R	N/R	Split
SSTL2_I_DCI			1.25	N/R	Split
SSTL2_II_DCI			1.25	Split	Split
LVDS_25_DT			N/R	N/R	N/R
LVDSEXT_25_DT			N/R	N/R	N/R
LDT_25_DT			N/R	N/R	N/R
ULVDS_25_DT			N/R	N/R	N/R

Table 12: Summary of Voltage Supply Requirements for All Input and Output Standards (Continued)

I/O Standard	V _{CCO}		V _{REF}	Termination Type	
	Output	Input	Input	Output	Input
HSTL_III_18	1.8	Note (3)	1.1	N/R	N/R
HSTL_IV_18			1.1	N/R	N/R
HSTL_I_18			0.9	N/R	N/R
HSTL_II_18			0.9	N/R	N/R
SSTL18_I			0.9	N/R	N/R
SSTL18_II			0.9	N/R	N/R
LVC MOS18		1.8	N/R	N/R	N/R
LVDCI_18			N/R	Series	N/R
LVDCI_DV2_18			N/R	Series	N/R
HSTL_III_DCI_18			1.1	N/R	Single
HSTL_IV_DCI_18			1.1	Single	Single
HSTL_I_DCI_18			0.9	N/R	Split
HSTL_II_DCI_18			0.9	Split	Split
SSTL18_I_DCI			0.9	N/R	Split
SSTL18_II_DCI			0.9	Split	Split
HSTL_III	1.5	Note (3)	0.9	N/R	N/R
HSTL_IV			0.9	N/R	N/R
HSTL_I			0.75	N/R	N/R
HSTL_II			0.75	N/R	N/R
LVC MOS15		1.5	N/R	N/R	N/R
LVDCI_15			N/R	Series	N/R
LVDCI_DV2_15			N/R	Series	N/R
GTL_P_DCI			1	Single	Single
HSTL_III_DCI			0.9	N/R	Single
HSTL_IV_DCI			0.9	Single	Single
HSTL_I_DCI			0.75	N/R	Split
HSTL_II_DCI			0.75	Split	Split
GTL_DCI	1.2	1.2	0.8	Single	Single
GTL_P	N/R	Note (3)	1	N/R	N/R
GTL			0.8	N/R	N/R

Notes:

1. See application note [XAPP659](#) for more detailed information.
2. See application note [XAPP653](#) for more detailed information.
3. Pin voltage must not exceed V_{CCO}.
4. N/R = no requirement.

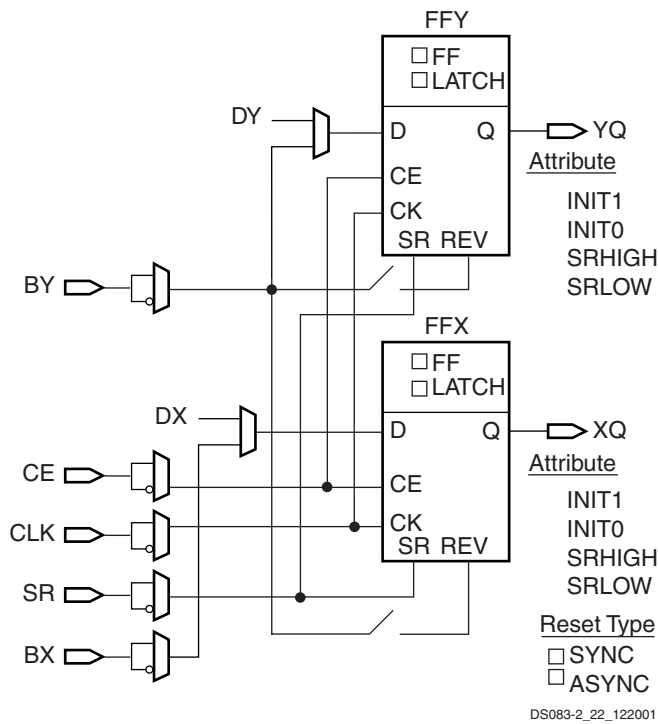


Figure 35: Register / Latch Configuration in a Slice

The set and reset functionality of a register or a latch can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

Distributed SelectRAM+ Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM+ element. SelectRAM+ elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8-bit RAM
- Single-Port 32 x 4-bit RAM
- Single-Port 64 x 2-bit RAM

- Single-Port 128 x 1-bit RAM
- Dual-Port 16 x 4-bit RAM
- Dual-Port 32 x 2-bit RAM
- Dual-Port 64 x 1-bit RAM

Distributed SelectRAM+ memory modules are synchronous (write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM+ memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.

Table 16 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM+ configuration.

Table 16: Distributed SelectRAM+ Configurations

RAM	Number of LUTs
16 x 1S	1
16 x 1D	2
32 x 1S	2
32 x 1D	4
64 x 1S	4
64 x 1D	8
128 x 1S	8

Notes:

1. S = single-port configuration; D = dual-port configuration

For single-port configurations, distributed SelectRAM+ memory has one address port for synchronous writes and asynchronous reads.

For dual-port configurations, distributed SelectRAM+ memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).

In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port

Table 65: Package Skew

Description	Symbol	Device/Package	Value	Units
Package Skew ⁽¹⁾	$T_{PKGSKEW}$	XC2VP2FF672	104	ps
		XC2VP4FF672	102	ps
		XC2VP7FF672	92	ps
		XC2VP7FF896	101	ps
		XC2VP20FF896	93	ps
		XC2VPX20FF896	93	ps
		XC2VP20FF1152	106	ps
		XC2VP30FF896	86	ps
		XC2VP30FF1152	112	ps
		XC2VP40FF1152	92	ps
		XC2VP40FF1148	100	ps
		XC2VP50FF1152	88	ps
		XC2VP50FF1148	101	ps
		XC2VP50FF1517	97	ps
		XC2VP70FF1517	95	ps
		XC2VP70FF1704	101	ps
		XC2VPX70FF1704	101	ps
		XC2VP100FF1704	86	ps
		XC2VP100FF1696	100	ps

Notes:

- These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball (7.1ps per mm).
- Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 66: Sample Window

Description	Symbol	Device	Speed Grade			Units
			-7	-6	-5	
Sampling Error at Receiver Pins ⁽¹⁾	T_{SAMP}	All	0.50	0.50	0.50	ns

Notes:

- This parameter indicates the total sampling error of Virtex-II Pro DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation.
- These measurements include:
 - CLK0 and CLK180 DCM jitter
 - Worst-case duty-cycle distortion, T_{DCD_CLK180}
 - DCM accuracy (phase offset)
 - DCM phase shift resolution
These measurements do not include package or clock tree skew.

FG256/FGG256 Fine-Pitch BGA Package

As shown in [Table 5](#), XC2VP2 and XC2VP4 Virtex-II Pro devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in each of these devices are identical. Following this table are the [FG256/FGG256 Fine-Pitch BGA Package Specifications \(1.00mm pitch\)](#).

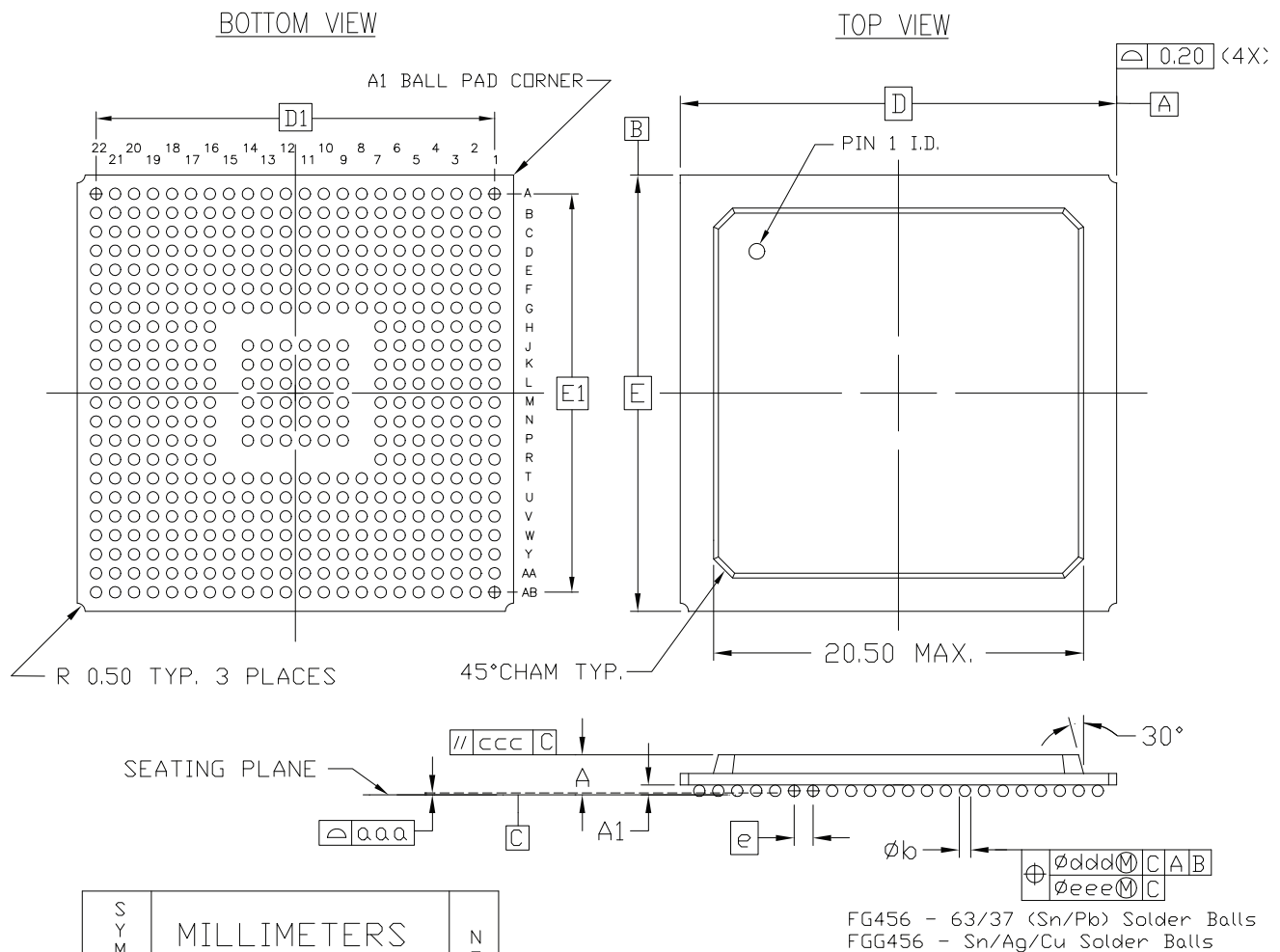
Table 5: FG256/FGG256 — XC2VP2 and XC2VP4

Bank	Pin Description	Pin Number
0	IO_L01N_0/VRP_0	C2
0	IO_L01P_0/VRN_0	C3
0	IO_L02N_0	B3
0	IO_L02P_0	C4
0	IO_L03N_0	A2
0	IO_L03P_0/VREF_0	A3
0	IO_L06N_0	D5
0	IO_L06P_0	C5
0	IO_L07P_0	D6
0	IO_L09N_0	E6
0	IO_L09P_0/VREF_0	E7
0	IO_L69N_0	D7
0	IO_L69P_0/VREF_0	C7
0	IO_L74N_0/GCLK7P	D8
0	IO_L74P_0/GCLK6S	C8
0	IO_L75N_0/GCLK5P	B8
0	IO_L75P_0/GCLK4S	A8
1	IO_L75N_1/GCLK3P	A9
1	IO_L75P_1/GCLK2S	B9
1	IO_L74N_1/GCLK1P	C9
1	IO_L74P_1/GCLK0S	D9
1	IO_L69N_1/VREF_1	C10
1	IO_L69P_1	D10
1	IO_L09N_1/VREF_1	E10
1	IO_L09P_1	E11
1	IO_L07N_1	D11
1	IO_L06N_1	C12
1	IO_L06P_1	D12
1	IO_L03N_1/VREF_1	A14
1	IO_L03P_1	A15

Table 6: FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
1	IO_L07P_1	F14			
1	IO_L06N_1	C15			
1	IO_L06P_1	D15			
1	IO_L05_1/No_Pair	E15			
1	IO_L03N_1/VREF_1	C16			
1	IO_L03P_1	D16			
1	IO_L02N_1	E16			
1	IO_L02P_1	E17			
1	IO_L01N_1/VRP_1	D17			
1	IO_L01P_1/VRN_1	D18			
2	IO_L01N_2/VRP_2	C21			
2	IO_L01P_2/VRN_2	C22			
2	IO_L02N_2	D21			
2	IO_L02P_2	D22			
2	IO_L03N_2	E19			
2	IO_L03P_2	E20			
2	IO_L04N_2/VREF_2	E21			
2	IO_L04P_2	E22			
2	IO_L06N_2	F19			
2	IO_L06P_2	F20			
2	IO_L43N_2	F21	NC		
2	IO_L43P_2	F22	NC		
2	IO_L46N_2/VREF_2	F18	NC		
2	IO_L46P_2	G18	NC		
2	IO_L48N_2	G19	NC		
2	IO_L48P_2	G20	NC		
2	IO_L49N_2	G21	NC		
2	IO_L49P_2	G22	NC		
2	IO_L50N_2	H19	NC		
2	IO_L50P_2	H20	NC		
2	IO_L52N_2/VREF_2	H21	NC		
2	IO_L52P_2	H22	NC		
2	IO_L54N_2	H18	NC		
2	IO_L54P_2	J17	NC		
2	IO_L55N_2	J19	NC		
2	IO_L55P_2	J20	NC		

FG456/FGG456 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	xx	xx	2.60	3
A ₁	0.35	0.50	0.60	
D/E	23.00 BSC			
D ₁ /E ₁	21.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa	xx	xx	0.20	2
ccc	xx	xx	0.35	
ddd	xx	xx	0.30	
eee	xx	xx	0.10	
M	22			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. NOMINAL 'A' DIMENSION IS TYPICALLY 2.20mm.
4. CONFORMS TO JEDEC MS-034-AAJ-1 (DEPOPULATED)

Figure 2: FG456/FGG456 Fine-Pitch BGA Package Specifications

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
4	VCCO_4		AA11			
4	VCCO_4		AA10			
5	VCCO_5		AB21			
5	VCCO_5		AB20			
5	VCCO_5		AB19			
5	VCCO_5		AB18			
5	VCCO_5		AA21			
5	VCCO_5		AA20			
5	VCCO_5		AA19			
5	VCCO_5		AA18			
5	VCCO_5		AA17			
5	VCCO_5		AA16			
6	VCCO_6		AB22			
6	VCCO_6		AA22			
6	VCCO_6		Y22			
6	VCCO_6		Y21			
6	VCCO_6		W22			
6	VCCO_6		W21			
6	VCCO_6		V22			
6	VCCO_6		V21			
6	VCCO_6		U21			
6	VCCO_6		T21			
7	VCCO_7		R21			
7	VCCO_7		P21			
7	VCCO_7		N22			
7	VCCO_7		N21			
7	VCCO_7		M22			
7	VCCO_7		M21			
7	VCCO_7		L22			
7	VCCO_7		L21			
7	VCCO_7		K22			
7	VCCO_7		J22			
N/A	CCLK		AC7			
N/A	PROG_B		G24			
N/A	DONE		AC8			

Table 9: FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
N/A	M0		AD24			
N/A	M1		AC24			
N/A	M2		AC23			
N/A	TCK		G7			
N/A	TDI		F26			
N/A	TDO		F5			
N/A	TMS		H8			
N/A	PWRDWN_B		AD7			
N/A	HSWAP_EN		H23			
N/A	RSVD		D6			
N/A	VBATT		H7			
N/A	DXP		H24			
N/A	DXN		D25			
N/A	AVCCAUXTX4		B26			
N/A	VTTXPAD4		B27			
N/A	TXNPAD4		A27			
N/A	TXPPAD4		A26			
N/A	GND4		C25			
N/A	RXPPAD4		A25			
N/A	RXNPAD4		A24			
N/A	VTRXPAD4		B25			
N/A	AVCCAUXRX4		B24			
N/A	AVCCAUXTX6		B19			
N/A	VTTXPAD6		B20			
N/A	TXNPAD6		A20			
N/A	TXPPAD6		A19			
N/A	GND6		C19			
N/A	RXPPAD6		A18			
N/A	RXNPAD6		A17			
N/A	VTRXPAD6		B18			
N/A	AVCCAUXRX6		B17			
N/A	AVCCAUXTX7		B13			
N/A	VTTXPAD7		B14			
N/A	TXNPAD7		A14			
N/A	TXPPAD7		A13			
N/A	GND7		C12			

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
2	IO_L05N_2	J8				
2	IO_L05P_2	J7				
2	IO_L06N_2	F5				
2	IO_L06P_2	F4				
2	IO_L15N_2	G4	NC			
2	IO_L15P_2	G3	NC			
2	IO_L16N_2/VREF_2	G6	NC			
2	IO_L16P_2	G5	NC			
2	IO_L17N_2	F2	NC			
2	IO_L17P_2	F1	NC			
2	IO_L18N_2	L10	NC			
2	IO_L18P_2	L9	NC			
2	IO_L19N_2	H6	NC			
2	IO_L19P_2	H5	NC			
2	IO_L20N_2	G2	NC			
2	IO_L20P_2	G1	NC			
2	IO_L21N_2	J6	NC			
2	IO_L21P_2	J5	NC			
2	IO_L22N_2/VREF_2	J4	NC			
2	IO_L22P_2	J3	NC			
2	IO_L23N_2	K8	NC			
2	IO_L23P_2	K7	NC			
2	IO_L24N_2	H4	NC			
2	IO_L24P_2	H3	NC			
2	IO_L31N_2	H2				
2	IO_L31P_2	H1				
2	IO_L32N_2	M10				
2	IO_L32P_2	M9				
2	IO_L33N_2	K5				
2	IO_L33P_2	K4				
2	IO_L34N_2/VREF_2	J2				
2	IO_L34P_2	K2				
2	IO_L35N_2	L8				
2	IO_L35P_2	L7				
2	IO_L36N_2	L6				
2	IO_L36P_2	L5				
2	IO_L37N_2	K1				
2	IO_L37P_2	L1				

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
1	VCCO_1	L15				
1	VCCO_1	M13				
1	VCCO_1	M14				
1	VCCO_1	M15				
1	VCCO_1	M16				
1	VCCO_1	M17				
2	VCCO_2	F3				
2	VCCO_2	K6				
2	VCCO_2	M11				
2	VCCO_2	N11				
2	VCCO_2	N12				
2	VCCO_2	P11				
2	VCCO_2	P12				
2	VCCO_2	R5				
2	VCCO_2	R11				
2	VCCO_2	R12				
2	VCCO_2	T12				
2	VCCO_2	U12				
3	VCCO_3	V12				
3	VCCO_3	W12				
3	VCCO_3	Y5				
3	VCCO_3	Y11				
3	VCCO_3	Y12				
3	VCCO_3	AA11				
3	VCCO_3	AA12				
3	VCCO_3	AB11				
3	VCCO_3	AB12				
3	VCCO_3	AC11				
3	VCCO_3	AE6				
3	VCCO_3	AJ3				
4	VCCO_4	AC13				
4	VCCO_4	AC14				
4	VCCO_4	AC15				
4	VCCO_4	AC16				
4	VCCO_4	AC17				
4	VCCO_4	AD12				
4	VCCO_4	AD13				
4	VCCO_4	AD14				

Table 10: FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
N/A	TXPPAD9	A8				
N/A	GND A9	C8				
N/A	RXPPAD9	A7				
N/A	RXNPAD9	A6				
N/A	VTRXPAD9	B7				
N/A	AVCCAUXRX9	B6				
N/A	AVCCAUXTX11	B4	NC	NC		
N/A	VTTXPAD11	B5	NC	NC		
N/A	TXNPAD11	A5	NC	NC		
N/A	TXPPAD11	A4	NC	NC		
N/A	GND A11	C5	NC	NC		
N/A	RXPPAD11	A3	NC	NC		
N/A	RXNPAD11	A2	NC	NC		
N/A	VTRXPAD11	B3	NC	NC		
N/A	AVCCAUXRX11	B2	NC	NC		
N/A	AVCCAUXRX14	AN2	NC	NC		
N/A	VTRXPAD14	AN3	NC	NC		
N/A	RXNPAD14	AP2	NC	NC		
N/A	RXPPAD14	AP3	NC	NC		
N/A	GND A14	AM5	NC	NC		
N/A	TXPPAD14	AP4	NC	NC		
N/A	TXNPAD14	AP5	NC	NC		
N/A	VTTXPAD14	AN5	NC	NC		
N/A	AVCCAUXTX14	AN4	NC	NC		
N/A	AVCCAUXRX16	AN6				
N/A	VTRXPAD16	AN7				
N/A	RXNPAD16	AP6				
N/A	RXPPAD16	AP7				
N/A	GND A16	AM8				
N/A	TXPPAD16	AP8				
N/A	TXNPAD16	AP9				
N/A	VTTXPAD16	AN9				
N/A	AVCCAUXTX16	AN8				
N/A	AVCCAUXRX17	AN10	NC	NC	NC	
N/A	VTRXPAD17	AN11	NC	NC	NC	
N/A	RXNPAD17	AP10	NC	NC	NC	
N/A	RXPPAD17	AP11	NC	NC	NC	
N/A	GND A17	AM12	NC	NC	NC	

Table 11: FF1148 — XC2VP40 and XC2VP50

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
7	IO_L51P_7	N31		
7	IO_L51N_7	P31		
7	IO_L50P_7	T27		
7	IO_L50N_7	R28		
7	IO_L49P_7	M33		
7	IO_L49N_7	M34		
7	IO_L48P_7	M31		
7	IO_L48N_7	M32		
7	IO_L47P_7	R24		
7	IO_L47N_7	R25		
7	IO_L46P_7	M29		
7	IO_L46N_7/VREF_7	M30		
7	IO_L45P_7	L33		
7	IO_L45N_7	L34		
7	IO_L44P_7	P27		
7	IO_L44N_7	P28		
7	IO_L43P_7	L29		
7	IO_L43N_7	L30		
7	IO_L42P_7	K33		
7	IO_L42N_7	K34		
7	IO_L41P_7	P26		
7	IO_L41N_7	R26		
7	IO_L40P_7	K32		
7	IO_L40N_7/VREF_7	L32		
7	IO_L39P_7	K29		
7	IO_L39N_7	K30		
7	IO_L38P_7	P24		
7	IO_L38N_7	P25		
7	IO_L37P_7	J32		
7	IO_L37N_7	J33		
7	IO_L36P_7	J31		
7	IO_L36N_7	K31		
7	IO_L35P_7	N28		
7	IO_L35N_7	N29		
7	IO_L34P_7	H32		
7	IO_L34N_7/VREF_7	H33		
7	IO_L33P_7	H29		
7	IO_L33N_7	H30		

Table 12: FF1517 — XC2VP50 and XC2VP70

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
4	IO_L38P_4	AH16		
4	IO_L39N_4	AR14		
4	IO_L39P_4	AP14		
4	IO_L43N_4	AU14		
4	IO_L43P_4	AT14		
4	IO_L44N_4	AH17		
4	IO_L44P_4	AG17		
4	IO_L45N_4	AN15		
4	IO_L45P_4/VREF_4	AM15		
4	IO_L46N_4	AR15		
4	IO_L46P_4	AP15		
4	IO_L47N_4	AK16		
4	IO_L47P_4	AJ17		
4	IO_L48N_4	AU15		
4	IO_L48P_4	AT15		
4	IO_L49N_4	AM16		
4	IO_L49P_4	AL16		
4	IO_L50_4/No_Pair	AM17		
4	IO_L53_4/No_Pair	AL17		
4	IO_L54N_4	AP16		
4	IO_L54P_4	AN17		
4	IO_L55N_4	AR16		
4	IO_L55P_4	AR17		
4	IO_L56N_4	AH18		
4	IO_L56P_4	AG18		
4	IO_L57N_4	AU17		
4	IO_L57P_4/VREF_4	AT17		
4	IO_L58N_4	AM18		
4	IO_L58P_4	AL18		
4	IO_L59N_4	AK18		
4	IO_L59P_4	AJ18		
4	IO_L60N_4	AP18		
4	IO_L60P_4	AN18		
4	IO_L64N_4	AT18		
4	IO_L64P_4	AR18		
4	IO_L65N_4	AH19		
4	IO_L65P_4	AG19		
4	IO_L66N_4	AU18		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
4	IO_L87P_4/VREF_4		AP15	NC	
4	IO_L37N_4		AV15		
4	IO_L37P_4		AU15		
4	IO_L38N_4		AY14		
4	IO_L38P_4		AY15		
4	IO_L39N_4		AM16		
4	IO_L39P_4		AL16		
4	IO_L43N_4		AP16		
4	IO_L43P_4		AN16		
4	IO_L44N_4		AR16		
4	IO_L44P_4		AT16		
4	IO_L45N_4		AV16		
4	IO_L45P_4/VREF_4		AU16		
4	IO_L46N_4		AL18		
4	IO_L46P_4		AL17		
4	IO_L47N_4		AM17		
4	IO_L47P_4		AN17		
4	IO_L48N_4		AR17		
4	IO_L48P_4		AP17		
4	IO_L49N_4		AU17		
4	IO_L49P_4		AT17		
4	IO_L50_4/No_Pair		AW16		
4	IO_L53_4/No_Pair		AW17		
4	IO_L54N_4		AN18		
4	IO_L54P_4		AM18		
4	IO_L55N_4		AT18		
4	IO_L55P_4		AR18		
4	IO_L56N_4		AV17		
4	IO_L56P_4		AV18		
4	IO_L57N_4		AY18		
4	IO_L57P_4/VREF_4		AY17		
4	IO_L58N_4		AM19		
4	IO_L58P_4		AL19		
4	IO_L59N_4		AP19		
4	IO_L59P_4		AN19		
4	IO_L60N_4		AT19		

Table 13: FF1704 — XC2VP70, XC2VPX70, and XC2VP100

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
6	IO_L34N_6		AH38		
6	IO_L35P_6		AH31		
6	IO_L35N_6		AH32		
6	IO_L36P_6		AJ40		
6	IO_L36N_6		AH40		
6	IO_L37P_6		AH41		
6	IO_L37N_6		AH42		
6	IO_L38P_6		AH35		
6	IO_L38N_6		AG35		
6	IO_L39P_6		AG36		
6	IO_L39N_6/VREF_6		AG37		
6	IO_L40P_6		AG38		
6	IO_L40N_6		AG39		
6	IO_L41P_6		AG32		
6	IO_L41N_6		AG33		
6	IO_L42P_6		AG40		
6	IO_L42N_6		AG41		
6	IO_L43P_6		AF33		
6	IO_L43N_6		AF34		
6	IO_L44P_6		AF35		
6	IO_L44N_6		AF36		
6	IO_L45P_6		AF37		
6	IO_L45N_6/VREF_6		AF38		
6	IO_L46P_6		AF39		
6	IO_L46N_6		AF40		
6	IO_L47P_6		AF31		
6	IO_L47N_6		AG31		
6	IO_L48P_6		AF41		
6	IO_L48N_6		AF42		
6	IO_L49P_6		AE35		
6	IO_L49N_6		AE36		
6	IO_L50P_6		AE31		
6	IO_L50N_6		AF32		
6	IO_L51P_6		AE38		
6	IO_L51N_6/VREF_6		AE39		
6	IO_L52P_6		AE41		

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
6	IO_L33N_6/VREF_6	AK40	
6	IO_L34P_6	AK36	
6	IO_L34N_6	AK37	
6	IO_L35P_6	AE36	
6	IO_L35N_6	AE37	
6	IO_L36P_6	AJ41	
6	IO_L36N_6	AJ42	
6	IO_L37P_6	AJ40	
6	IO_L37N_6	AH40	
6	IO_L38P_6	AE34	
6	IO_L38N_6	AE35	
6	IO_L39P_6	AJ38	
6	IO_L39N_6/VREF_6	AH37	
6	IO_L40P_6	AJ36	
6	IO_L40N_6	AJ37	
6	IO_L41P_6	AE32	
6	IO_L41N_6	AE33	
6	IO_L42P_6	AH41	
6	IO_L42N_6	AH42	
6	IO_L43P_6	AH38	
6	IO_L43N_6	AH39	
6	IO_L44P_6	AD36	
6	IO_L44N_6	AC35	
6	IO_L45P_6	AH36	
6	IO_L45N_6/VREF_6	AG36	
6	IO_L46P_6	AG41	
6	IO_L46N_6	AG42	
6	IO_L47P_6	AD34	
6	IO_L47N_6	AC33	
6	IO_L48P_6	AG40	
6	IO_L48N_6	AF39	
6	IO_L49P_6	AG38	
6	IO_L49N_6	AG39	
6	IO_L50P_6	AD32	
6	IO_L50N_6	AD33	
6	IO_L51P_6	AG37	
6	IO_L51N_6/VREF_6	AF37	

Table 14: FF1696 — XC2VP100

Bank	Pin Description	Pin Number	No Connects
			XC2VP100
7	IO_L26P_7	V31	
7	IO_L26N_7	U31	
7	IO_L25P_7	L41	
7	IO_L25N_7	L42	
7	IO_L24P_7	K40	
7	IO_L24N_7	L40	
7	IO_L23P_7	T34	
7	IO_L23N_7	T35	
7	IO_L22P_7	L38	
7	IO_L22N_7/VREF_7	L39	
7	IO_L21P_7	K36	
7	IO_L21N_7	L36	
7	IO_L20P_7	T32	
7	IO_L20N_7	T33	
7	IO_L19P_7	K41	
7	IO_L19N_7	K42	
7	IO_L18P_7	K37	
7	IO_L18N_7	K38	
7	IO_L17P_7	R34	
7	IO_L17N_7	R35	
7	IO_L16P_7	H42	
7	IO_L16N_7/VREF_7	J41	
7	IO_L15P_7	J39	
7	IO_L15N_7	J40	
7	IO_L14P_7	R32	
7	IO_L14N_7	R33	
7	IO_L13P_7	J36	
7	IO_L13N_7	J37	
7	IO_L12P_7	H40	
7	IO_L12N_7	H41	
7	IO_L11P_7	T31	
7	IO_L11N_7	R31	
7	IO_L10P_7	H38	
7	IO_L10N_7/VREF_7	H39	
7	IO_L09P_7	H36	
7	IO_L09N_7	H37	
7	IO_L08P_7	P34	