# AMD Xilinx - XC2VP30-7FF896C Datasheet



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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 3424 |
| Number of Logic Elements/Cells | 30816 |
| Total RAM Bits | 2506752 |
| Number of I/O | 556 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 896-BBGA, FCBGA |
| Supplier Device Package | 896-FCBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2vp30-7ff896c |

RXP and RXN as shown in Figure 5. This supports multiple termination styles, including high-side, low-side, and differential (floating or active). This configuration supports receiver termination compatible to Virtex-II Pro devices, using a CML (high-side) termination to an active supply of 1.8V – 2.5V. For DC coupling of two Virtex-II Pro X devices, a 1.5V CML termination for VTRX is recommended.

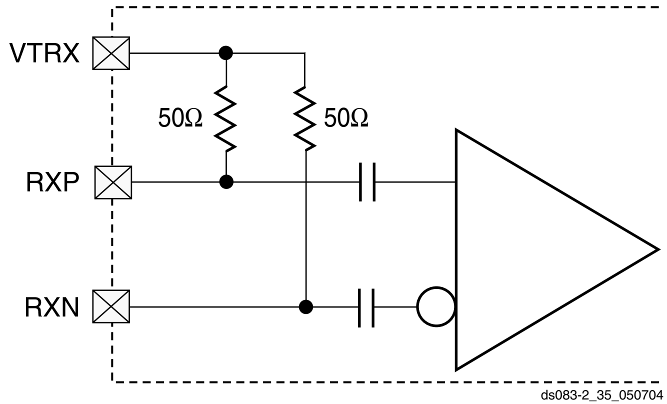


*Figure 5:* **RocketIO X Receive Termination**

## PCS

### *Fabric Data Interface*

Internally, the PCS operates in either 2-byte mode (16/20 bits) or 4-byte mode (32/40 bits). When in 2-byte mode, the FPGA fabric interface can either be 1, 2, or 4 bytes wide. When in 4-byte mode, the FPGA fabric interface can either be 4 or 8 bytes wide. When accompanied by the predefined modes of the PMA, the user thus has a large combination of protocols and data rates from which to choose.

USRCLK2 clocks data on the fabric side, while USRCLK clocks data on the PCS side. This creates distinct USRCLK/USRCLK2 frequency ratios for different combinations of fabric and internal data widths. Table 2 summarizes the USRCLK2-to-USRCLK ratios for the different possible combinations of data widths.

*Table 2:* **Clock Ratios for Various Data Widths**

| Fabric Data Width | Frequency Ratio of USRCLK:USRCLK2 | |
|---|---|---|
| | 2-Byte Internal Data Width | 4-Byte Internal Data Width |
| 1 byte | 1:2 (1) | N/A |
| 2 byte | 1:1 | N/A |
| 4 byte | 2:1 (1) | 1:1 |
| 8 byte | N/A | 2:1 (1) |

**Notes:**
1. Each edge of slower clock must align with falling edge of faster clock.

As a general guide, use 2-byte internal data width mode when the serial speed is below 5 Gb/s, and 4-byte internal data width mode when the serial speed is greater than 5 Gb/s. In 2-byte mode, the PCS processes 4-byte data every other byte.

No fixed phase relationship is assumed between REFCLK, RXRECCLK, and/or any other clock that is not tied to either of these clocks. When RXUSRCLK and RXUSRCLK2 have different frequencies, each edge of the slower clock is aligned to a falling edge of the faster clock. The same relationships apply to TXUSRCLK and TXUSRCLK2.

### *FPGA Transmit Interface*

The FPGA can send either one, two, or four characters of data to the transmitter. Each character can be either 8 bits or 10 bits wide. If 8-bit data is applied, the additional inputs become control signals for the 8B/10B encoder. When the 8B/10B encoder is bypassed, the 10-bit character order is generated as follows:

TXCHARDISPMODE[0] (first bit transmitted)
TXCHARDISPVAL[0]
TXDATA[7:0] (last bit transmitted is TXDATA[0])

### *64B/66B Encoder/Decoder*

The RocketIO X PCS features a 64B/66B encoder/decoder, scrambler/descrambler, and gearbox functions that can be bypassed as needed. The encoder is compliant with IEEE 802.3ae specifications.

### *Scrambler/Gearbox*

The bypassable scrambler operates on the read side of the transmit FIFO. The scrambler uses the following generator polynomial to scramble 64B/66B payload data:

$$G(x) = 1 + x^{39} + x^{58}$$

The scrambler works in conjunction with the gearbox, which frames 64B/66B data for the PMA. The gearbox should always be enabled when using the 64B/66B protocal.

*Table 15:* **SelectIO-Ultra Differential Buffers With On-Chip Termination**

| I/O Standard Description | IOSTANDARD Attribute | |
|---|---|---|
| | **External Termination** | **On-Chip Termination** |
| LVDS 2.5V | LVDS_25 | LVDS_25_DCI |
| LVDS Extended 2.5V | LVDSEXT_25 | LVDSEXT_25_DCI |

Figure 28 provides examples illustrating the use of the HSTL_I_DCI, HSTL_II_DCI, HSTL_III_DCI, and HSTL_IV_DCI I/O standards. For a complete list, see the ***Virtex-II Pro Platform FPGA User Guide***.

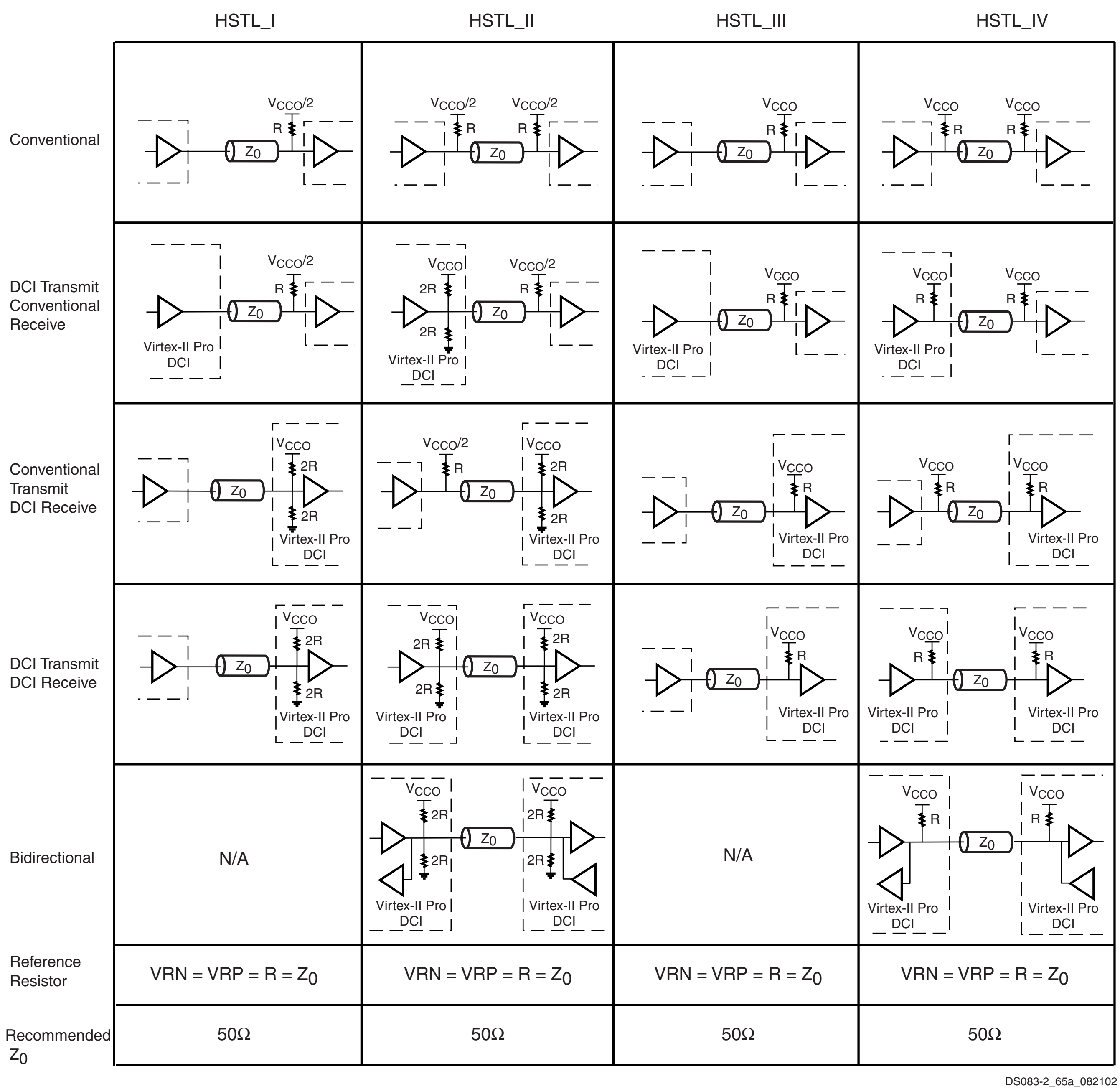


*Figure 28:* **HSTL DCI Usage Examples**

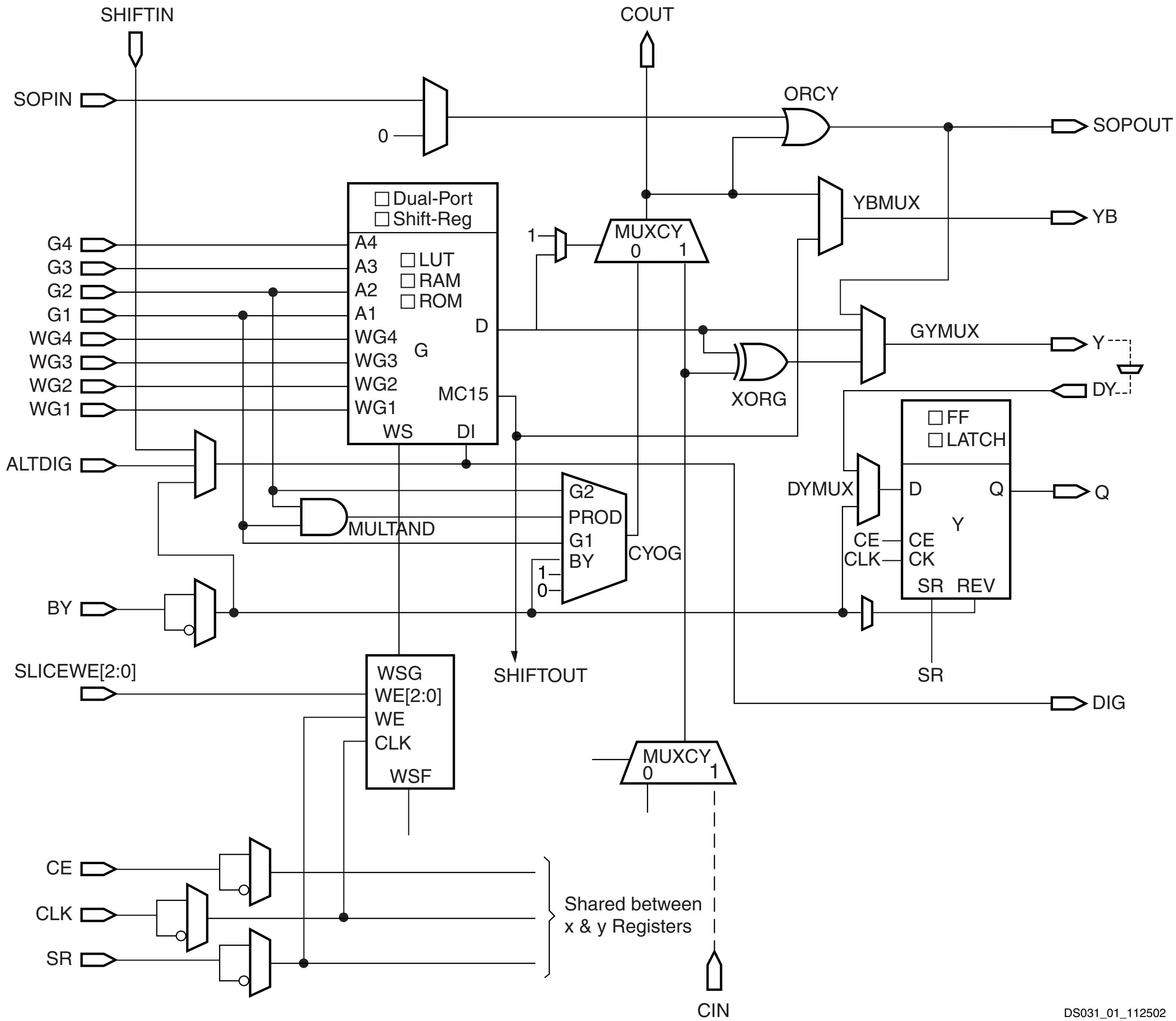


*Figure 34:* **Virtex-II Pro Slice (Top Half)**

## 18-Bit x 18-Bit Multipliers

### Introduction

A Virtex-II Pro multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II Pro devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18 Kb block SelectRAM+ resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

Each SelectRAM+ memory and multiplier block is tied to four switch matrices, as shown in Figure 53.

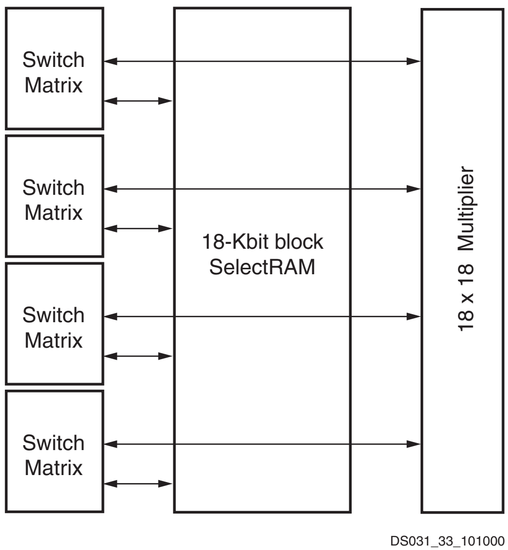


*Figure 53:* **SelectRAM+ and Multiplier Blocks**

### Association With Block SelectRAM+ Memory

The interconnect is designed to allow SelectRAM+ memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM+ and the multiplier. Thus, SelectRAM+ memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM+ memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM+ resource feeding the multiplier. The use of SelectRAM+ memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

### Configuration

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits. Figure 54 shows a multiplier block.

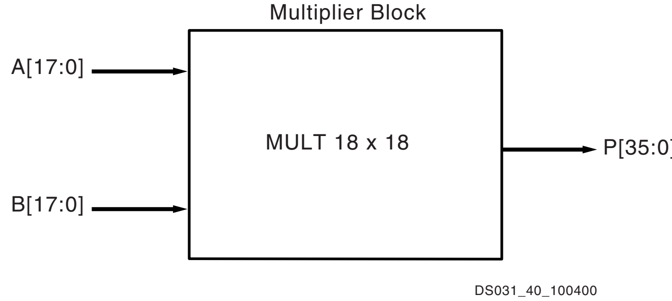


*Figure 54:* **Multiplier Block**

### Locations / Organization

Multiplier organization is identical to the 18 Kb SelectRAM+ organization, because each multiplier is associated with an 18 Kb block SelectRAM+ resource.

*Table 26:* **Multiplier Resources**

| Device | Columns | Total Multipliers |
|---|---|---|
| XC2VP2 | 4 | 12 |
| XC2VP4 | 4 | 28 |
| XC2VP7 | 6 | 44 |
| XC2VP20 | 8 | 88 |
| XC2VP30 | 8 | 136 |
| XC2VPX20 | 8 | 88 |
| XC2VP40 | 10 | 192 |
| XC2VP50 | 12 | 232 |
| XC2VP70 | 14 | 328 |
| XC2VPX70 | 14 | 308 |
| XC2VP100 | 16 | 444 |

In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic. (Refer to Configurable Logic Blocks (CLBs), page 35).

## Global Clock Multiplexer Buffers

Virtex-II Pro devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads center on both the top edge and the bottom edge of the device, as illustrated in Figure 55.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II Pro devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

## Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The $V_{CCINT}$ power supply must ramp on, monotonically, no faster than 200 µs and no slower than 50 ms. Ramp-on is defined as: 0 $V_{DC}$ to minimum supply voltages (see Table 2).

$V_{CCAUX}$ and $V_{CCO}$ can power on at any ramp rate. Power supplies can be turned on in any sequence.

Table 5 shows the minimum current required by Virtex-II Pro devices for proper power-on and configuration.

If the current minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

Once initialized and configured, use the power calculator to estimate current drain on these supplies.

For more information on $V_{CCAUX}$, $V_{CCO}$, and configuration mode, refer to Chapter 3 in the *Virtex-II Pro Platform FPGA User Guide*.

*Table 5:* **Power-On Current for Virtex-II Pro Devices**

| Symbol | Device | | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | XC2VP2 | XC2VP4 | XC2VP7 | XC2VP20 | XC2VPX20 | XC2VP30 | XC2VP40 | XC2VP50 | XC2VP70 | XC2VPX70 | XC2VP100 | |
| $I_{CCINTMIN}$ | 500 | 500 | 500 | 600 | 600 | 800 | 1050 | 1250 | 1700 | 1700 | 2200 | mA |
| $I_{CCAUXMIN}$ | 250 | 250 | 250 | 250 | 250 | 250 | 250 | 250 | 250 | 250 | 250 | mA |
| $I_{CCOMIN}$ | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | mA |

**Notes:**
1. Power-on current parameter values are specified for Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.5.
2. $I_{CCOMIN}$ values listed here apply to the entire device (all banks).

## General Power Supply Requirements

Proper decoupling of all FPGA power supplies is essential. Consult Xilinx Application Note **XAPP623** for detailed information on power distribution system design.

$V_{CCAUX}$ powers critical resources in the FPGA. Therefore, this supply voltage is especially susceptible to power supply noise. $V_{CCAUX}$ can share a power plane with $V_{CCO}$, but only if $V_{CCO}$ does not have excessive noise. Staying within simultaneously switching output (SSO) limits is essential for keeping power supply noise to a minimum. Refer to **XAPP689**, "Managing Ground Bounce in Large FPGAs," to determine the number of simultaneously switching outputs allowed per bank at the package level.

Changes in $V_{CCAUX}$ voltage beyond 200 mV peak-to-peak should take place at a rate no faster than 10 mV per millisecond.

Recommended practices that can help reduce jitter and period distortion are described in Xilinx Answer Record 13756.

## Virtex-II Pro Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II Pro devices. The numbers reported here are fully characterized worst-case values. Note that these values are subject to the same guidelines as Virtex-II Pro Switching Characteristics (speed files).

Table 13 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

*Table 13:* **Pin-to-Pin Performance**

| Description | Device Used & Speed Grade | Pin-to-Pin Performance (with I/O Delays) | Units |
|---|---|---|---|
| **Basic Functions:** | | | |
| 16-bit Address Decoder | XC2VP20FF1152-6 | 7.20 | ns |
| 32-bit Address Decoder | XC2VP20FF1152-6 | 8.08 | ns |
| 64-bit Address Decoder | XC2VP20FF1152-6 | 8.15 | ns |
| 4:1 MUX | XC2VP20FF1152-6 | 3.85 | ns |
| 8:1 MUX | XC2VP20FF1152-6 | 7.24 | ns |
| 16:1 MUX | XC2VP20FF1152-6 | 7.30 | ns |
| 32:1 MUX | XC2VP20FF1152-6 | 7.64 | ns |
| Combinatorial (pad to LUT to pad) | XC2VP20FF1152-6 | 3.26 | ns |
| **Memory:** | | | |
| **Block RAM** | | | |
| Pad to setup | XC2VP20FF1152-6 | 1.72 | ns |
| Clock to Pad | XC2VP20FF1152-6 | 6.63 | ns |
| **Distributed RAM** | | | |
| Pad to setup | XC2VP20FF1152-6 | 1.78 | ns |
| Clock to Pad | XC2VP20FF1152-6 | 4.12 | ns |

*Table 34:* **RocketIO TXUSRCLK2 Switching Characteristics**

| Description | Symbol | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -7 | -6 | -5 | |
| **Setup and Hold Relative to Clock (TXUSRCLK2)** | | | | | |
| CONFIGENABLE control input | $T_{GCCK}$_CFGEN/$T_{GCKC}$_CFGEN | 0.35/ 0.10 | 0.35/ 0.10 | 0.39/ 0.11 | ns, min |
| TXBYPASS8B10B control inputs | $T_{GCCK}$_TBYP/$T_{GCKC}$_TBYP | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| TXFORCECRCERR control input | $T_{GCCK}$_TCRCE/$T_{GCKC}$_TCRCE | 0.39/ 0.12 | 0.44/ 0.14 | 0.49/ 0.15 | ns, min |
| TXPOLARITY control input | $T_{GCCK}$_TPOL/$T_{GCKC}$_TPOL | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| TXINHIBIT control inputs | $T_{GCCK}$_TINH/$T_{GCKC}$_TINH | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| LOOPBACK control inputs | $T_{GCCK}$_LBK/$T_{GCKC}$_LBK | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| TXRESET control input | $T_{GCCK}$_TRST/$T_{GCKC}$_TRST | 0.02/ 0.10 | 0.02/ 0.10 | 0.02/ 0.11 | ns, min |
| TXCHARISK control inputs | $T_{GCCK}$_TKCH/$T_{GCKC}$_TKCH | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| TXCHARDISPMODE control inputs | $T_{GCCK}$_TCDM/$T_{GCKC}$_TCDM | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| TXCHARDISPVAL control inputs | $T_{GCCK}$_TCDV/$T_{GCKC}$_TCDV | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| CONFIGIN data input | $T_{GDCK}$_CFGIN/$T_{GCKD}$_CFGIN | 0.35/ 0.10 | 0.35/ 0.10 | 0.39/ 0.11 | ns, min |
| TXDATA data inputs | $T_{GDCK}$_TDAT/$T_{GCKD}$_TDAT | 0.02/ 0.00 | 0.02/ 0.00 | 0.02/ 0.00 | ns, min |
| **Clock to Out** | | | | | |
| TXBUFERR status output | $T_{GCKST}$_TBERR | 0.54 | 0.54 | 0.60 | ns, max |
| TXKERR status outputs | $T_{GCKST}$_TKERR | 0.41 | 0.41 | 0.46 | ns, max |
| TXRUNDISP status outputs | $T_{GCKST}$_TRDIS | 0.41 | 0.41 | 0.46 | ns, max |
| CONFIGOUT data output | $T_{GCKDO}$_CFGOUT | 0.25 | 0.25 | 0.28 | ns, max |
| **Clock** | | | | | |
| TXUSRCLK2 minimum pulse width, High | $T_{GPWH}$_TX2 | 1.42 | 1.42 | 2.25 | ns, min |
| TXUSRCLK2 minimum pulse width, Low | $T_{GPWL}$_TX2 | 1.42 | 1.42 | 2.25 | ns, min |

*Table 5:* **FG256/FGG256 — XC2VP2 and XC2VP4**

| Bank | Pin Description | Pin Number |
|---|---|---|
| 7 | IO_L85N_7 | G2 |
| 7 | IO_L06P_7 | G3 |
| 7 | IO_L06N_7 | G4 |
| 7 | IO_L04P_7 | F1 |
| 7 | IO_L04N_7/VREF_7 | F2 |
| 7 | IO_L03P_7 | F3 |
| 7 | IO_L03N_7 | F4 |
| 7 | IO_L02P_7 | F5 |
| 7 | IO_L02N_7 | E4 |
| 7 | IO_L01P_7/VRN_7 | E2 |
| 7 | IO_L01N_7/VRP_7 | E3 |
| | | |
| 0 | VCCO_0 | F8 |
| 0 | VCCO_0 | F7 |
| 0 | VCCO_0 | E8 |
| 1 | VCCO_1 | F9 |
| 1 | VCCO_1 | F10 |
| 1 | VCCO_1 | E9 |
| 2 | VCCO_2 | H12 |
| 2 | VCCO_2 | H11 |
| 2 | VCCO_2 | G11 |
| 3 | VCCO_3 | K11 |
| 3 | VCCO_3 | J12 |
| 3 | VCCO_3 | J11 |
| 4 | VCCO_4 | M9 |
| 4 | VCCO_4 | L9 |
| 4 | VCCO_4 | L10 |
| 5 | VCCO_5 | M8 |
| 5 | VCCO_5 | L8 |
| 5 | VCCO_5 | L7 |
| 6 | VCCO_6 | K6 |
| 6 | VCCO_6 | J6 |
| 6 | VCCO_6 | J5 |
| 7 | VCCO_7 | H6 |
| 7 | VCCO_7 | H5 |

*Table 7:* **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 |
| N/A | AVCCAUXRX21 | AE7 | | | |
| N/A | VTRXPAD21 | AE6 | | | |
| N/A | RXNPAD21 | AF7 | | | |
| N/A | RXPPAD21 | AF6 | | | |
| N/A | GNDA21 | AD6 | | | |
| N/A | TXPPAD21 | AF5 | | | |
| N/A | TXNPAD21 | AF4 | | | |
| N/A | VTTXPAD21 | AE4 | | | |
| N/A | AVCCAUXTX21 | AE5 | | | |
| N/A | M2 | AD4 | | | |
| N/A | M0 | AF3 | | | |
| N/A | M1 | AE3 | | | |
| N/A | TDI | D3 | | | |
| | | | | | |
| N/A | VCCINT | G10 | | | |
| N/A | VCCINT | G13 | | | |
| N/A | VCCINT | G14 | | | |
| N/A | VCCINT | G17 | | | |
| N/A | VCCINT | J9 | | | |
| N/A | VCCINT | J18 | | | |
| N/A | VCCINT | K7 | | | |
| N/A | VCCINT | K10 | | | |
| N/A | VCCINT | K11 | | | |
| N/A | VCCINT | K16 | | | |
| N/A | VCCINT | K17 | | | |
| N/A | VCCINT | K20 | | | |
| N/A | VCCINT | L10 | | | |
| N/A | VCCINT | L17 | | | |
| N/A | VCCINT | N7 | | | |
| N/A | VCCINT | N20 | | | |
| N/A | VCCINT | P7 | | | |
| N/A | VCCINT | P20 | | | |
| N/A | VCCINT | T10 | | | |
| N/A | VCCINT | T17 | | | |
| N/A | VCCINT | U7 | | | |

*Table 9:* **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

| Bank | Pin Description | | Pin Number | No Connects | | |
|---|---|---|---|---|---|---|
| | Virtex-II Pro devices | XC2VPX20 (if Different) | | XC2VP7 | XC2VP20, XC2VPX20 | XC2VP30 |
| 0 | IO_L01N_0/VRP_0 | | E25 | | | |
| 0 | IO_L01P_0/VRN_0 | | E24 | | | |
| 0 | IO_L02N_0 | | F24 | | | |
| 0 | IO_L02P_0 | | F23 | | | |
| 0 | IO_L03N_0 | | E23 | | | |
| 0 | IO_L03P_0/VREF_0 | | E22 | | | |
| 0 | IO_L05_0/No_Pair | | G23 | | | |
| 0 | IO_L06N_0 | | H22 | | | |
| 0 | IO_L06P_0 | | G22 | | | |
| 0 | IO_L07N_0 | | F22 | | | |
| 0 | IO_L07P_0 | | F21 | | | |
| 0 | IO_L08N_0 | | D24 | | | |
| 0 | IO_L08P_0 | | C24 | | | |
| 0 | IO_L09N_0 | | H21 | | | |
| 0 | IO_L09P_0/VREF_0 | | G21 | | | |
| 0 | IO_L37N_0 | | E21 | | | |
| 0 | IO_L37P_0 | | D21 | | | |
| 0 | IO_L38N_0 | | D23 | | | |
| 0 | IO_L38P_0 | | C23 | | | |
| 0 | IO_L39N_0 | | H20 | | | |
| 0 | IO_L39P_0 | | G20 | | | |
| 0 | IO_L43N_0 | | E20 | | | |
| 0 | IO_L43P_0 | | D20 | | | |
| 0 | IO_L44N_0 | | B23 | | | |
| 0 | IO_L44P_0 | | A23 | | | |
| 0 | IO_L45N_0 | | H19 | | | |
| 0 | IO_L45P_0/VREF_0 | | G19 | | | |
| 0 | IO_L46N_0 | | E19 | NC | | |
| 0 | IO_L46P_0 | | E18 | NC | | |
| 0 | IO_L47N_0 | | C22 | NC | | |
| 0 | IO_L47P_0 | | B22 | NC | | |
| 0 | IO_L48N_0 | | F20 | NC | | |
| 0 | IO_L48P_0 | | F19 | NC | | |
| 0 | IO_L49N_0 | | G17 | NC | | |
| 0 | IO_L49P_0 | | F17 | NC | | |
| 0 | IO_L50_0/No_Pair | | B21 | NC | | |

*Table 9:* **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

| Bank | Pin Description | | Pin Number | No Connects | | |
|---|---|---|---|---|---|---|
| | Virtex-II Pro devices | XC2VPX20 (if Different) | | XC2VP7 | XC2VP20, XC2VPX20 | XC2VP30 |
| 6 | IO_L44P_6 | | AA25 | | | |
| 6 | IO_L44N_6 | | AA26 | | | |
| 6 | IO_L45P_6 | | AC29 | | | |
| 6 | IO_L45N_6/VREF_6 | | AB29 | | | |
| 6 | IO_L46P_6 | | AB27 | | | |
| 6 | IO_L46N_6 | | AB28 | | | |
| 6 | IO_L47P_6 | | W23 | | | |
| 6 | IO_L47N_6 | | W24 | | | |
| 6 | IO_L48P_6 | | AA27 | | | |
| 6 | IO_L48N_6 | | AA28 | | | |
| 6 | IO_L49P_6 | | Y26 | | | |
| 6 | IO_L49N_6 | | Y27 | | | |
| 6 | IO_L50P_6 | | W25 | | | |
| 6 | IO_L50N_6 | | W26 | | | |
| 6 | IO_L51P_6 | | AB30 | | | |
| 6 | IO_L51N_6/VREF_6 | | AA30 | | | |
| 6 | IO_L52P_6 | | W27 | | | |
| 6 | IO_L52N_6 | | W28 | | | |
| 6 | IO_L53P_6 | | V23 | | | |
| 6 | IO_L53N_6 | | V24 | | | |
| 6 | IO_L54P_6 | | AA29 | | | |
| 6 | IO_L54N_6 | | Y29 | | | |
| 6 | IO_L55P_6 | | V25 | | | |
| 6 | IO_L55N_6 | | V26 | | | |
| 6 | IO_L56P_6 | | U23 | | | |
| 6 | IO_L56N_6 | | U24 | | | |
| 6 | IO_L57P_6 | | Y30 | | | |
| 6 | IO_L57N_6/VREF_6 | | W30 | | | |
| 6 | IO_L58P_6 | | V27 | | | |
| 6 | IO_L58N_6 | | V28 | | | |
| 6 | IO_L59P_6 | | U22 | | | |
| 6 | IO_L59N_6 | | T22 | | | |
| 6 | IO_L60P_6 | | W29 | | | |
| 6 | IO_L60N_6 | | V29 | | | |
| 6 | IO_L85P_6 | | U26 | | | |
| 6 | IO_L85N_6 | | U27 | | | |

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

| Bank | Pin Description | | Pin Number | No Connects | | |
|---|---|---|---|---|---|---|
| | Virtex-II Pro devices | XC2VPX20 (if Different) | | XC2VP7 | XC2VP20, XC2VPX20 | XC2VP30 |
| N/A | TXPPAD19 | | AK19 | | | |
| N/A | TXNPAD19 | | AK20 | | | |
| N/A | VTTXPAD19 | | AJ20 | | | |
| N/A | AVCCAUXTX19 | | AJ19 | | | |
| N/A | AVCCAUXRX21 | | AJ24 | | | |
| N/A | VTRXPAD21 | | AJ25 | | | |
| N/A | RXNPAD21 | | AK24 | | | |
| N/A | RXPPAD21 | | AK25 | | | |
| N/A | GNDA21 | | AH25 | | | |
| N/A | TXPPAD21 | | AK26 | | | |
| N/A | TXNPAD21 | | AK27 | | | |
| N/A | VTTXPAD21 | | AJ27 | | | |
| N/A | AVCCAUXTX21 | | AJ26 | | | |
| | | | | | | |
| N/A | VCCAUX | | AK29 | | | |
| N/A | VCCAUX | | AK16 | | | |
| N/A | VCCAUX | | AK15 | | | |
| N/A | VCCAUX | | AK2 | | | |
| N/A | VCCAUX | | AJ30 | | | |
| N/A | VCCAUX | | AJ1 | | | |
| N/A | VCCAUX | | T30 | | | |
| N/A | VCCAUX | | T1 | | | |
| N/A | VCCAUX | | R30 | | | |
| N/A | VCCAUX | | R1 | | | |
| N/A | VCCAUX | | B30 | | | |
| N/A | VCCAUX | | B1 | | | |
| N/A | VCCAUX | | A29 | | | |
| N/A | VCCAUX | | A16 | | | |
| N/A | VCCAUX | | A15 | | | |
| N/A | VCCAUX | | A2 | | | |
| N/A | VCCINT | | Y19 | | | |
| N/A | VCCINT | | Y18 | | | |
| N/A | VCCINT | | Y17 | | | |
| N/A | VCCINT | | Y16 | | | |
| N/A | VCCINT | | Y15 | | | |
| N/A | VCCINT | | Y14 | | | |

*Table 10:* **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | | | |
|---|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 |
| N/A | TXPPAD17 | AP12 | NC | NC | NC | |
| N/A | TXNPAD17 | AP13 | NC | NC | NC | |
| N/A | VTTXPAD17 | AN13 | NC | NC | NC | |
| N/A | AVCCAUXTX17 | AN12 | NC | NC | NC | |
| N/A | AVCCAUXRX18 | AN14 | | | | |
| N/A | VTRXPAD18 | AN15 | | | | |
| N/A | RXNPAD18 | AP14 | | | | |
| N/A | RXPPAD18 | AP15 | | | | |
| N/A | GNDA18 | AM15 | | | | |
| N/A | TXPPAD18 | AP16 | | | | |
| N/A | TXNPAD18 | AP17 | | | | |
| N/A | VTTXPAD18 | AN17 | | | | |
| N/A | AVCCAUXTX18 | AN16 | | | | |
| N/A | AVCCAUXRX19 | AN18 | | | | |
| N/A | VTRXPAD19 | AN19 | | | | |
| N/A | RXNPAD19 | AP18 | | | | |
| N/A | RXPPAD19 | AP19 | | | | |
| N/A | GNDA19 | AM20 | | | | |
| N/A | TXPPAD19 | AP20 | | | | |
| N/A | TXNPAD19 | AP21 | | | | |
| N/A | VTTXPAD19 | AN21 | | | | |
| N/A | AVCCAUXTX19 | AN20 | | | | |
| N/A | AVCCAUXRX20 | AN22 | NC | NC | NC | |
| N/A | VTRXPAD20 | AN23 | NC | NC | NC | |
| N/A | RXNPAD20 | AP22 | NC | NC | NC | |
| N/A | RXPPAD20 | AP23 | NC | NC | NC | |
| N/A | GNDA20 | AM23 | NC | NC | NC | |
| N/A | TXPPAD20 | AP24 | NC | NC | NC | |
| N/A | TXNPAD20 | AP25 | NC | NC | NC | |
| N/A | VTTXPAD20 | AN25 | NC | NC | NC | |
| N/A | AVCCAUXTX20 | AN24 | NC | NC | NC | |
| N/A | AVCCAUXRX21 | AN26 | | | | |
| N/A | VTRXPAD21 | AN27 | | | | |
| N/A | RXNPAD21 | AP26 | | | | |
| N/A | RXPPAD21 | AP27 | | | | |
| N/A | GNDA21 | AM27 | | | | |
| N/A | TXPPAD21 | AP28 | | | | |
| N/A | TXNPAD21 | AP29 | | | | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| N/A | VCCINT | M23 | | |
| N/A | VCCINT | AB22 | | |
| N/A | VCCINT | AA22 | | |
| N/A | VCCINT | Y22 | | |
| N/A | VCCINT | W22 | | |
| N/A | VCCINT | V22 | | |
| N/A | VCCINT | U22 | | |
| N/A | VCCINT | T22 | | |
| N/A | VCCINT | R22 | | |
| N/A | VCCINT | P22 | | |
| N/A | VCCINT | N22 | | |
| N/A | VCCINT | AB21 | | |
| N/A | VCCINT | N21 | | |
| N/A | VCCINT | AB20 | | |
| N/A | VCCINT | N20 | | |
| N/A | VCCINT | AB19 | | |
| N/A | VCCINT | N19 | | |
| N/A | VCCINT | AB18 | | |
| N/A | VCCINT | N18 | | |
| N/A | VCCINT | AB17 | | |
| N/A | VCCINT | N17 | | |
| N/A | VCCINT | AB16 | | |
| N/A | VCCINT | N16 | | |
| N/A | VCCINT | AB15 | | |
| N/A | VCCINT | N15 | | |
| N/A | VCCINT | AB14 | | |
| N/A | VCCINT | N14 | | |
| N/A | VCCINT | AB13 | | |
| N/A | VCCINT | AA13 | | |
| N/A | VCCINT | Y13 | | |
| N/A | VCCINT | W13 | | |
| N/A | VCCINT | V13 | | |
| N/A | VCCINT | U13 | | |
| N/A | VCCINT | T13 | | |
| N/A | VCCINT | R13 | | |
| N/A | VCCINT | P13 | | |
| N/A | VCCINT | N13 | | |
| N/A | VCCINT | AC12 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 2 | IO_L30N_2 | N6 | | |
| 2 | IO_L30P_2 | N7 | | |
| 2 | IO_L31N_2 | M4 | | |
| 2 | IO_L31P_2 | N5 | | |
| 2 | IO_L32N_2 | R11 | | |
| 2 | IO_L32P_2 | R12 | | |
| 2 | IO_L33N_2 | N1 | | |
| 2 | IO_L33P_2 | N2 | | |
| 2 | IO_L34N_2/VREF_2 | P6 | | |
| 2 | IO_L34P_2 | P7 | | |
| 2 | IO_L35N_2 | R13 | | |
| 2 | IO_L35P_2 | T13 | | |
| 2 | IO_L36N_2 | P4 | | |
| 2 | IO_L36P_2 | P5 | | |
| 2 | IO_L37N_2 | P3 | | |
| 2 | IO_L37P_2 | N3 | | |
| 2 | IO_L38N_2 | T10 | | |
| 2 | IO_L38P_2 | T11 | | |
| 2 | IO_L39N_2 | P1 | | |
| 2 | IO_L39P_2 | P2 | | |
| 2 | IO_L40N_2/VREF_2 | R7 | | |
| 2 | IO_L40P_2 | R8 | | |
| 2 | IO_L41N_2 | T12 | | |
| 2 | IO_L41P_2 | U12 | | |
| 2 | IO_L42N_2 | R5 | | |
| 2 | IO_L42P_2 | R6 | | |
| 2 | IO_L43N_2 | R3 | | |
| 2 | IO_L43P_2 | R4 | | |
| 2 | IO_L44N_2 | U8 | | |
| 2 | IO_L44P_2 | T8 | | |
| 2 | IO_L45N_2 | R1 | | |
| 2 | IO_L45P_2 | R2 | | |
| 2 | IO_L46N_2/VREF_2 | T6 | | |
| 2 | IO_L46P_2 | T7 | | |
| 2 | IO_L47N_2 | U9 | | |
| 2 | IO_L47P_2 | U10 | | |
| 2 | IO_L48N_2 | T2 | | |
| 2 | IO_L48P_2 | T3 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 6 | IO_L53P_6 | AB30 | | |
| 6 | IO_L53N_6 | AB31 | | |
| 6 | IO_L54P_6 | AC38 | | |
| 6 | IO_L54N_6 | AC39 | | |
| 6 | IO_L55P_6 | AC34 | | |
| 6 | IO_L55N_6 | AC35 | | |
| 6 | IO_L56P_6 | AA28 | | |
| 6 | IO_L56N_6 | AA29 | | |
| 6 | IO_L57P_6 | AB38 | | |
| 6 | IO_L57N_6/VREF_6 | AB39 | | |
| 6 | IO_L58P_6 | AB36 | | |
| 6 | IO_L58N_6 | AB37 | | |
| 6 | IO_L59P_6 | AA30 | | |
| 6 | IO_L59N_6 | AA31 | | |
| 6 | IO_L60P_6 | AB34 | | |
| 6 | IO_L60N_6 | AB35 | | |
| 6 | IO_L85P_6 | AB32 | | |
| 6 | IO_L85N_6 | AB33 | | |
| 6 | IO_L86P_6 | AA27 | | |
| 6 | IO_L86N_6 | Y27 | | |
| 6 | IO_L87P_6 | AA36 | | |
| 6 | IO_L87N_6/VREF_6 | AA37 | | |
| 6 | IO_L88P_6 | AA34 | | |
| 6 | IO_L88N_6 | AA35 | | |
| 6 | IO_L89P_6 | Y28 | | |
| 6 | IO_L89N_6 | Y29 | | |
| 6 | IO_L90P_6 | AA32 | | |
| 6 | IO_L90N_6 | AA33 | | |
| | | | | |
| 7 | IO_L90P_7 | Y36 | | |
| 7 | IO_L90N_7 | Y37 | | |
| 7 | IO_L89P_7 | Y31 | | |
| 7 | IO_L89N_7 | W31 | | |
| 7 | IO_L88P_7 | Y32 | | |
| 7 | IO_L88N_7/VREF_7 | Y33 | | |
| 7 | IO_L87P_7 | W36 | | |
| 7 | IO_L87N_7 | W37 | | |
| 7 | IO_L86P_7 | W27 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 5 | IO_L37N_5 | | AU28 | | |
| 5 | IO_L37P_5 | | AV28 | | |
| 5 | IO_L87N_5/VREF_5 | | AP28 | NC | |
| 5 | IO_L87P_5 | | AR28 | NC | |
| 5 | IO_L86N_5 | | AN28 | NC | |
| 5 | IO_L86P_5 | | AM28 | NC | |
| 5 | IO_L85N_5 | | AV29 | NC | |
| 5 | IO_L85P_5 | | AW29 | NC | |
| 5 | IO_L84N_5 | | AT29 | NC | |
| 5 | IO_L84P_5 | | AU29 | NC | |
| 5 | IO_L83_5/No_Pair | | AR29 | NC | |
| 5 | IO_L78N_5 | | AM29 | NC | |
| 5 | IO_L78P_5 | | AN29 | NC | |
| 5 | IO_L36N_5/VREF_5 | | AL29 | | |
| 5 | IO_L36P_5 | | AL28 | | |
| 5 | IO_L35N_5 | | AY30 | | |
| 5 | IO_L35P_5 | | AW30 | | |
| 5 | IO_L34N_5 | | AU30 | | |
| 5 | IO_L34P_5 | | AV30 | | |
| 5 | IO_L30N_5 | | AR30 | | |
| 5 | IO_L30P_5 | | AT30 | | |
| 5 | IO_L29N_5 | | AN30 | | |
| 5 | IO_L29P_5 | | AP30 | | |
| 5 | IO_L28N_5 | | AL30 | | |
| 5 | IO_L28P_5 | | AM30 | | |
| 5 | IO_L27N_5/VREF_5 | | AV31 | | |
| 5 | IO_L27P_5 | | AW31 | | |
| 5 | IO_L26N_5 | | AU31 | | |
| 5 | IO_L26P_5 | | AT31 | | |
| 5 | IO_L25N_5 | | AP31 | | |
| 5 | IO_L25P_5 | | AR31 | | |
| 5 | IO_L21N_5 | | AM31 | | |
| 5 | IO_L21P_5 | | AN31 | | |
| 5 | IO_L20N_5 | | AY32 | | |
| 5 | IO_L20P_5 | | AY33 | | |
| 5 | IO_L19N_5 | | AU32 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| N/A | RXPPAD21 | | BB31 | | |
| N/A | GNDA21 | | AY31 | | |
| N/A | TXPPAD21 | | BB32 | | |
| N/A | TXNPAD21 | | BB33 | | |
| N/A | VTTXPAD21 | | BA33 | | |
| N/A | AVCCAUXTX21 | | BA32 | | |
| N/A | AVCCAUXRX22 | | BA34 | | |
| N/A | VTRXPAD22 | | BA35 | | |
| N/A | RXNPAD22 | | BB34 | | |
| N/A | RXPPAD22 | | BB35 | | |
| N/A | GNDA22 | | AY35 | | |
| N/A | TXPPAD22 | | BB36 | | |
| N/A | TXNPAD22 | | BB37 | | |
| N/A | VTTXPAD22 | | BA37 | | |
| N/A | AVCCAUXTX22 | | BA36 | | |
| N/A | AVCCAUXRX23 | | BA38 | | |
| N/A | VTRXPAD23 | | BA39 | | |
| N/A | RXNPAD23 | | BB38 | | |
| N/A | RXPPAD23 | | BB39 | | |
| N/A | GNDA23 | | AY39 | | |
| N/A | TXPPAD23 | | BB40 | | |
| N/A | TXNPAD23 | | BB41 | | |
| N/A | VTTXPAD23 | | BA41 | | |
| N/A | AVCCAUXTX23 | | BA40 | | |
| | | | | | |
| N/A | VCCINT | | AB27 | | |
| N/A | VCCINT | | AB16 | | |
| N/A | VCCINT | | AC27 | | |
| N/A | VCCINT | | AC16 | | |
| N/A | VCCINT | | AD27 | | |
| N/A | VCCINT | | AD16 | | |
| N/A | VCCINT | | AE27 | | |
| N/A | VCCINT | | AE16 | | |
| N/A | VCCINT | | AF27 | | |
| N/A | VCCINT | | AF26 | | |
| N/A | VCCINT | | AF17 | | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects XC2VP100 |
|---|---|---|---|
| 4 | IO_L58P_4 | AW19 | |
| 4 | IO_L59N_4 | AP19 | |
| 4 | IO_L59P_4 | AN19 | |
| 4 | IO_L60N_4 | BB19 | |
| 4 | IO_L60P_4 | BA19 | |
| 4 | IO_L64N_4 | AU20 | |
| 4 | IO_L64P_4 | AT20 | |
| 4 | IO_L65N_4 | AL21 | |
| 4 | IO_L65P_4 | AL20 | |
| 4 | IO_L66N_4 | BA20 | |
| 4 | IO_L66P_4/VREF_4 | AY20 | |
| 4 | IO_L67N_4 | AR21 | |
| 4 | IO_L67P_4 | AP21 | |
| 4 | IO_L68N_4 | AN20 | |
| 4 | IO_L68P_4 | AM20 | |
| 4 | IO_L69N_4 | AU21 | |
| 4 | IO_L69P_4/VREF_4 | AT21 | |
| 4 | IO_L73N_4 | AW21 | |
| 4 | IO_L73P_4 | AV21 | |
| 4 | IO_L74N_4/GCLK3S | AN21 | |
| 4 | IO_L74P_4/GCLK2P | AM21 | |
| 4 | IO_L75N_4/GCLK1S | BA21 | |
| 4 | IO_L75P_4/GCLK0P | AY21 | |
| | | | |
| 5 | IO_L75N_5/GCLK7S | AY22 | |
| 5 | IO_L75P_5/GCLK6P | BA22 | |
| 5 | IO_L74N_5/GCLK5S | AM22 | |
| 5 | IO_L74P_5/GCLK4P | AN22 | |
| 5 | IO_L73N_5 | AV22 | |
| 5 | IO_L73P_5 | AW22 | |
| 5 | IO_L69N_5/VREF_5 | AT22 | |
| 5 | IO_L69P_5 | AU22 | |
| 5 | IO_L68N_5 | AM23 | |
| 5 | IO_L68P_5 | AN23 | |
| 5 | IO_L67N_5 | AP22 | |
| 5 | IO_L67P_5 | AR22 | |
| 5 | IO_L66N_5/VREF_5 | AY23 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 7 | IO_L87P_7 | AA37 | |
| 7 | IO_L87N_7 | AA38 | |
| 7 | IO_L86P_7 | AA33 | |
| 7 | IO_L86N_7 | AA34 | |
| 7 | IO_L85P_7 | Y40 | |
| 7 | IO_L85N_7 | Y41 | |
| 7 | IO_L60P_7 | W41 | |
| 7 | IO_L60N_7 | W42 | |
| 7 | IO_L59P_7 | AA31 | |
| 7 | IO_L59N_7 | AA32 | |
| 7 | IO_L58P_7 | V40 | |
| 7 | IO_L58N_7/VREF_7 | W40 | |
| 7 | IO_L57P_7 | W37 | |
| 7 | IO_L57N_7 | W38 | |
| 7 | IO_L56P_7 | Y36 | |
| 7 | IO_L56N_7 | Y37 | |
| 7 | IO_L55P_7 | V41 | |
| 7 | IO_L55N_7 | V42 | |
| 7 | IO_L54P_7 | V38 | |
| 7 | IO_L54N_7 | V39 | |
| 7 | IO_L53P_7 | Y31 | |
| 7 | IO_L53N_7 | Y32 | |
| 7 | IO_L52P_7 | U40 | |
| 7 | IO_L52N_7/VREF_7 | U41 | |
| 7 | IO_L51P_7 | T40 | |
| 7 | IO_L51N_7 | U39 | |
| 7 | IO_L50P_7 | Y35 | |
| 7 | IO_L50N_7 | W36 | |
| 7 | IO_L49P_7 | T37 | |
| 7 | IO_L49N_7 | U37 | |
| 7 | IO_L48P_7 | T41 | |
| 7 | IO_L48N_7 | T42 | |
| 7 | IO_L47P_7 | Y33 | |
| 7 | IO_L47N_7 | W34 | |
| 7 | IO_L46P_7 | T38 | |
| 7 | IO_L46N_7/VREF_7 | T39 | |
| 7 | IO_L45P_7 | R36 | |