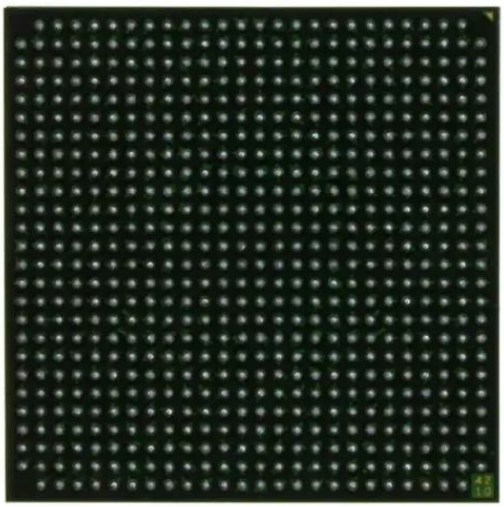

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	752
Number of Logic Elements/Cells	6768
Total RAM Bits	516096
Number of I/O	348
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2vp4-5ff672c

Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Introduction and Overview

DS083 (v5.0) June 21, 2011 **Product Specification**

Summary of Virtex-II Pro™ / Virtex-II Pro X Features

- High-Performance Platform FPGA Solution, Including
  - Up to twenty RocketIO™ or RocketIO X embedded Multi-Gigabit Transceivers (MGTs)
  - Up to two IBM PowerPC™ RISC processor blocks
- Based on Virtex-II™ Platform FPGA Technology
  - Flexible logic resources
  - SRAM-based in-system configuration
  - Active Interconnect technology
  - SelectRAM™+ memory hierarchy
  - Dedicated 18-bit x 18-bit multiplier blocks
  - High-performance clock management circuitry
  - SelectI/O™-Ultra technology
  - XCITE Digitally Controlled Impedance (DCI) I/O

Virtex-II Pro / Virtex-II Pro X family members and resources are shown in Table 1.

Table 1: **Virtex-II Pro / Virtex-II Pro X FPGA Family Members**

Device[1]	RocketIO Transceiver Blocks	PowerPC Processor Blocks	Logic Cells[2]	CLB (1 = 4 slices = max 128 bits)		18 X 18 Bit Multiplier Blocks	Block SelectRAM+		DCMs	Maximum User I/O Pads
				Slices	Max Distr RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)		
XC2VP2	4	0	3,168	1,408	44	12	12	216	4	204
XC2VP4	4	1	6,768	3,008	94	28	28	504	4	348
XC2VP7	8	1	11,088	4,928	154	44	44	792	4	396
XC2VP20	8	2	20,880	9,280	290	88	88	1,584	8	564
XC2VPX20	8[4]	1	22,032	9,792	306	88	88	1,584	8	552
XC2VP30	8	2	30,816	13,696	428	136	136	2,448	8	644
XC2VP40	0[3], 8, or 12	2	43,632	19,392	606	192	192	3,456	8	804
XC2VP50	0[3] or 16	2	53,136	23,616	738	232	232	4,176	8	852
XC2VP70	16 or 20	2	74,448	33,088	1,034	328	328	5,904	8	996
XC2VPX70	20[4]	2	74,448	33,088	1,034	308	308	5,544	8	992
XC2VP100	0[3] or 20	2	99,216	44,096	1,378	444	444	7,992	12	1,164

Notes:
1. -7 speed grade devices are not available in Industrial grade.
2. Logic Cell ≈ (1) 4-input LUT + (1)FF + Carry Logic
3. These devices can be ordered in a configuration without RocketIO transceivers. See Table 3 for package configurations.
4. Virtex-II Pro X devices equipped with RocketIO X transceiver cores.

RocketIO X Transceiver Features (XC2VPX20 and XC2VPX70 Only)

- Variable-Speed Full-Duplex Transceiver (XC2VPX20) Allowing 2.488 Gb/s to 6.25 Gb/s Baud Transfer Rates.
  - Includes specific baud rates used by various standards, as listed in Table 4, Module 2.
- Fixed-Speed Full-Duplex Tranceiver (XC2VPX70) Operating at 4.25 Gb/s Baud Transfer Rate.
- Eight or Twenty Transceiver Modules on an FPGA, Depending upon Device
- Monolithic Clock Synthesis and Clock Recovery
  - Eliminates the need for external components
- Automatic Lock-to-Reference Function
- Programmable Serial Output Differential Swing
  - 200 mV to 1600 mV, peak-peak
  - Allows compatibility with other serial system voltage levels
- Programmable Pre-emphasis Levels 0 to 500%
- Telecom/Datacom Support Modes
  - "x8" and "x10" clocking/data paths
  - 64B/66B clocking support

Disparity Control

The 8B/10B encoder is initialized with a negative running disparity. Unique control allows forcing the current running disparity state.

TXRUNDISP signals its current running disparity. This may be useful in those cases where there is a need to manipulate the initial running disparity value.

Bits TXCHARDISPMODE and TXCHARDISPVAL control the generation of running disparity before each byte.

For example, the transceiver can generate the sequence

```
K28.5+ K28.5+ K28.5- K28.5-
```

or

```
K28.5- K28.5- K28.5+ K28.5+
```

by specifying inverted running disparity for the second and fourth bytes.

Transmit FIFO

Proper operation of the circuit is only possible if the FPGA clock (TXUSRCLK) is frequency-locked to the reference clock (REFCLK). Phase variations up to one clock cycle are allowable. The FIFO has a depth of four. Overflow or underflow conditions are detected and signaled at the interface. Bypassing of this FIFO is programmable.

8B/10B Encoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

A bypassable 8B/10B encoder is included. The encoder uses the same 256 data characters and 12 control characters used by Gigabit Ethernet, Fibre Channel, and InfiniBand.

The encoder accepts 8 bits of data along with a K-character signal for a total of 9 bits per character applied, and generates a 10 bit character for transmission. If the K-character signal is High, the data is encoded into one of the twelve possible K-characters available in the 8B/10B code. If the K-character input is Low, the 8 bits are encoded as standard data. If the K-character input is High, and a user applies other than one of the twelve possible combinations, TXKERR indicates the error.

8B/10B Decoder

Note: In the RocketIO transceiver, the most-significant byte is sent first; in the RocketIO X transceiver, the least-significant byte is sent first.

An optional 8B/10B decoder is included. A programmable option allows the decoder to be bypassed. When the 8B/10B decoder is bypassed, the 10-bit character order is, for example,

RXCHARISK[0] (first bit received)
RXRUNDISP[0]
RXDATA[7:0] (last bit received is RXDATA[0])

The decoder uses the same table that is used for Gigabit Ethernet, Fibre Channel, and InfiniBand. In addition to decoding all data and K-characters, the decoder has several extra features. The decoder separately detects both “disparity errors” and “out-of-band” errors. A disparity error is the reception of 10-bit character that exists within the 8B/10B table but has an incorrect disparity. An out-of-band error is the reception of a 10-bit character that does not exist within the 8B/10B table. It is possible to obtain an out-of-band error without having a disparity error. The proper disparity is always computed for both legal and illegal characters. The current running disparity is available at the RXRUNDISP signal.

The 8B/10B decoder performs a unique operation if out-of-band data is detected. If out-of-band data is detected, the decoder signals the error and passes the illegal 10-bits through and places them on the outputs. This can be used for debugging purposes if desired.

The decoder also signals the reception of one of the 12 valid K-characters. In addition, a programmable comma detect is included. The comma detect signal registers a comma on the receipt of any comma+, comma–, or both. Since the comma is defined as a 7-bit character, this includes several out-of-band characters. Another option allows the decoder to detect only the three defined commas (K28.1, K28.5, and K28.7) as comma+, comma–, or both. In total, there are six possible options, three for valid commas and three for "any comma."

Note that all bytes (1, 2, 4, or 8) at the RX FPGA interface each have their own individual 8B/10B indicators (K-character, disparity error, out-of-band error, current running disparity, and comma detect).

Receiver Buffer

The receiver includes buffers (FIFOs) in the datapath. This section gives the reasons for including the buffers and outlines their operation.

The receiver buffer is required for two reasons:

- *Clock correction* to accommodate the slight difference in frequency between the recovered clock RXRECCLK and the internal FPGA user clock RXUSRCLK
- *Channel bonding* to allow realignment of the input stream to ensure proper alignment of data being read through multiple transceivers

The receiver uses an *elastic buffer*, where "elastic" refers to the ability to modify the read pointer for clock correction and channel bonding.

Comma Detection

Word alignment is dependent on the state of comma detect bits. If comma detect is enabled, the transceiver recognizes up to two 10-bit preprogrammed characters. Upon detection of the character or characters, the comma detect output is driven high and the data is synchronously aligned. If a comma is detected and the data is aligned, no further alignment alteration takes place. If a comma is received and realignment is necessary, the data is realigned and an indi-

Table 12: **Summary of Voltage Supply Requirements for All Input and Output Standards**

I/O Standard	V_{CCO}		V_{REF}	Termination Type	
	Output	Input	Input	Output	Input
LVTTL(1)	3.3	3.3	N/R	N/R	N/R
LVCMOS33(1)			N/R	N/R	N/R
LVDCI_33(1)			N/R	Series	N/R
PCIX(2)			N/R	N/R	N/R
PCI33_3(2)			N/R	N/R	N/R
PCI66_3(2)			N/R	N/R	N/R
LVDS_25	2.5	Note (3)	N/R	N/R	N/R
LVDSEXT_25			N/R	N/R	N/R
LDT_25			N/R	N/R	N/R
ULVDS_25			N/R	N/R	N/R
BLVDS_25			N/R	N/R	N/R
LVPECL_25			N/R	N/R	N/R
SSTL2_I			1.25	N/R	N/R
SSTL2_II			1.25	N/R	N/R
LVCMOS25		2.5	N/R	N/R	N/R
LVDCI_25			N/R	Series	N/R
LVDCI_DV2_25			N/R	Series	N/R
LVDS_25_DCI			N/R	N/R	Split
LVDSEXT_25_DCI			N/R	N/R	Split
SSTL2_I_DCI			1.25	N/R	Split
SSTL2_II_DCI			1.25	Split	Split
LVDS_25_DT			N/R	N/R	N/R
LVDSEXT_25_DT			N/R	N/R	N/R
LDT_25_DT			N/R	N/R	N/R
ULVDS_25_DT			N/R	N/R	N/R

Table 12: **Summary of Voltage Supply Requirements for All Input and Output Standards *(Continued)***

I/O Standard	V_{CCO}		V_{REF}	Termination Type	
	Output	Input	Input	Output	Input
HSTL_III_18	1.8	Note (3)	1.1	N/R	N/R
HSTL_IV_18			1.1	N/R	N/R
HSTL_I_18			0.9	N/R	N/R
HSTL_II_18			0.9	N/R	N/R
SSTL18_I			0.9	N/R	N/R
SSTL18_II			0.9	N/R	N/R
LVCMOS18		1.8	N/R	N/R	N/R
LVDCI_18			N/R	Series	N/R
LVDCI_DV2_18			N/R	Series	N/R
HSTL_III_DCI_18			1.1	N/R	Single
HSTL_IV_DCI_18			1.1	Single	Single
HSTL_I_DCI_18			0.9	N/R	Split
HSTL_II_DCI_18			0.9	Split	Split
SSTL18_I_DCI			0.9	N/R	Split
SSTL18_II_DCI			0.9	Split	Split
HSTL_III	1.5	Note (3)	0.9	N/R	N/R
HSTL_IV			0.9	N/R	N/R
HSTL_I			0.75	N/R	N/R
HSTL_II			0.75	N/R	N/R
LVCMOS15		1.5	N/R	N/R	N/R
LVDCI_15			N/R	Series	N/R
LVDCI_DV2_15			N/R	Series	N/R
GTLP_DCI			1	Single	Single
HSTL_III_DCI			0.9	N/R	Single
HSTL_IV_DCI			0.9	Single	Single
HSTL_I_DCI			0.75	N/R	Split
HSTL_II_DCI			0.75	Split	Split
GTL_DCI	1.2	1.2	0.8	Single	Single
GTLP	N/R	Note (3)	1	N/R	N/R
GTL			0.8	N/R	N/R

Notes:
1. See application note **XAPP659** for more detailed information.
2. See application note **XAPP653** for more detailed information.
3. Pin voltage must not exceed V_{CCO}.
4. N/R = no requirement.

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 39. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous; however, the storage element or flip-flop is available to implement a synchronous read. Any of the 16 bits can be read out asynchronously by varying the address. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

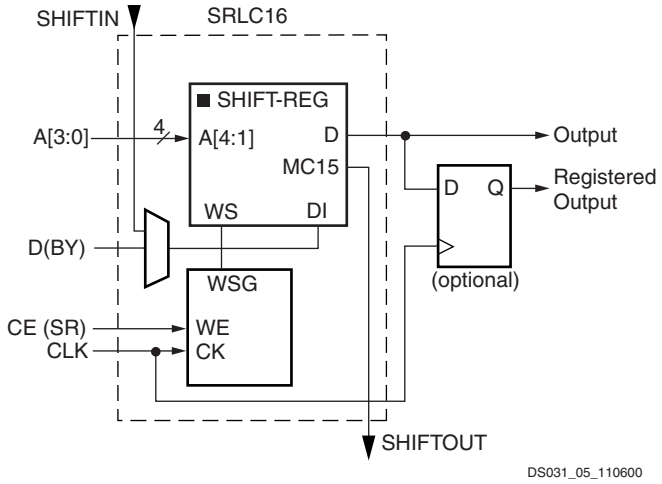

Figure 39: **Shift Register Configurations**

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See Figure 40.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

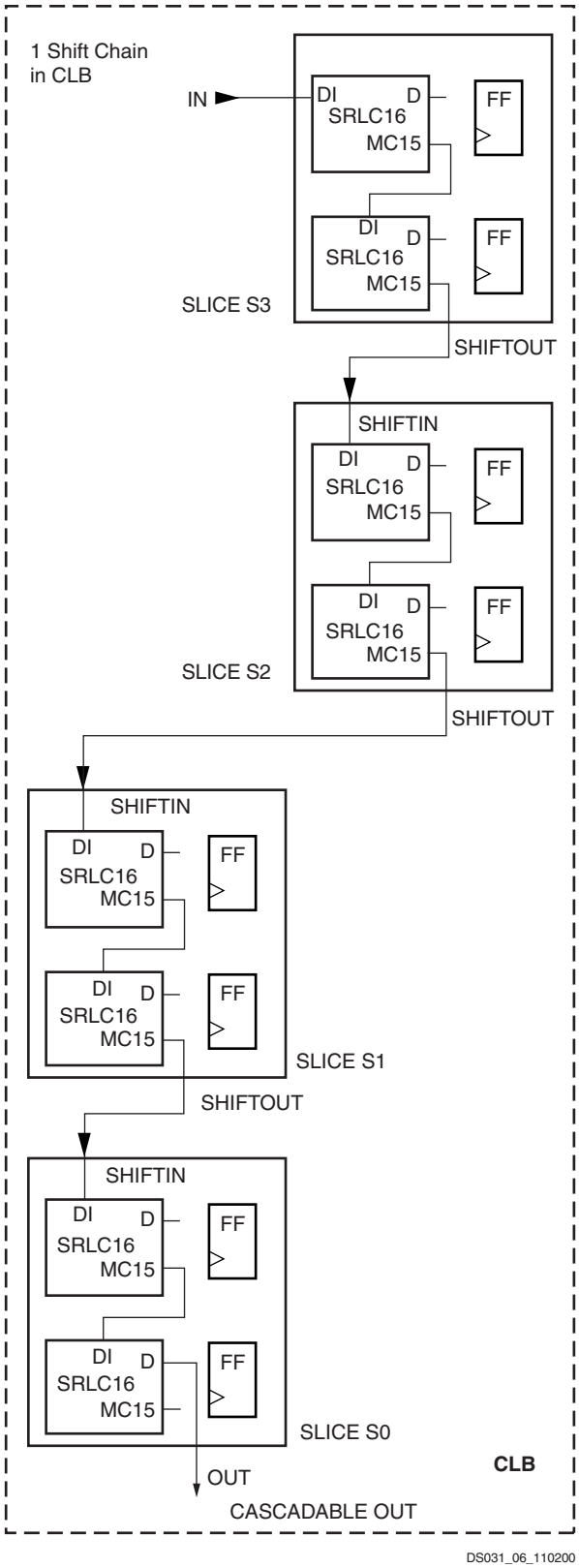

Figure 40: **Cascadable Shift Register**

18-Bit x 18-Bit Multipliers

Introduction

A Virtex-II Pro multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II Pro devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18 Kb block SelectRAM+ resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

Each SelectRAM+ memory and multiplier block is tied to four switch matrices, as shown in Figure 53.

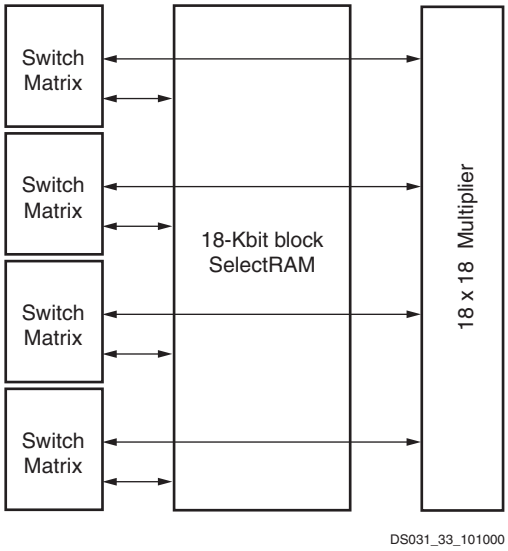

Figure 53: **SelectRAM+ and Multiplier Blocks**

Association With Block SelectRAM+ Memory

The interconnect is designed to allow SelectRAM+ memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM+ and the multiplier. Thus, SelectRAM+ memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM+ memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM+ resource feeding the multiplier. The use of SelectRAM+ memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

Configuration

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits. Figure 54 shows a multiplier block.

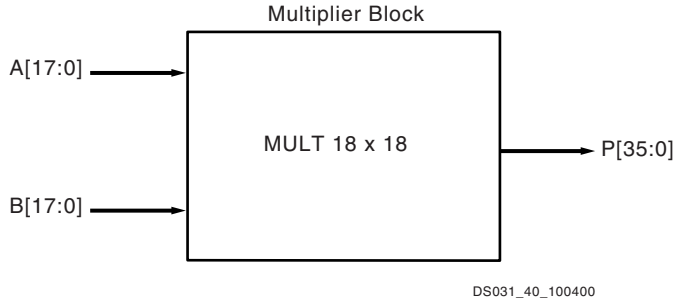

Figure 54: **Multiplier Block**

Locations / Organization

Multiplier organization is identical to the 18 Kb SelectRAM+ organization, because each multiplier is associated with an 18 Kb block SelectRAM+ resource.

Table 26: **Multiplier Resources**

Device	Columns	Total Multipliers
XC2VP2	4	12
XC2VP4	4	28
XC2VP7	6	44
XC2VP20	8	88
XC2VP30	8	136
XC2VPX20	8	88
XC2VP40	10	192
XC2VP50	12	232
XC2VP70	14	328
XC2VPX70	14	308
XC2VP100	16	444

In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic. (Refer to Configurable Logic Blocks (CLBs), page 35).

Global Clock Multiplexer Buffers

Virtex-II Pro devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads center on both the top edge and the bottom edge of the device, as illustrated in Figure 55.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II Pro devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

Date	Version	Revision
03/24/03	2.5.1	• Table 10: Corrected I/O standard names SSTL18_I and SSTL18_II to SSTL18_I_DCI and SSTL18_II_DCI respectively. • Figure 61, text below: Corrected wording of criteria for clock switching.
05/27/03	2.6	• Removed Compatible Output Standards and Compatible Input Standards tables. • Added new Table 12, Summary of Voltage Supply Requirements for All Input and Output Standards. This table replaces deleted I/O standards tables. • Corrected sentence in section Input/Output Individual Options, page 27, to read “The optional weak-keeper circuit is connected to each *user I/O pad*.” • Added section Rules for Combining I/O Standards in the Same Bank, page 29.
06/02/03	2.7	• Added four Differential Termination I/O standards to Table 9 and Table 12. • Added section On-Chip Differential Termination and Figure 31, page 34.
08/25/03	2.7.1	• Added footnote referring to XAPP659 to 3.3V I/O callouts in Table 8 and Table 12.
09/10/03	2.8	• Section Configuration, page 56: Added text indicating that the mode pins M0-M2 must be held to a constant DC level during and after configuration.
10/14/03	2.9	• Deleted section Functional Description: RocketIO Multi-Gigabit Transceiver (MGT), page 10. Added section Local Clocking, page 51. • Sections Slave-Serial Mode and Master-Serial Mode, page 56: Changed "rising" to "falling" edge with respect to DOUT. • Table 8, page 24 and Table 10, page 25: Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V.
12/10/03	3.0	• XC2VP2 through XC2VP70 speed grades -5, -6, and -7, and XC2VP100 speed grades -5 and -6, are released to **Production status**.
02/19/04	3.1	• Section BUFGMUX, page 50: Corrected the definition of the "presently selected clock" to be I0 or I1. Corrected signal names in Figure 61 and associated text from CLK0 and CLK1 to I0 and I1.
03/09/04	3.1.1	• Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
04/22/04	3.2	• Section Clock De-skew, page 52: Removed reference to CLK2X as an option for DCM clock feedback.
06/30/04	4.0	Merged in DS110-2 (Module 2 of Virtex-II Pro X data sheet). Separate RocketIO and RocketIO X sections created.
11/17/04	4.1	• Figure 11, page 12: Corrected figure by removing coupling capacitors from input. • Section Rules for Combining I/O Standards in the Same Bank, page 29: Corrected I/O standard in the first example from LVDS_25_DCI to LVDS_25.
03/01/05	4.2	• Reassigned heading hierarchies for better agreement with content. • Table 7: Corrected VCCAUXTX and VCCAUXRX to AVCCAUXTX and AVCCAUXRX respectively. • Table 9: Corrected V_{OD} (output voltage) range for LVDSEXT_25. • Table 25: Corrected SelectRAM+ memory available for XC2VPX70 device. • Table 33: Updated configuration default bitstream lengths.
06/20/05	4.3	*No changes in Module 2 for this revision.*
09/15/05	4.4	• Table 1: Deleted SONET OC-192 protocol. • Table 3: Deleted RocketIO X primitives for SONET OC-192, 10 Gbit Ethernet, and Xilinx 10G (Aurora) protocols. • Changed all instances of 10.3125 Gb/s to 6.25 Gb/s. • Table 7: Changed RocketIO X VCCAUXRX from 1.5V globally to 1.5V for 8B/10B encoding, 1.8V for all other encoding protocols.

Table 46: **Pipelined Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-7	-6	-5	
Setup and Hold Times Before/After Clock					
Data Inputs	$T_{MULIDCK}/T_{MULCKID}$	1.86/ 0.00	2.06/ 0.00	2.31/ 0.00	ns, max
Clock Enable	$T_{MULIDCK\_CE}/T_{MULCKID\_CE}$	0.23/ 0.00	0.25/ 0.00	0.28/ 0.00	ns, max
Reset	$T_{MULIDCK\_RST}/T_{MULCKID\_RST}$	0.21/–0.09	0.24/–0.09	0.26/–0.10	ns, max
Clock to Output Pin					
Clock to Pin35	T_{MULTCK_P35}	2.45	2.92	3.27	ns, max
Clock to Pin34	T_{MULTCK_P34}	2.36	2.82	3.16	ns, max
Clock to Pin33	T_{MULTCK_P33}	2.28	2.72	3.05	ns, max
Clock to Pin32	T_{MULTCK_P32}	2.20	2.62	2.93	ns, max
Clock to Pin31	T_{MULTCK_P31}	2.12	2.52	2.82	ns, max
Clock to Pin30	T_{MULTCK_P30}	2.03	2.42	2.71	ns, max
Clock to Pin29	T_{MULTCK_P29}	1.95	2.32	2.60	ns, max
Clock to Pin28	T_{MULTCK_P28}	1.87	2.22	2.48	ns, max
Clock to Pin27	T_{MULTCK_P27}	1.79	2.12	2.37	ns, max
Clock to Pin26	T_{MULTCK_P26}	1.70	2.02	2.26	ns, max
Clock to Pin25	T_{MULTCK_P25}	1.62	1.92	2.15	ns, max
Clock to Pin24	T_{MULTCK_P24}	1.54	1.82	2.03	ns, max
Clock to Pin23	T_{MULTCK_P23}	1.46	1.71	1.92	ns, max
Clock to Pin22	T_{MULTCK_P22}	1.37	1.61	1.81	ns, max
Clock to Pin21	T_{MULTCK_P21}	1.29	1.51	1.69	ns, max
Clock to Pin20	T_{MULTCK_P20}	1.21	1.41	1.58	ns, max
Clock to Pin19	T_{MULTCK_P19}	1.13	1.31	1.47	ns, max
Clock to Pin18	T_{MULTCK_P18}	1.04	1.21	1.36	ns, max
Clock to Pin17	T_{MULTCK_P17}	0.96	1.11	1.24	ns, max
Clock to Pin16	T_{MULTCK_P16}	0.88	1.01	1.13	ns, max
Clock to Pin15	T_{MULTCK_P15}	0.80	0.91	1.02	ns, max
Clock to Pin14	T_{MULTCK_P14}	0.71	0.81	0.91	ns, max
Clock to Pin13	T_{MULTCK_P13}	0.63	0.71	0.79	ns, max
Clock to Pin12	T_{MULTCK_P12}	0.63	0.71	0.79	ns, max
Clock to Pin11	T_{MULTCK_P11}	0.63	0.71	0.79	ns, max
Clock to Pin10	T_{MULTCK_P10}	0.63	0.71	0.79	ns, max
Clock to Pin9	T_{MULTCK_P9}	0.63	0.71	0.79	ns, max
Clock to Pin8	T_{MULTCK_P8}	0.63	0.71	0.79	ns, max
Clock to Pin7	T_{MULTCK_P7}	0.63	0.71	0.79	ns, max
Clock to Pin6	T_{MULTCK_P6}	0.63	0.71	0.79	ns, max
Clock to Pin5	T_{MULTCK_P5}	0.63	0.71	0.79	ns, max
Clock to Pin4	T_{MULTCK_P4}	0.63	0.71	0.79	ns, max
Clock to Pin3	T_{MULTCK_P3}	0.63	0.71	0.79	ns, max
Clock to Pin2	T_{MULTCK_P2}	0.63	0.71	0.79	ns, max
Clock to Pin1	T_{MULTCK_P1}	0.63	0.71	0.79	ns, max
Clock to Pin0	T_{MULTCK_P0}	0.63	0.71	0.79	ns, max

Input Clock Tolerances

Table 58: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			–7		–6		–5		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/High Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz	25.00		25.00		25.00		ns
PSCLK and CLKIN(3)	PSCLK_PULSE and CLKIN_PULSE	1 – 10 MHz	25.00		25.00		25.00		ns
		10 – 25 MHz	10.00		10.00		10.00		ns
		25 – 50 MHz	5.00		5.00		5.00		ns
		50 – 100 MHz	3.00		3.00		3.00		ns
		100 – 150 MHz	2.40		2.40		2.40		ns
		150 – 200 MHz	2.00		2.00		2.00		ns
		200 – 250 MHz	1.80		1.80		1.80		ns
		250 – 300 MHz	1.50		1.50		1.50		ns
		300 – 350 MHz	1.30		1.30		1.30		ns
		350 – 400 MHz	1.15		1.15		1.15		ns
		> 400 MHz	1.05		1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_LF			±300		±300		±300	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_LF			±300		±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_HF			±150		±150		±150	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_HF			±150		±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_LF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_LF			±1		±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_HF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_HF			±1		±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT			±1		±1		±1	ns

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
1	IO_L07P_1	F14			
1	IO_L06N_1	C15			
1	IO_L06P_1	D15			
1	IO_L05_1/No_Pair	E15			
1	IO_L03N_1/VREF_1	C16			
1	IO_L03P_1	D16			
1	IO_L02N_1	E16			
1	IO_L02P_1	E17			
1	IO_L01N_1/VRP_1	D17			
1	IO_L01P_1/VRN_1	D18			
2	IO_L01N_2/VRP_2	C21			
2	IO_L01P_2/VRN_2	C22			
2	IO_L02N_2	D21			
2	IO_L02P_2	D22			
2	IO_L03N_2	E19			
2	IO_L03P_2	E20			
2	IO_L04N_2/VREF_2	E21			
2	IO_L04P_2	E22			
2	IO_L06N_2	F19			
2	IO_L06P_2	F20			
2	IO_L43N_2	F21	NC		
2	IO_L43P_2	F22	NC		
2	IO_L46N_2/VREF_2	F18	NC		
2	IO_L46P_2	G18	NC		
2	IO_L48N_2	G19	NC		
2	IO_L48P_2	G20	NC		
2	IO_L49N_2	G21	NC		
2	IO_L49P_2	G22	NC		
2	IO_L50N_2	H19	NC		
2	IO_L50P_2	H20	NC		
2	IO_L52N_2/VREF_2	H21	NC		
2	IO_L52P_2	H22	NC		
2	IO_L54N_2	H18	NC		
2	IO_L54P_2	J17	NC		
2	IO_L55N_2	J19	NC		
2	IO_L55P_2	J20	NC		

Table 6: **FG456/FGG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
2	IO_L56N_2	J21	NC		
2	IO_L56P_2	J22	NC		
2	IO_L58N_2/VREF_2	J18	NC		
2	IO_L58P_2	K18	NC		
2	IO_L60N_2	K19	NC		
2	IO_L60P_2	K20	NC		
2	IO_L85N_2	K21			
2	IO_L85P_2	K22			
2	IO_L86N_2	K17			
2	IO_L86P_2	L17			
2	IO_L88N_2/VREF_2	L18			
2	IO_L88P_2	L19			
2	IO_L90N_2	L20			
2	IO_L90P_2	L21			
3	IO_L90N_3	M21			
3	IO_L90P_3	M20			
3	IO_L89N_3	M19			
3	IO_L89P_3	M18			
3	IO_L87N_3/VREF_3	M17			
3	IO_L87P_3	N17			
3	IO_L85N_3	N22			
3	IO_L85P_3	N21			
3	IO_L60N_3	N20	NC		
3	IO_L60P_3	N19	NC		
3	IO_L59N_3	N18	NC		
3	IO_L59P_3	P18	NC		
3	IO_L57N_3/VREF_3	P22	NC		
3	IO_L57P_3	P21	NC		
3	IO_L55N_3	P20	NC		
3	IO_L55P_3	P19	NC		
3	IO_L54N_3	P17	NC		
3	IO_L54P_3	R18	NC		
3	IO_L53N_3	R22	NC		
3	IO_L53P_3	R21	NC		
3	IO_L51N_3/VREF_3	R20	NC		
3	IO_L51P_3	R19	NC		

FG676/FGG676 Fine-Pitch BGA Package

As shown in Table 7, XC2VP20, XC2VP30, and XC2VP40 Virtex-II Pro devices are available in the FG676/FGG676 fine-pitch BGA package. The pins in these devices are the same, except for the differences shown in the "No Connects" column. Following this table are the FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
0	IO_L01N_0/VRP_0	E5			
0	IO_L01P_0/VRN_0	D5			
0	IO_L02N_0	E6			
0	IO_L02P_0	D6			
0	IO_L03N_0	G7			
0	IO_L03P_0/VREF_0	F7			
0	IO_L05_0/No_Pair	E7			
0	IO_L06N_0	D7			
0	IO_L06P_0	C7			
0	IO_L07N_0	H8			
0	IO_L07P_0	G8			
0	IO_L09N_0	F8			
0	IO_L09P_0/VREF_0	E8			
0	IO_L37N_0	B8			
0	IO_L37P_0	A8			
0	IO_L39N_0	H9			
0	IO_L39P_0	G9			
0	IO_L43N_0	F9			
0	IO_L43P_0	E9			
0	IO_L45N_0	D9			
0	IO_L45P_0/VREF_0	C9			
0	IO_L46N_0	H10			
0	IO_L46P_0	H11			
0	IO_L48N_0	E10			
0	IO_L48P_0	E11			
0	IO_L49N_0	D10			
0	IO_L49P_0	C10			
0	IO_L50_0/No_Pair	G11			
0	IO_L53_0/No_Pair	F11			
0	IO_L54N_0	J12			
0	IO_L54P_0	H12			

Table 7: **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP20	XC2VP30	XC2VP40
3	IO_L49N_3	T24			
3	IO_L49P_3	U24			
3	IO_L48N_3	U23			
3	IO_L48P_3	U22			
3	IO_L47N_3	T19			
3	IO_L47P_3	U19			
3	IO_L45N_3/VREF_3	V26			
3	IO_L45P_3	V25			
3	IO_L43N_3	V24			
3	IO_L43P_3	V23			
3	IO_L42N_3	V22			
3	IO_L42P_3	V21			
3	IO_L41N_3	V20			
3	IO_L41P_3	V19			
3	IO_L39N_3/VREF_3	W26			
3	IO_L39P_3	W25			
3	IO_L37N_3	W21			
3	IO_L37P_3	W20			
3	IO_L36N_3	Y26			
3	IO_L36P_3	Y25			
3	IO_L35N_3	Y24			
3	IO_L35P_3	Y23			
3	IO_L33N_3/VREF_3	W22			
3	IO_L33P_3	Y22			
3	IO_L31N_3	AA26			
3	IO_L31P_3	AA25			
3	IO_L24N_3	AA24	NC		
3	IO_L24P_3	AA23	NC		
3	IO_L23N_3	Y21	NC		
3	IO_L23P_3	AA21	NC		
3	IO_L06N_3	AB26			
3	IO_L06P_3	AB25			
3	IO_L05N_3	AA22			
3	IO_L05P_3	AB23			
3	IO_L03N_3/VREF_3	AC26			

FF672 Flip-Chip Fine-Pitch BGA Package

As shown in Table 8, XC2VP2, XC2VP4, and XC2VP7 Virtex-II Pro devices are available in the FF672 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for differences shown in the "No Connects" column. Following this table are the FF672 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
0	IO_L01N_0/VRP_0	B24			
0	IO_L01P_0/VRN_0	A24			
0	IO_L02N_0	D21			
0	IO_L02P_0	C21			
0	IO_L03N_0	E20			
0	IO_L03P_0/VREF_0	D20			
0	IO_L05_0/No_Pair	F19			
0	IO_L06N_0	E19			
0	IO_L06P_0	E18			
0	IO_L07N_0	D19			
0	IO_L07P_0	C19			
0	IO_L08N_0	B19			
0	IO_L08P_0	A19			
0	IO_L09N_0	G18			
0	IO_L09P_0/VREF_0	F18			
0	IO_L37N_0	D18	NC	NC	
0	IO_L37P_0	C18	NC	NC	
0	IO_L38N_0	G17	NC	NC	
0	IO_L38P_0	H16	NC	NC	
0	IO_L39N_0	F17	NC	NC	
0	IO_L39P_0	F16	NC	NC	
0	IO_L43N_0	E17	NC	NC	
0	IO_L43P_0	D17	NC	NC	
0	IO_L44N_0	G16	NC	NC	
0	IO_L44P_0	G15	NC	NC	
0	IO_L45N_0	E16	NC	NC	
0	IO_L45P_0/VREF_0	D16	NC	NC	
0	IO_L67N_0	F15			
0	IO_L67P_0	E15			
0	IO_L68N_0	D15			
0	IO_L68P_0	C15			
0	IO_L69N_0	H15			
0	IO_L69P_0/VREF_0	H14			

Table 9: **FF896 — XC2VP7, XC2VP20, XC2VPX20, and XC2VP30**

Bank	Pin Description		Pin Number	No Connects		
	Virtex-II Pro devices	XC2VPX20 (if Different)		XC2VP7	XC2VP20, XC2VPX20	XC2VP30
2	IO_L59N_2		P8			
2	IO_L59P_2		P7			
2	IO_L60N_2		N4			
2	IO_L60P_2		N3			
2	IO_L85N_2		P3			
2	IO_L85P_2		P2			
2	IO_L86N_2		R8			
2	IO_L86P_2		R7			
2	IO_L87N_2		P5			
2	IO_L87P_2		P4			
2	IO_L88N_2/VREF_2		R2			
2	IO_L88P_2		T2			
2	IO_L89N_2		R6			
2	IO_L89P_2		R5			
2	IO_L90N_2		R4			
2	IO_L90P_2		R3			
3	IO_L90N_3		U1			
3	IO_L90P_3		V1			
3	IO_L89N_3		T5			
3	IO_L89P_3		T6			
3	IO_L88N_3		T3			
3	IO_L88P_3		T4			
3	IO_L87N_3/VREF_3		U2			
3	IO_L87P_3		U3			
3	IO_L86N_3		T7			
3	IO_L86P_3		T8			
3	IO_L85N_3		U4			
3	IO_L85P_3		U5			
3	IO_L60N_3		V2			
3	IO_L60P_3		W2			
3	IO_L59N_3		T9			
3	IO_L59P_3		U9			
3	IO_L58N_3		V3			
3	IO_L58P_3		V4			
3	IO_L57N_3/VREF_3		W1			

Table 10: **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

Bank	Pin Description	Pin Number	No Connects			
			XC2VP20	XC2VP30	XC2VP40	XC2VP50
3	IO_L58P_3	W6				
3	IO_L57N_3/VREF_3	Y3				
3	IO_L57P_3	Y4				
3	IO_L56N_3	W7				
3	IO_L56P_3	W8				
3	IO_L55N_3	Y6				
3	IO_L55P_3	Y7				
3	IO_L54N_3	AA2				
3	IO_L54P_3	AB2				
3	IO_L53N_3	W9				
3	IO_L53P_3	W10				
3	IO_L52N_3	AA3				
3	IO_L52P_3	AA4				
3	IO_L51N_3/VREF_3	AB1				
3	IO_L51P_3	AC1				
3	IO_L50N_3	Y9				
3	IO_L50P_3	Y10				
3	IO_L49N_3	AA5				
3	IO_L49P_3	AA6				
3	IO_L48N_3	AB3				
3	IO_L48P_3	AB4				
3	IO_L47N_3	AA7				
3	IO_L47P_3	AA8				
3	IO_L46N_3	AB5				
3	IO_L46P_3	AB6				
3	IO_L45N_3/VREF_3	AC2				
3	IO_L45P_3	AD2				
3	IO_L44N_3	AA9				
3	IO_L44P_3	AA10				
3	IO_L43N_3	AC3				
3	IO_L43P_3	AC4				
3	IO_L42N_3	AD1				
3	IO_L42P_3	AE1				
3	IO_L41N_3	AB7				
3	IO_L41P_3	AB8				
3	IO_L40N_3	AC6				
3	IO_L40P_3	AC7				
3	IO_L39N_3/VREF_3	AD3				

FF1148 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, XC2VP40 and XC2VP50 Virtex-II Pro devices are available in the FF1148 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the FF1148 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 11: **FF1148 — XC2VP40 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP40	XC2VP50
0	IO_L01N_0/VRP_0	E25		
0	IO_L01P_0/VRN_0	F25		
0	IO_L02N_0	J24		
0	IO_L02P_0	K24		
0	IO_L03N_0	C25		
0	IO_L03P_0/VREF_0	D25		
0	IO_L05_0/No_Pair	G25		
0	IO_L06N_0	A25		
0	IO_L06P_0	B25		
0	IO_L07N_0	G24		
0	IO_L07P_0	G23		
0	IO_L08N_0	H23		
0	IO_L08P_0	H22		
0	IO_L09N_0	E24		
0	IO_L09P_0/VREF_0	F24		
0	IO_L19N_0	C24		
0	IO_L19P_0	C23		
0	IO_L20N_0	J23		
0	IO_L20P_0	K23		
0	IO_L21N_0	A24		
0	IO_L21P_0	B24		
0	IO_L25N_0	E23		
0	IO_L25P_0	F23		
0	IO_L26N_0	K22		
0	IO_L26P_0	L22		
0	IO_L27N_0	D23		
0	IO_L27P_0/VREF_0	D22		
0	IO_L37N_0	A23		
0	IO_L37P_0	B23		
0	IO_L38N_0	J21		
0	IO_L38P_0	J20		
0	IO_L39N_0	F22		
0	IO_L39P_0	G22		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
4	IO_L66P_4/VREF_4	AU19		
4	IO_L67N_4	AM19		
4	IO_L67P_4	AL19		
4	IO_L68N_4	AK19		
4	IO_L68P_4	AJ19		
4	IO_L69N_4	AP19		
4	IO_L69P_4/VREF_4	AN19		
4	IO_L73N_4	AT19		
4	IO_L73P_4	AR19		
4	IO_L74N_4/GCLK3S	AH20		
4	IO_L74P_4/GCLK2P	AG20		
4	IO_L75N_4/GCLK1S	AL20		
4	IO_L75P_4/GCLK0P	AK20		
5	IO_L75N_5/GCLK7S	AR20		
5	IO_L75P_5/GCLK6P	AT20		
5	IO_L74N_5/GCLK5S	AH21		
5	IO_L74P_5/GCLK4P	AJ21		
5	IO_L73N_5	AP20		
5	IO_L73P_5	AP21		
5	IO_L69N_5/VREF_5	AU21		
5	IO_L69P_5	AU22		
5	IO_L68N_5	AK21		
5	IO_L68P_5	AL21		
5	IO_L67N_5	AR21		
5	IO_L67P_5	AT21		
5	IO_L66N_5/VREF_5	AN21		
5	IO_L66P_5	AN22		
5	IO_L65N_5	AM20		
5	IO_L65P_5	AM21		
5	IO_L64N_5	AR22		
5	IO_L64P_5	AT22		
5	IO_L60N_5	AP22		
5	IO_L60P_5	AR23		
5	IO_L59N_5	AG21		
5	IO_L59P_5	AG22		
5	IO_L58N_5	AL22		
5	IO_L58P_5	AM22		

Table 12: **FF1517 — XC2VP50 and XC2VP70**

Bank	Pin Description	Pin Number	No Connects	
			XC2VP50	XC2VP70
5	IO_L29N_5	AK26	NC	
5	IO_L29P_5	AL26	NC	
5	IO_L28N_5	AL27	NC	
5	IO_L28P_5	AM27	NC	
5	IO_L27N_5/VREF_5	AR28		
5	IO_L27P_5	AT28		
5	IO_L26N_5	AH26		
5	IO_L26P_5	AH27		
5	IO_L25N_5	AL28		
5	IO_L25P_5	AM28		
5	IO_L21N_5	AT29		
5	IO_L21P_5	AU29		
5	IO_L20N_5	AJ27		
5	IO_L20P_5	AJ28		
5	IO_L19N_5	AP29		
5	IO_L19P_5	AR29		
5	IO_L09N_5/VREF_5	AM29		
5	IO_L09P_5	AN29		
5	IO_L08N_5	AK29		
5	IO_L08P_5	AL29		
5	IO_L07N_5/VREF_5	AT30		
5	IO_L07P_5	AU30		
5	IO_L06N_5/VRP_5	AP30		
5	IO_L06P_5/VRN_5	AR30		
5	IO_L05_5/No_Pair	AK28		
5	IO_L03N_5/D4	AM30		
5	IO_L03P_5/D5	AN30		
5	IO_L02N_5/D6	AL30		
5	IO_L02P_5/D7	AK30		
5	IO_L01N_5/RDWR_B	AR31		
5	IO_L01P_5/CS_B	AT31		
6	IO_L01P_6/VRN_6	AU33		
6	IO_L01N_6/VRP_6	AT33		
6	IO_L02P_6	AT32		
6	IO_L02N_6	AR32		
6	IO_L03P_6	AN31		
6	IO_L03N_6/VREF_6	AM31		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
2	IO_L08P_2		K5		
2	IO_L09N_2		K8		
2	IO_L09P_2		K7		
2	IO_L10N_2/VREF_2		K2		
2	IO_L10P_2		K1		
2	IO_L11N_2		L8		
2	IO_L11P_2		L9		
2	IO_L12N_2		L6		
2	IO_L12P_2		L7		
2	IO_L13N_2		K3		
2	IO_L13P_2		L3		
2	IO_L14N_2		L5		
2	IO_L14P_2		L4		
2	IO_L15N_2		L1		
2	IO_L15P_2		L2		
2	IO_L16N_2/VREF_2		M7		
2	IO_L16P_2		M8		
2	IO_L17N_2		M11		
2	IO_L17P_2		M12		
2	IO_L18N_2		M9		
2	IO_L18P_2		M10		
2	IO_L19N_2		M2		
2	IO_L19P_2		M3		
2	IO_L20N_2		M4		
2	IO_L20P_2		M5		
2	IO_L21N_2		N7		
2	IO_L21P_2		N8		
2	IO_L22N_2/VREF_2		N5		
2	IO_L22P_2		N6		
2	IO_L23N_2		N9		
2	IO_L23P_2		N10		
2	IO_L24N_2		N3		
2	IO_L24P_2		N4		
2	IO_L25N_2		N1		
2	IO_L25P_2		N2		
2	IO_L26N_2		N11		

Table 13: **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

Bank	Pin Description		Pin Number	No Connects	
	Virtex-II Pro Devices	XC2VPX70 (if Different)		XC2VP70, XC2VPX70	XC2VP100
N/A	VCCAUX		AM11		
N/A	VCCAUX		AN33		
N/A	VCCAUX		AN10		
N/A	VCCAUX		AV39		
N/A	VCCAUX		AV4		
N/A	VCCAUX		AW38		
N/A	VCCAUX		AW22		
N/A	VCCAUX		AW21		
N/A	VCCAUX		AW5		
N/A	VCCAUX		AA42		
N/A	VCCAUX		AA41		
N/A	VCCAUX		AA2		
N/A	VCCAUX		AA1		
N/A	VCCAUX		Y42		
N/A	VCCAUX		Y1		
N/A	VCCAUX		L32		
N/A	VCCAUX		L11		
N/A	VCCAUX		K33		
N/A	VCCAUX		K10		
N/A	VCCAUX		E39		
N/A	VCCAUX		E4		
N/A	VCCAUX		D38		
N/A	VCCAUX		D22		
N/A	VCCAUX		D21		
N/A	VCCAUX		D5		
N/A	GND		AB38		
N/A	GND		AB35		
N/A	GND		AB32		
N/A	GND		AB26		
N/A	GND		AB25		
N/A	GND		AB24		
N/A	GND		AB23		
N/A	GND		AB22		
N/A	GND		AB21		
N/A	GND		AB20		
N/A	GND		AB19		