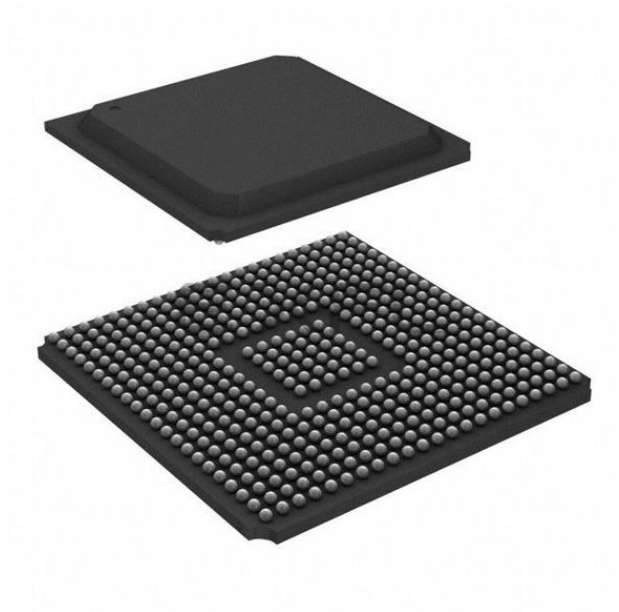
# AMD Xilinx - XC2VP4-5FG456I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 752 |
| Number of Logic Elements/Cells | 6768 |
| Total RAM Bits | 516096 |
| Number of I/O | 248 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 456-BBGA |
| Supplier Device Package | 456-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2vp4-5fg456i |

ing character, and remembers its location in the buffer. At some point, one transceiver designated as the master instructs all the transceivers to align to the channel bonding character "P" (or to some location relative to the channel bonding character).

After this operation, words transmitted to the FPGA fabric are properly aligned: RRRR, SSSS, TTTT, and so forth, as shown in the bottom-right portion of Figure 7. To ensure that the channels remain properly aligned following the channel bonding operation, the master transceiver must also control the clock correction operations described in the previous section for all channel-bonded transceivers.

### *Transmitter Buffer*

The transmitter's buffer write pointer (TXUSRCLK) is frequency-locked to its read pointer (REFCLK). Therefore, clock correction and channel bonding are not required. The purpose of the transmitter's buffer is to accommodate a phase difference between TXUSRCLK and REFCLK. A simple FIFO suffices for this purpose. A FIFO depth of four will permit reliable operation with simple detection of overflow or underflow, which could occur if the clocks are not frequency-locked.

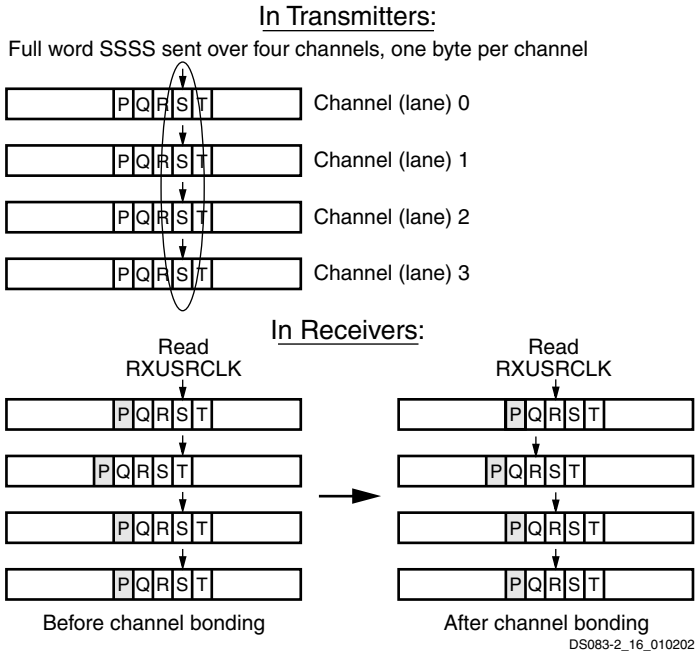


*Figure 7:* **Channel Bonding (Alignment)**

## RocketIO X Configuration

This section outlines functions that can be selected or controlled by configuration. Xilinx implementation software supports the transceiver primitives shown in Table 3.

*Table 3:* **Supported RocketIO X Transceiver Primitives**

| Primitive | Description |
|---|---|
| GT10_CUSTOM | Fully customizable by user |
| GT10_OC48_1 | SONET OC-48, 1-byte data path |
| GT10_OC48_2 | SONET OC-48, 2-byte data path |
| GT10_OC48_4 | SONET OC-48, 4-byte data path |
| GT10_PCI_EXPRESS_1 | PCI Express, 1-byte data path |
| GT10_PCI_EXPRESS_2 | PCI Express, 2-byte data path |
| GT10_PCI_EXPRESS_4 | PCI Express, 4-byte data path |
| GT10_INFINIBAND_1 | Infiniband, 1-byte data path |
| GT10_INFINIBAND_2 | Infiniband, 2-byte data path |
| GT10_INFINIBAND_4 | Infiniband, 4-byte data path |

Figure 30 provides examples illustrating the use of the LVDS_25_DCI and LVDSEXT_25_DCI I/O standards. For a complete list, see the ***Virtex-II Pro Platform FPGA User Guide***.

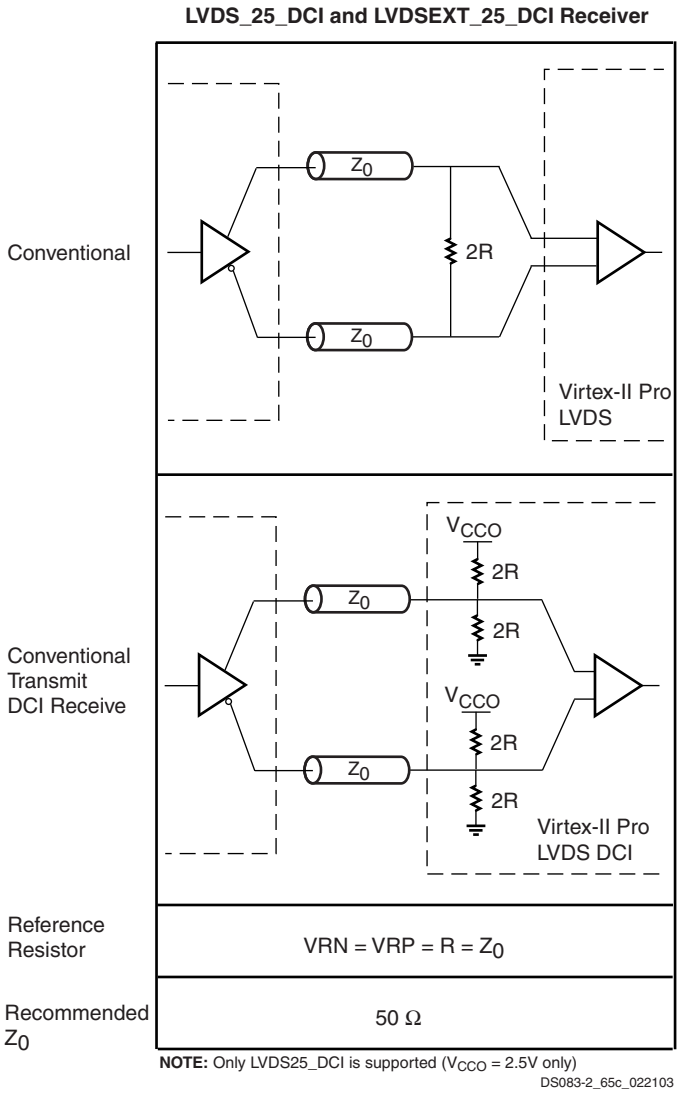


*Figure 30:* **LVDS DCI Usage Examples**

### *On-Chip Differential Termination*

Virtex-II Pro provides a true 100Ω differential termination (DT) across the input differential receiver terminals. The LVDS_25_DT, LVDSEXT_25_DT, LDT_25_DT, and ULVDS_25_DT standards support on-chip differential termination.

The on-chip input differential termination in Virtex-II Pro provides major advantages over the external resistor or the DCI termination solution:

- Eliminates the stub at the receiver completely and therefore greatly improve signal integrity
- Consumes less power than DCI termination
- Supports LDT (not supported by DCI termination)
- Frees up VRP/VRN pins

Figure 31 provides examples illustrating the use of the LVDS_25_DT, LVDSEXT_25_DT, LDT_25_DT, and ULVDS_25_DT I/O standards. For further details, refer to **Solution Record 17244**. Also see the ***Virtex-II Pro Platform FPGA User Guide*** for more design information.

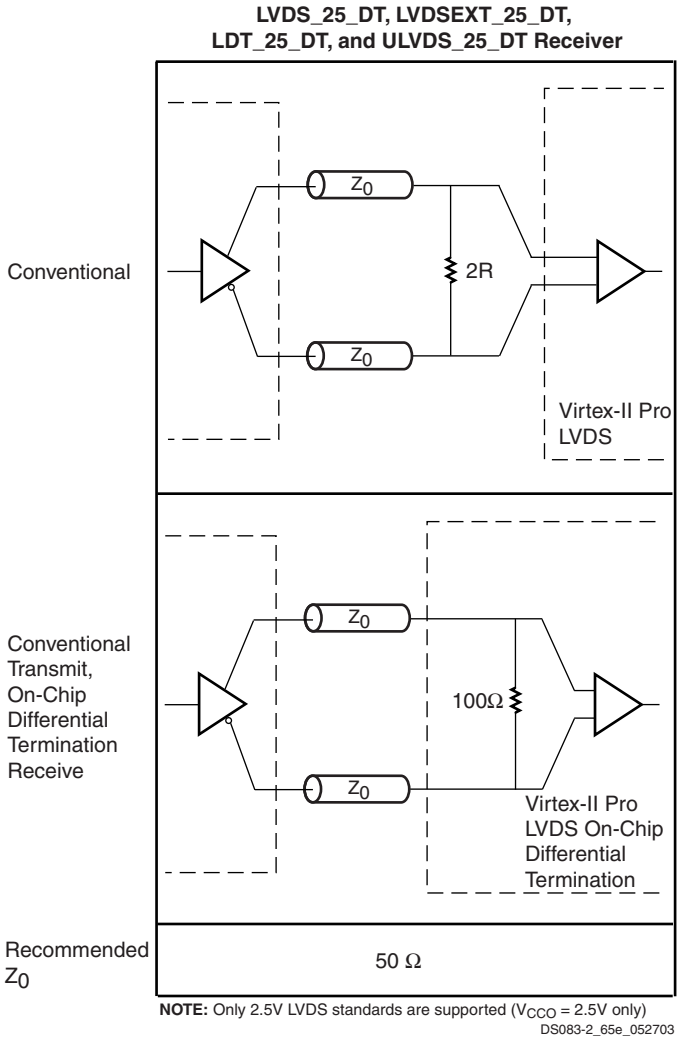


*Figure 31:* **LVDS Differential Termination Usage Examples**

nally in user logic. In such cases, the width is viewed as 8 + 1, 16 + 2, or 32 + 4. These extra parity bits are stored and behave exactly as the other bits, including the timing parameters. Video applications can use the 9-bit ratio of Virtex-II Pro block SelectRAM+ memory to advantage.

Each block SelectRAM+ cell is a fully synchronous memory as illustrated in Figure 47. Input data bus and output data bus widths are identical.

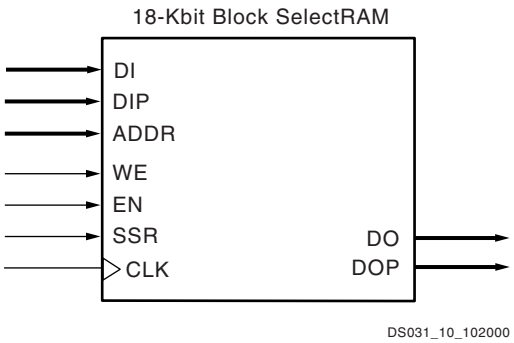


*Figure 47:* **18 Kb Block SelectRAM+ Memory in Single-Port Mode**

### Dual-Port Configuration

As a dual-port RAM, each port of block SelectRAM+ has access to a common 18 Kb memory resource. These are fully synchronous ports with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

Table 22 illustrates the different configurations available on ports A and B.

If both ports are configured in either 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations, the 18 Kb block is accessible from port A or B. If both ports are configured in either 16K x 1-bit, 8K x 2-bit. or 4K x 4-bit configurations, the 16 K-bit block is accessible from Port A or Port B. All other configurations result in one port having access to an 18 Kb memory block and the other port having access to a 16 K-bit subset of the memory block equal to 16 Kbs.

*Table 22:* **Dual-Port Mode Configurations**

| | | | | | | |
|---|---|---|---|---|---|---|
| Port A | 16K x 1 | 16K x 1 | 16K x 1 | 16K x 1 | 16K x 1 | 16K x 1 |
| Port B | 16K x 1 | 8K x 2 | 4K x 4 | 2K x 9 | 1K x 18 | 512 x 36 |
| Port A | 8K x 2 | 8K x 2 | 8K x 2 | 8K x 2 | 8K x 2 | |
| Port B | 8K x 2 | 4K x 4 | 2K x 9 | 1K x 18 | 512 x 36 | |
| Port A | 4K x 4 | 4K x 4 | 4K x 4 | 4K x 4 | | |
| Port B | 4K x 4 | 2K x 9 | 1K x 18 | 512 x 36 | | |
| Port A | 2K x 9 | 2K x 9 | 2K x 9 | | | |
| Port B | 2K x 9 | 1K x 18 | 512 x 36 | | | |
| Port A | 1K x 18 | 1K x 18 | | | | |
| Port B | 1K x 18 | 512 x 36 | | | | |
| Port A | 512 x 36 | | | | | |
| Port B | 512 x 36 | | | | | |

*Table 35:* **IOB Input Switching Characteristics *(Continued)***

| | | | Speed Grade | | | |
|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Device** | **-7** | **-6** | **-5** | **Units** |
| **Setup and Hold Times With Respect to Clock at IOB Input Register** | | | | | | |
| Pad, no delay | $T_{IOPICK}/T_{IOICKP}$ | All | 0.84/–0.61 | 0.86/–0.63 | 0.90/–0.67 | ns, min |
| Pad, with delay | $T_{IOPICKD}/T_{IOICKPD}$ | XC2VP2 | 2.28/–1.89 | 2.60/–2.15 | 2.95/–2.43 | ns, max |
| | | XC2VP4 | 2.55/–2.10 | 2.87/–2.36 | 3.21/–2.65 | ns, max |
| | | XC2VP7 | 2.48/–2.05 | 2.82/–2.32 | 3.15/–2.60 | ns, max |
| | | XC2VP20 | 2.63/–2.05 | 3.02/–2.35 | 3.40/–2.66 | ns, max |
| | | XC2VPX20 | 2.63/–2.05 | 3.02/–2.35 | 3.40/–2.66 | ns, max |
| | | XC2VP30 | 2.67/–2.07 | 3.09/–2.42 | 3.49/–2.73 | ns, max |
| | | XC2VP40 | 3.28/–2.56 | 3.61/–2.83 | 4.01/–3.15 | ns, max |
| | | XC2VP50 | 3.84/–3.02 | 4.08/–3.21 | 4.42/–3.48 | ns, max |
| | | XC2VP70 | 3.98/–3.13 | 4.23/–3.33 | 4.55/–3.58 | ns, max |
| | | XC2VPX70 | 3.98/–3.13 | 4.23/–3.33 | 4.55/–3.58 | ns, max |
| | | XC2VP100 | N/A | 6.48/–5.13 | 7.04/–5.57 | ns, max |
| ICE input | $T_{IOICECK}/T_{IOCKICE}$ | All | 0.39/ 0.01 | 0.44/ 0.01 | 0.49/ 0.01 | ns, min |
| SR input (IFF, synchronous) | $T_{IOSRCKI}$ | All | 0.52 | 0.57 | 0.75 | ns, min |
| **Set/Reset Delays** | | | | | | |
| SR input to IQ (asynchronous) | $T_{IOSRIQ}$ | All | 1.13 | 1.27 | 1.42 | ns, max |
| GSR to output IQ | $T_{GSRQ}$ | All | 5.87 | 6.75 | 7.43 | ns, max |

**Notes:**
1. Input timing for LVCMOS25 is measured at 1.25V. For other I/O standards, see Table 39.

## IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVCMOS25 with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments.

*Table 37:* **IOB Output Switching Characteristics**

| | | Speed Grade | | | |
|---|---|---|---|---|---|
| **Description** | **Symbol** | **-7** | **-6** | **-5** | **Units** |
| **Propagation Delays** | | | | | |
| O input to Pad | $T_{IOOP}$ | 1.58 | 1.68 | 1.85 | ns, max |
| O input to Pad via transparent latch | $T_{IOOLP}$ | 1.65 | 1.82 | 1.99 | ns, max |
| **3-State Delays** | | | | | |
| T input to Pad high-impedance(2) | $T_{IOTHZ}$ | 1.23 | 1.35 | 1.51 | ns, max |
| T input to valid data on Pad | $T_{IOTP}$ | 1.51 | 1.63 | 1.78 | ns, max |
| T input to Pad high-impedance via transparent latch(2) | $T_{IOTLPHZ}$ | 1.08 | 1.22 | 1.36 | ns, max |
| T input to valid data on Pad via transparent latch | $T_{IOTLPON}$ | 1.56 | 1.69 | 1.85 | ns, max |
| GTS to Pad high-impedance(2) | $T_{GTS}$ | 4.11 | 4.73 | 5.20 | ns, max |
| **Sequential Delays** | | | | | |
| Clock CLK to Pad | $T_{IOCKP}$ | 1.59 | 1.76 | 1.93 | ns, max |
| Clock CLK to Pad high-impedance (synchronous)(2) | $T_{IOCKHZ}$ | 1.39 | 1.55 | 1.73 | ns, max |
| Clock CLK to valid data on Pad (synchronous) | $T_{IOCKON}$ | 1.67 | 1.82 | 2.00 | ns, max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| O input | $T_{IOOCK}/T_{IOCKO}$ | 0.23/ 0.12 | 0.26/ 0.14 | 0.29/ 0.15 | ns, min |
| OCE input | $T_{IOOCECK}/T_{IOCKOCE}$ | 0.39/ 0.01 | 0.44/ 0.01 | 0.49/ 0.01 | ns, min |
| SR input (OFF) | $T_{IOSRCKO}/T_{IOCKOSR}$ | 0.52/ 0.00 | 0.57/ 0.00 | 0.75/ 0.00 | ns, min |
| 3–State Setup Times, T input | $T_{IOTCK}/T_{IOCKT}$ | 0.23/ 0.12 | 0.26/ 0.14 | 0.29/ 0.15 | ns, min |
| 3-State Setup Times, TCE input | $T_{IOTCECK}/T_{IOCKTCE}$ | 0.39/ 0.01 | 0.44/ 0.01 | 0.49/ 0.01 | ns, min |
| 3-State Setup Times, SR input (TFF) | $T_{IOSRCKT}/T_{IOCKTSR}$ | 0.52/ 0.00 | 0.57/ 0.00 | 0.75/ 0.00 | ns, min |
| **Set/Reset Delays** | | | | | |
| Minimum Pulse Width, SR inputs (asynchronous) | $T_{RPW}$ | 0.37 | 0.40 | 0.45 | ns, min |
| SR input to Pad (asynchronous) | $T_{IOSRP}$ | 2.33 | 2.56 | 2.83 | ns, max |
| SR input to Pad high-impedance (asynchronous)(2) | $T_{IOSRHZ}$ | 1.97 | 2.16 | 2.41 | ns, max |
| SR input to valid data on Pad (asynchronous) | $T_{IOSRON}$ | 2.24 | 2.44 | 2.69 | ns, max |
| GSR to Pad | $T_{IOGSRQ}$ | 5.87 | 6.75 | 7.43 | ns, max |

**Notes:**
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. The 3-state turn-off delays should not be adjusted.

*Table 7:* **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 |
| 2 | IO_L31P_2 | F26 | | | |
| 2 | IO_L32N_2 | G22 | | | |
| 2 | IO_L32P_2 | H22 | | | |
| 2 | IO_L34N_2/VREF_2 | G23 | | | |
| 2 | IO_L34P_2 | G24 | | | |
| 2 | IO_L36N_2 | G25 | | | |
| 2 | IO_L36P_2 | G26 | | | |
| 2 | IO_L37N_2 | H20 | | | |
| 2 | IO_L37P_2 | H21 | | | |
| 2 | IO_L38N_2 | H25 | | | |
| 2 | IO_L38P_2 | H26 | | | |
| 2 | IO_L40N_2/VREF_2 | J19 | | | |
| 2 | IO_L40P_2 | J20 | | | |
| 2 | IO_L42N_2 | J21 | | | |
| 2 | IO_L42P_2 | J22 | | | |
| 2 | IO_L43N_2 | J23 | | | |
| 2 | IO_L43P_2 | J24 | | | |
| 2 | IO_L44N_2 | J25 | | | |
| 2 | IO_L44P_2 | J26 | | | |
| 2 | IO_L46N_2/VREF_2 | K19 | | | |
| 2 | IO_L46P_2 | L19 | | | |
| 2 | IO_L48N_2 | K22 | | | |
| 2 | IO_L48P_2 | K23 | | | |
| 2 | IO_L49N_2 | K24 | | | |
| 2 | IO_L49P_2 | L24 | | | |
| 2 | IO_L50N_2 | K25 | | | |
| 2 | IO_L50P_2 | K26 | | | |
| 2 | IO_L52N_2/VREF_2 | L20 | | | |
| 2 | IO_L52P_2 | M20 | | | |
| 2 | IO_L54N_2 | L21 | | | |
| 2 | IO_L54P_2 | L22 | | | |
| 2 | IO_L55N_2 | L25 | | | |
| 2 | IO_L55P_2 | L26 | | | |
| 2 | IO_L56N_2 | M18 | | | |
| 2 | IO_L56P_2 | M19 | | | |

*Table 7:* **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 |
| 3 | VCCO_3 | AB24 | | | |
| 4 | VCCO_4 | U14 | | | |
| 4 | VCCO_4 | U15 | | | |
| 4 | VCCO_4 | V16 | | | |
| 4 | VCCO_4 | V17 | | | |
| 4 | VCCO_4 | AC16 | | | |
| 4 | VCCO_4 | AD19 | | | |
| 4 | VCCO_4 | AD22 | | | |
| 5 | VCCO_5 | U12 | | | |
| 5 | VCCO_5 | U13 | | | |
| 5 | VCCO_5 | V10 | | | |
| 5 | VCCO_5 | V11 | | | |
| 5 | VCCO_5 | AC11 | | | |
| 5 | VCCO_5 | AD5 | | | |
| 5 | VCCO_5 | AD8 | | | |
| 6 | VCCO_6 | P10 | | | |
| 6 | VCCO_6 | R10 | | | |
| 6 | VCCO_6 | T4 | | | |
| 6 | VCCO_6 | T9 | | | |
| 6 | VCCO_6 | U9 | | | |
| 6 | VCCO_6 | W3 | | | |
| 6 | VCCO_6 | AB3 | | | |
| 7 | VCCO_7 | E3 | | | |
| 7 | VCCO_7 | H3 | | | |
| 7 | VCCO_7 | K9 | | | |
| 7 | VCCO_7 | L4 | | | |
| 7 | VCCO_7 | L9 | | | |
| 7 | VCCO_7 | M10 | | | |
| 7 | VCCO_7 | N10 | | | |
| | | | | | |
| N/A | PROG_B | B1 | | | |
| N/A | HSWAP_EN | B3 | | | |
| N/A | DXP | A3 | | | |
| N/A | DXN | C4 | | | |
| N/A | AVCCAUXTX4 | B5 | | | |

*Table 7:* **FG676/FGG676 — XC2VP20, XC2VP30, and XC2VP40**

| Bank | Pin Description | Pin Number | No Connects | | |
|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 |
| N/A | GND | H4 | | | |
| N/A | GND | H23 | | | |
| N/A | GND | K6 | | | |
| N/A | GND | K21 | | | |
| N/A | GND | L11 | | | |
| N/A | GND | L12 | | | |
| N/A | GND | L13 | | | |
| N/A | GND | L14 | | | |
| N/A | GND | L15 | | | |
| N/A | GND | L16 | | | |
| N/A | GND | M3 | | | |
| N/A | GND | M11 | | | |
| N/A | GND | M12 | | | |
| N/A | GND | M13 | | | |
| N/A | GND | M14 | | | |
| N/A | GND | M15 | | | |
| N/A | GND | M16 | | | |
| N/A | GND | M24 | | | |
| N/A | GND | N11 | | | |
| N/A | GND | N12 | | | |
| N/A | GND | N13 | | | |
| N/A | GND | N14 | | | |
| N/A | GND | N15 | | | |
| N/A | GND | N16 | | | |
| N/A | GND | P11 | | | |
| N/A | GND | P12 | | | |
| N/A | GND | P13 | | | |
| N/A | GND | P14 | | | |
| N/A | GND | P15 | | | |
| N/A | GND | P16 | | | |
| N/A | GND | R3 | | | |
| N/A | GND | R11 | | | |
| N/A | GND | R12 | | | |
| N/A | GND | R13 | | | |
| N/A | GND | R14 | | | |

*Table 10:* **FF1152 — XC2VP20, XC2VP30, XC2VP40, and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | | | |
|---|---|---|---|---|---|---|
| | | | XC2VP20 | XC2VP30 | XC2VP40 | XC2VP50 |
| 7 | VCCO_7 | T23 | | | | |
| 7 | VCCO_7 | U23 | | | | |
| | | | | | | |
| N/A | CCLK | AE9 | | | | |
| N/A | PROG_B | J26 | | | | |
| N/A | DONE | AE10 | | | | |
| N/A | M0 | AF26 | | | | |
| N/A | M1 | AE26 | | | | |
| N/A | M2 | AE25 | | | | |
| N/A | TCK | J9 | | | | |
| N/A | TDI | H28 | | | | |
| N/A | TDO | H7 | | | | |
| N/A | TMS | K10 | | | | |
| N/A | PWRDWN_B | AF9 | | | | |
| N/A | HSWAP_EN | K25 | | | | |
| N/A | RSVD | G8 | | | | |
| N/A | VBATT | K9 | | | | |
| N/A | DXP | K26 | | | | |
| N/A | DXN | G27 | | | | |
| N/A | AVCCAUXTX2 | B32 | NC | NC | | |
| N/A | VTTXPAD2 | B33 | NC | NC | | |
| N/A | TXNPAD2 | A33 | NC | NC | | |
| N/A | TXPPAD2 | A32 | NC | NC | | |
| N/A | GNDA2 | C30 | NC | NC | | |
| N/A | RXPPAD2 | A31 | NC | NC | | |
| N/A | RXNPAD2 | A30 | NC | NC | | |
| N/A | VTRXPAD2 | B31 | NC | NC | | |
| N/A | AVCCAUXRX2 | B30 | NC | NC | | |
| N/A | AVCCAUXTX4 | B28 | | | | |
| N/A | VTTXPAD4 | B29 | | | | |
| N/A | TXNPAD4 | A29 | | | | |
| N/A | TXPPAD4 | A28 | | | | |
| N/A | GNDA4 | C27 | | | | |
| N/A | RXPPAD4 | A27 | | | | |
| N/A | RXNPAD4 | A26 | | | | |
| N/A | VTRXPAD4 | B27 | | | | |
| N/A | AVCCAUXRX4 | B26 | | | | |
| N/A | AVCCAUXTX5 | B24 | NC | NC | NC | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| 4 | IO_L47N_4 | AE15 | | |
| 4 | IO_L47P_4 | AD15 | | |
| 4 | IO_L48N_4 | AM14 | | |
| 4 | IO_L48P_4 | AL14 | | |
| 4 | IO_L49N_4 | AP14 | | |
| 4 | IO_L49P_4 | AN14 | | |
| 4 | IO_L50_4/No_Pair | AH15 | | |
| 4 | IO_L53_4/No_Pair | AG16 | | |
| 4 | IO_L54N_4 | AK15 | | |
| 4 | IO_L54P_4 | AJ15 | | |
| 4 | IO_L55N_4 | AM15 | | |
| 4 | IO_L55P_4 | AL16 | | |
| 4 | IO_L56N_4 | AE16 | | |
| 4 | IO_L56P_4 | AD16 | | |
| 4 | IO_L57N_4 | AP15 | | |
| 4 | IO_L57P_4/VREF_4 | AN15 | | |
| 4 | IO_L66N_4 | AJ16 | NC | |
| 4 | IO_L66P_4/VREF_4 | AH16 | NC | |
| 4 | IO_L67N_4 | AN16 | | |
| 4 | IO_L67P_4 | AM16 | | |
| 4 | IO_L68N_4 | AG17 | | |
| 4 | IO_L68P_4 | AF17 | | |
| 4 | IO_L69N_4 | AJ17 | | |
| 4 | IO_L69P_4/VREF_4 | AH17 | | |
| 4 | IO_L73N_4 | AL17 | | |
| 4 | IO_L73P_4 | AK17 | | |
| 4 | IO_L74N_4/GCLK3S | AE17 | | |
| 4 | IO_L74P_4/GCLK2P | AD17 | | |
| 4 | IO_L75N_4/GCLK1S | AN17 | | |
| 4 | IO_L75P_4/GCLK0P | AM17 | | |
| | | | | |
| 5 | IO_L75N_5/GCLK7S | AM18 | | |
| 5 | IO_L75P_5/GCLK6P | AN18 | | |
| 5 | IO_L74N_5/GCLK5S | AD18 | | |
| 5 | IO_L74P_5/GCLK4P | AE18 | | |
| 5 | IO_L73N_5 | AK18 | | |
| 5 | IO_L73P_5 | AL18 | | |
| 5 | IO_L69N_5/VREF_5 | AH18 | | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| 6 | IO_L44N_6 | AA28 | | |
| 6 | IO_L45P_6 | AC31 | | |
| 6 | IO_L45N_6/VREF_6 | AC32 | | |
| 6 | IO_L46P_6 | AC29 | | |
| 6 | IO_L46N_6 | AC30 | | |
| 6 | IO_L47P_6 | AA24 | | |
| 6 | IO_L47N_6 | AA25 | | |
| 6 | IO_L48P_6 | AB32 | | |
| 6 | IO_L48N_6 | AB33 | | |
| 6 | IO_L49P_6 | AB28 | | |
| 6 | IO_L49N_6 | AB29 | | |
| 6 | IO_L50P_6 | AA26 | | |
| 6 | IO_L50N_6 | Y26 | | |
| 6 | IO_L51P_6 | AA33 | | |
| 6 | IO_L51N_6/VREF_6 | AA34 | | |
| 6 | IO_L52P_6 | AB31 | | |
| 6 | IO_L52N_6 | AA31 | | |
| 6 | IO_L53P_6 | Y24 | | |
| 6 | IO_L53N_6 | Y25 | | |
| 6 | IO_L54P_6 | AA29 | | |
| 6 | IO_L54N_6 | AA30 | | |
| 6 | IO_L55P_6 | Y33 | | |
| 6 | IO_L55N_6 | Y34 | | |
| 6 | IO_L56P_6 | Y28 | | |
| 6 | IO_L56N_6 | W27 | | |
| 6 | IO_L57P_6 | AA32 | | |
| 6 | IO_L57N_6/VREF_6 | Y32 | | |
| 6 | IO_L58P_6 | Y29 | | |
| 6 | IO_L58N_6 | Y30 | | |
| 6 | IO_L59P_6 | W24 | | |
| 6 | IO_L59N_6 | W25 | | |
| 6 | IO_L60P_6 | W31 | | |
| 6 | IO_L60N_6 | W32 | | |
| 6 | IO_L85P_6 | W28 | | |
| 6 | IO_L85N_6 | W29 | | |
| 6 | IO_L86P_6 | V26 | | |
| 6 | IO_L86N_6 | V27 | | |
| 6 | IO_L87P_6 | W33 | | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| N/A | VCCINT | M23 | | |
| N/A | VCCINT | AB22 | | |
| N/A | VCCINT | AA22 | | |
| N/A | VCCINT | Y22 | | |
| N/A | VCCINT | W22 | | |
| N/A | VCCINT | V22 | | |
| N/A | VCCINT | U22 | | |
| N/A | VCCINT | T22 | | |
| N/A | VCCINT | R22 | | |
| N/A | VCCINT | P22 | | |
| N/A | VCCINT | N22 | | |
| N/A | VCCINT | AB21 | | |
| N/A | VCCINT | N21 | | |
| N/A | VCCINT | AB20 | | |
| N/A | VCCINT | N20 | | |
| N/A | VCCINT | AB19 | | |
| N/A | VCCINT | N19 | | |
| N/A | VCCINT | AB18 | | |
| N/A | VCCINT | N18 | | |
| N/A | VCCINT | AB17 | | |
| N/A | VCCINT | N17 | | |
| N/A | VCCINT | AB16 | | |
| N/A | VCCINT | N16 | | |
| N/A | VCCINT | AB15 | | |
| N/A | VCCINT | N15 | | |
| N/A | VCCINT | AB14 | | |
| N/A | VCCINT | N14 | | |
| N/A | VCCINT | AB13 | | |
| N/A | VCCINT | AA13 | | |
| N/A | VCCINT | Y13 | | |
| N/A | VCCINT | W13 | | |
| N/A | VCCINT | V13 | | |
| N/A | VCCINT | U13 | | |
| N/A | VCCINT | T13 | | |
| N/A | VCCINT | R13 | | |
| N/A | VCCINT | P13 | | |
| N/A | VCCINT | N13 | | |
| N/A | VCCINT | AC12 | | |

*Table 11:* **FF1148 — XC2VP40 and XC2VP50**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP40 | XC2VP50 |
| N/A | GND | AP19 | | |
| N/A | GND | AK19 | | |
| N/A | GND | AF19 | | |
| N/A | GND | AA19 | | |
| N/A | GND | Y19 | | |
| N/A | GND | W19 | | |
| N/A | GND | V19 | | |
| N/A | GND | U19 | | |
| N/A | GND | T19 | | |
| N/A | GND | R19 | | |
| N/A | GND | P19 | | |
| N/A | GND | J19 | | |
| N/A | GND | E19 | | |
| N/A | GND | A19 | | |
| N/A | GND | AP18 | | |
| N/A | GND | AA18 | | |
| N/A | GND | Y18 | | |
| N/A | GND | W18 | | |
| N/A | GND | V18 | | |
| N/A | GND | U18 | | |
| N/A | GND | T18 | | |
| N/A | GND | R18 | | |
| N/A | GND | P18 | | |
| N/A | GND | A18 | | |
| N/A | GND | AA17 | | |
| N/A | GND | Y17 | | |
| N/A | GND | W17 | | |
| N/A | GND | V17 | | |
| N/A | GND | U17 | | |
| N/A | GND | T17 | | |
| N/A | GND | R17 | | |
| N/A | GND | P17 | | |
| N/A | GND | AP16 | | |
| N/A | GND | AK16 | | |
| N/A | GND | AF16 | | |
| N/A | GND | AA16 | | |
| N/A | GND | Y16 | | |
| N/A | GND | W16 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| 6 | IO_L04P_6 | AR33 | | |
| 6 | IO_L04N_6 | AP33 | | |
| 6 | IO_L05P_6 | AM32 | | |
| 6 | IO_L05N_6 | AL31 | | |
| 6 | IO_L06P_6 | AT34 | | |
| 6 | IO_L06N_6 | AR34 | | |
| 6 | IO_L73P_6 | AU35 | NC | |
| 6 | IO_L73N_6 | AT35 | NC | |
| 6 | IO_L75P_6 | AT38 | NC | |
| 6 | IO_L75N_6/VREF_6 | AT39 | NC | |
| 6 | IO_L76P_6 | AR37 | NC | |
| 6 | IO_L76N_6 | AR38 | NC | |
| 6 | IO_L78P_6 | AP38 | NC | |
| 6 | IO_L78N_6 | AP39 | NC | |
| 6 | IO_L79P_6 | AP36 | NC | |
| 6 | IO_L79N_6 | AP37 | NC | |
| 6 | IO_L81P_6 | AP35 | NC | |
| 6 | IO_L81N_6/VREF_6 | AN35 | NC | |
| 6 | IO_L82P_6 | AN38 | NC | |
| 6 | IO_L82N_6 | AN39 | NC | |
| 6 | IO_L84P_6 | AN36 | NC | |
| 6 | IO_L84N_6 | AN37 | NC | |
| 6 | IO_L07P_6 | AN33 | | |
| 6 | IO_L07N_6 | AN34 | | |
| 6 | IO_L08P_6 | AK31 | | |
| 6 | IO_L08N_6 | AK32 | | |
| 6 | IO_L09P_6 | AM37 | | |
| 6 | IO_L09N_6/VREF_6 | AM38 | | |
| 6 | IO_L10P_6 | AM36 | | |
| 6 | IO_L10N_6 | AL35 | | |
| 6 | IO_L11P_6 | AJ31 | | |
| 6 | IO_L11N_6 | AH30 | | |
| 6 | IO_L12P_6 | AM33 | | |
| 6 | IO_L12N_6 | AM34 | | |
| 6 | IO_L13P_6 | AL38 | | |
| 6 | IO_L13N_6 | AL39 | | |
| 6 | IO_L14P_6 | AH29 | | |
| 6 | IO_L14N_6 | AG29 | | |

*Table 12:* **FF1517 — XC2VP50 and XC2VP70**

| Bank | Pin Description | Pin Number | No Connects | |
|---|---|---|---|---|
| | | | XC2VP50 | XC2VP70 |
| N/A | VCCAUX | AP6 | | |
| N/A | VCCAUX | F6 | | |
| N/A | VCCAUX | AR5 | | |
| N/A | VCCAUX | E5 | | |
| N/A | VCCAUX | AW2 | | |
| N/A | VCCAUX | Y2 | | |
| N/A | VCCAUX | A2 | | |
| N/A | VCCAUX | AV1 | | |
| N/A | VCCAUX | AA1 | | |
| N/A | VCCAUX | Y1 | | |
| N/A | VCCAUX | W1 | | |
| N/A | VCCAUX | B1 | | |
| | | | | |
| N/A | GND | A3 | | |
| N/A | GND | AV2 | | |
| N/A | GND | AU2 | | |
| N/A | GND | AA2 | | |
| N/A | GND | W2 | | |
| N/A | GND | C2 | | |
| N/A | GND | B2 | | |
| N/A | GND | AU1 | | |
| N/A | GND | AM1 | | |
| N/A | GND | AH1 | | |
| N/A | GND | AD1 | | |
| N/A | GND | T1 | | |
| N/A | GND | M1 | | |
| N/A | GND | H1 | | |
| N/A | GND | C1 | | |
| N/A | GND | AD5 | | |
| N/A | GND | T5 | | |
| N/A | GND | M5 | | |
| N/A | GND | H5 | | |
| N/A | GND | AU4 | | |
| N/A | GND | AT4 | | |
| N/A | GND | D4 | | |
| N/A | GND | C4 | | |
| N/A | GND | AW3 | | |
| N/A | GND | AV3 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 3 | IO_L77N_3 | | AT3 | | |
| 3 | IO_L77P_3 | | AT4 | | |
| 3 | IO_L76N_3 | | AU1 | | |
| 3 | IO_L76P_3 | | AU2 | | |
| 3 | IO_L75N_3/VREF_3 | | AU3 | | |
| 3 | IO_L75P_3 | | AU4 | | |
| 3 | IO_L74N_3 | | AV3 | | |
| 3 | IO_L74P_3 | | AW3 | | |
| 3 | IO_L73N_3 | | AV1 | | |
| 3 | IO_L73P_3 | | AV2 | | |
| 3 | IO_L06N_3 | | AW1 | | |
| 3 | IO_L06P_3 | | AW2 | | |
| 3 | IO_L05N_3 | | AT8 | | |
| 3 | IO_L05P_3 | | AU8 | | |
| 3 | IO_L04N_3 | | AT6 | | |
| 3 | IO_L04P_3 | | AU7 | | |
| 3 | IO_L03N_3/VREF_3 | | AY5 | | |
| 3 | IO_L03P_3 | | AY6 | | |
| 3 | IO_L02N_3 | | AV7 | | |
| 3 | IO_L02P_3 | | AW7 | | |
| 3 | IO_L01N_3/VRP_3 | | AV6 | | |
| 3 | IO_L01P_3/VRN_3 | | AW6 | | |
| | | | | | |
| 4 | IO_L01N_4/BUSY/DOUT(1) | | AT9 | | |
| 4 | IO_L01P_4/INIT_B | | AR9 | | |
| 4 | IO_L02N_4/D0/DIN(1) | | AU9 | | |
| 4 | IO_L02P_4/D1 | | AV9 | | |
| 4 | IO_L03N_4/D2 | | AY9 | | |
| 4 | IO_L03P_4/D3 | | AW9 | | |
| 4 | IO_L05_4/No_Pair | | AN11 | | |
| 4 | IO_L06N_4/VRP_4 | | AR10 | | |
| 4 | IO_L06P_4/VRN_4 | | AP10 | | |
| 4 | IO_L07N_4 | | AU10 | | |
| 4 | IO_L07P_4/VREF_4 | | AT10 | | |
| 4 | IO_L08N_4 | | AV10 | | |
| 4 | IO_L08P_4 | | AW10 | | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| 4 | IO_L09N_4 | | AR11 | | |
| 4 | IO_L09P_4/VREF_4 | | AP11 | | |
| 4 | IO_L19N_4 | | AV11 | | |
| 4 | IO_L19P_4 | | AU11 | | |
| 4 | IO_L20N_4 | | AY10 | | |
| 4 | IO_L20P_4 | | AY11 | | |
| 4 | IO_L21N_4 | | AN12 | | |
| 4 | IO_L21P_4 | | AM12 | | |
| 4 | IO_L25N_4 | | AR12 | | |
| 4 | IO_L25P_4 | | AP12 | | |
| 4 | IO_L26N_4 | | AT12 | | |
| 4 | IO_L26P_4 | | AU12 | | |
| 4 | IO_L27N_4 | | AW12 | | |
| 4 | IO_L27P_4/VREF_4 | | AV12 | | |
| 4 | IO_L28N_4 | | AM13 | | |
| 4 | IO_L28P_4 | | AL13 | | |
| 4 | IO_L29N_4 | | AP13 | | |
| 4 | IO_L29P_4 | | AN13 | | |
| 4 | IO_L30N_4 | | AT13 | | |
| 4 | IO_L30P_4 | | AR13 | | |
| 4 | IO_L34N_4 | | AV13 | | |
| 4 | IO_L34P_4 | | AU13 | | |
| 4 | IO_L35N_4 | | AW13 | | |
| 4 | IO_L35P_4 | | AY13 | | |
| 4 | IO_L36N_4 | | AL15 | | |
| 4 | IO_L36P_4/VREF_4 | | AL14 | | |
| 4 | IO_L78N_4 | | AN14 | NC | |
| 4 | IO_L78P_4 | | AM14 | NC | |
| 4 | IO_L83_4/No_Pair | | AR14 | NC | |
| 4 | IO_L84N_4 | | AU14 | NC | |
| 4 | IO_L84P_4 | | AT14 | NC | |
| 4 | IO_L85N_4 | | AW14 | NC | |
| 4 | IO_L85P_4 | | AV14 | NC | |
| 4 | IO_L86N_4 | | AM15 | NC | |
| 4 | IO_L86P_4 | | AN15 | NC | |
| 4 | IO_L87N_4 | | AR15 | NC | |

*Table 13:* **FF1704 — XC2VP70, XC2VPX70, and XC2VP100**

| Bank | Pin Description | | Pin Number | No Connects | |
|---|---|---|---|---|---|
| | Virtex-II Pro Devices | XC2VPX70 (if Different) | | XC2VP70, XC2VPX70 | XC2VP100 |
| N/A | VCCAUX | | AM11 | | |
| N/A | VCCAUX | | AN33 | | |
| N/A | VCCAUX | | AN10 | | |
| N/A | VCCAUX | | AV39 | | |
| N/A | VCCAUX | | AV4 | | |
| N/A | VCCAUX | | AW38 | | |
| N/A | VCCAUX | | AW22 | | |
| N/A | VCCAUX | | AW21 | | |
| N/A | VCCAUX | | AW5 | | |
| N/A | VCCAUX | | AA42 | | |
| N/A | VCCAUX | | AA41 | | |
| N/A | VCCAUX | | AA2 | | |
| N/A | VCCAUX | | AA1 | | |
| N/A | VCCAUX | | Y42 | | |
| N/A | VCCAUX | | Y1 | | |
| N/A | VCCAUX | | L32 | | |
| N/A | VCCAUX | | L11 | | |
| N/A | VCCAUX | | K33 | | |
| N/A | VCCAUX | | K10 | | |
| N/A | VCCAUX | | E39 | | |
| N/A | VCCAUX | | E4 | | |
| N/A | VCCAUX | | D38 | | |
| N/A | VCCAUX | | D22 | | |
| N/A | VCCAUX | | D21 | | |
| N/A | VCCAUX | | D5 | | |
| N/A | GND | | AB38 | | |
| N/A | GND | | AB35 | | |
| N/A | GND | | AB32 | | |
| N/A | GND | | AB26 | | |
| N/A | GND | | AB25 | | |
| N/A | GND | | AB24 | | |
| N/A | GND | | AB23 | | |
| N/A | GND | | AB22 | | |
| N/A | GND | | AB21 | | |
| N/A | GND | | AB20 | | |
| N/A | GND | | AB19 | | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 0 | IO_L11N_0 | M25 | NC |
| 0 | IO_L11P_0 | M26 | NC |
| 0 | IO_L12N_0 | F26 | NC |
| 0 | IO_L12P_0 | G26 | NC |
| 0 | IO_L18N_0 | B26 | NC |
| 0 | IO_L18P_0/VREF_0 | C26 | NC |
| 0 | IO_L46N_0 | G24 | |
| 0 | IO_L46P_0 | G25 | |
| 0 | IO_L47N_0 | K26 | |
| 0 | IO_L47P_0 | L26 | |
| 0 | IO_L48N_0 | E25 | |
| 0 | IO_L48P_0 | F25 | |
| 0 | IO_L49N_0 | C24 | |
| 0 | IO_L49P_0 | C25 | |
| 0 | IO_L50_0/No_Pair | L24 | |
| 0 | IO_L53_0/No_Pair | L25 | |
| 0 | IO_L54N_0 | A25 | |
| 0 | IO_L54P_0 | B25 | |
| 0 | IO_L55N_0 | H23 | |
| 0 | IO_L55P_0 | H24 | |
| 0 | IO_L56N_0 | J25 | |
| 0 | IO_L56P_0 | K25 | |
| 0 | IO_L57N_0 | E24 | |
| 0 | IO_L57P_0/VREF_0 | F24 | |
| 0 | IO_L58N_0 | D23 | |
| 0 | IO_L58P_0 | D24 | |
| 0 | IO_L59N_0 | J24 | |
| 0 | IO_L59P_0 | K24 | |
| 0 | IO_L60N_0 | A24 | |
| 0 | IO_L60P_0 | B24 | |
| 0 | IO_L64N_0 | F23 | |
| 0 | IO_L64P_0 | G23 | |
| 0 | IO_L65N_0 | M22 | |
| 0 | IO_L65P_0 | M23 | |
| 0 | IO_L66N_0 | B23 | |
| 0 | IO_L66P_0/VREF_0 | C23 | |
| 0 | IO_L67N_0 | H22 | |

*Table 14:* **FF1696 — XC2VP100**

| Bank | Pin Description | Pin Number | No Connects |
|---|---|---|---|
| | | | XC2VP100 |
| 2 | IO_L40P_2 | R5 | |
| 2 | IO_L41N_2 | V6 | |
| 2 | IO_L41P_2 | V7 | |
| 2 | IO_L42N_2 | R3 | |
| 2 | IO_L42P_2 | P3 | |
| 2 | IO_L43N_2 | R1 | |
| 2 | IO_L43P_2 | R2 | |
| 2 | IO_L44N_2 | W10 | |
| 2 | IO_L44P_2 | W11 | |
| 2 | IO_L45N_2 | T7 | |
| 2 | IO_L45P_2 | R7 | |
| 2 | IO_L46N_2/VREF_2 | T4 | |
| 2 | IO_L46P_2 | T5 | |
| 2 | IO_L47N_2 | W9 | |
| 2 | IO_L47P_2 | Y10 | |
| 2 | IO_L48N_2 | T1 | |
| 2 | IO_L48P_2 | T2 | |
| 2 | IO_L49N_2 | U6 | |
| 2 | IO_L49P_2 | T6 | |
| 2 | IO_L50N_2 | W7 | |
| 2 | IO_L50P_2 | Y8 | |
| 2 | IO_L51N_2 | U4 | |
| 2 | IO_L51P_2 | T3 | |
| 2 | IO_L52N_2/VREF_2 | U2 | |
| 2 | IO_L52P_2 | U3 | |
| 2 | IO_L53N_2 | Y11 | |
| 2 | IO_L53P_2 | Y12 | |
| 2 | IO_L54N_2 | V4 | |
| 2 | IO_L54P_2 | V5 | |
| 2 | IO_L55N_2 | V1 | |
| 2 | IO_L55P_2 | V2 | |
| 2 | IO_L56N_2 | Y6 | |
| 2 | IO_L56P_2 | Y7 | |
| 2 | IO_L57N_2 | W5 | |
| 2 | IO_L57P_2 | W6 | |
| 2 | IO_L58N_2/VREF_2 | W3 | |
| 2 | IO_L58P_2 | V3 | |